5 to 60V Three-Phase Brushless DC Motor Pre-Driver

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with Following Results:
  - Device Temperature Grade 1
- Wide Operating Voltage: 5V to 60V
- Charge Pump Gate Drive Supply
- 100% Duty Operation with Trickle Charge Circuit
- 1A Maximum Peak Source Current
- 2A Maximum Peak Sink Current
- 3.3V and 5V Logic Compatible
- Low-Power Sleep Mode
- Adjustable Dead-Time
- Fault Indication Output
- Full Protection Features
  - Over Current Protection
  - Short Circuit Protection
  - Input Undervoltage Lockout
  - Gate Driver Undervoltage Lockout
  - Bootstrap Undervoltage Protection
  - Thermal Shutdown Protection
- Available in QFN-28L(4mm×5mm) Package

DESCRIPTION

The SCT55611Q is a highly integrated gate driver IC for three-phase Brushless DC(BLDC) motor control. It is capable of driving 3 high-side and 3 low-side N-channel MOSFETs with a wide input supply range from 5V to 60V.

The SCT55611Q supports 100% duty operation with an internal trickle charge circuit to maintain high-side gate driver voltage. Low-power sleep mode is supported to achieve low stand-by current.

The SCT55611Q provides full protection features, including over current protection, short circuit protection, input undervoltage lockout, gate driver undervoltage lockout, bootstrap undervoltage protection and thermal shutdown protection. Fault conditions are indicated through an open-drain output pin(nFAULT).

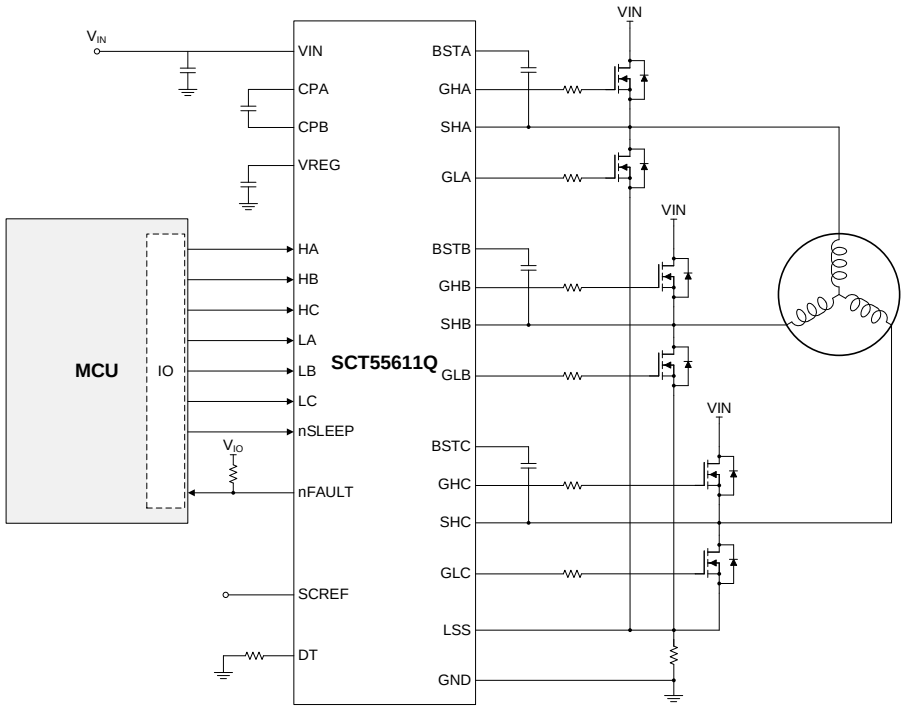
The device is available in 4mm×5mm QFN-28L package with wettable flanks.

APPLICATIONS

- Three-Phase Brushless DC Motor
- Automotive Actuators, Fans and Pumps

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TYPICAL APPLICATION



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REVISION HISTORY

Revision 0.8: Customer Sample.

DEVICE ORDER INFORMATION

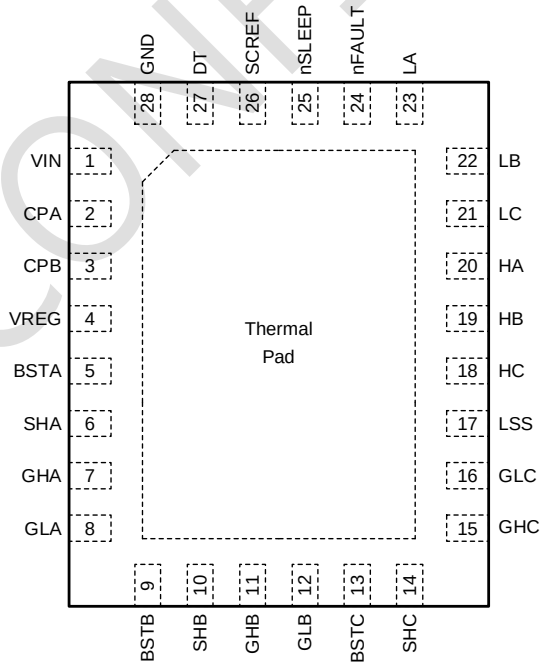
ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL
SCT55611QQZBR	Tape & Reel	5000	5611Q	28	QFN 4×5-28L	2

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN	-0.3	62	V
CPA	-0.3	13	V
CPB	-0.3	6	V
VREG	-0.3	13	V
BSTA - SHA, BSTB - SHB, BSTC - SHC	-0.3	13	V
GHA - SHA, GHB - SHB, GHC - SHC	-0.3	13	V
SHA, SHB, SHC	-0.3	65	V
GLA, GLB, GLC	-0.3	13	V
LSS	-0.3	1	V
HA, HB, HC, LA, LB, LC, DT, SCREF, nSLEEP, nFAULT	-0.3	6	V
Operation junction temperature T_J (2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

PIN CONFIGURATION



Top View: 28-Lead QFN 4mm×5mm

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes thermal shutdown protection to protect the device during overload conditions. Junction temperature will exceed 175°C when thermal shutdown protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

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PIN FUNCTIONS

NAME	PIN	PIN FUNCTION
VIN	1	Input supply voltage. Connect a bypass capacitor close to the pin.
CPA	2	Charge pump switching node. Connect a ceramic capacitor between CPA and CPB.
CPB	3	
VREG	4	Gate driver supply output. Connect a ceramic capacitor to ground.
BSTA	5	Phase A bootstrap pin. Connect a ceramic capacitor between BSTA and SHA.
SHA	6	Phase A high-side source pin. Connect to the source of high-side FET.
GHA	7	Phase A high-side gate driver output. Connect to the gate of high-side FET.
GLA	8	Phase A low-side gate driver output. Connect to the gate of low-side FET.
BSTB	9	Phase B bootstrap pin. Connect a ceramic capacitor between BSTB and SHB.
SHB	10	Phase B high-side source pin. Connect to the source of high-side FET.
GHB	11	Phase B high-side gate driver output. Connect to the gate of high-side FET.
GLB	12	Phase B low-side gate driver output. Connect to the gate of low-side FET.
BSTC	13	Phase C bootstrap pin. Connect a ceramic capacitor between BSTC and SHC.
SHC	14	Phase C high-side source pin. Connect to the source of high-side FET.
GHC	15	Phase C high-side gate driver output. Connect to the gate of high-side FET.
GLC	16	Phase C low-side gate driver output. Connect to the gate of low-side FET.
LSS	17	Low-side source pin. Connect to the sources of phase A/B/C low side FET.
HC	18	Phase C high-side drive signal input pin. Internal pulldown.
HB	19	Phase B high-side drive signal input pin. Internal pulldown.
HA	20	Phase A high-side drive signal input pin. Internal pulldown.
LC	21	Phase C low-side drive signal input pin. Internal pulldown.
LB	22	Phase B low-side drive signal input pin. Internal pulldown.
LA	23	Phase A low-side drive signal input pin. Internal pulldown.
nFAULT	24	Fault indication output pin. Open-drain output and pulled low when in a fault condition. Connect an external pull-up resistor to an external supply.
nSLEEP	25	Sleep mode input pin. Logic low to enter low-power sleep mode and high to exit. Internal pulldown.
SCREF	26	Short circuit protection reference input pin.
DT	27	Dead-time setting pin. Connect a resistor to ground to set the dead-time.
GND	28	Ground.

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RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	5	60	V
V_{SCREF}	SCREF voltage	0.125	2.4	V
T_J	Operating junction temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins(2)	-1	+1	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	QFN-28L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	37.1	°C/W
$R_{\theta JC\ (top)}$	Junction to case (top) thermal resistance(1)	40.7	
$R_{\theta JC\ (bot)}$	Junction to case (bottom) thermal resistance(1)	7.4	
$R_{\theta JB}$	Junction to board thermal resistance(1)	16.7	
$R_{\psi JT}$	Junction-to-top characterization parameter	5.1	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT55611Q is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT55611Q. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, T_J = -40°C to 150°C, unless otherwise stated. Typical values are at T_J = 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Input Supply Voltage		5		60	V
I_Q	Quiescent Current	nSLEEP = 1, gate not switching		1	2	mA
I_{SLEEP}		nSLEEP = 0			3	uA
Control Logic						
V_{IL}	Input Logic Low Threshold				0.8	V
V_{IH}	Input Logic High Threshold		2			V
$I_{IN(H)}$	Logic Input Current	V_{IH}=5V	-20		20	uA
$I_{IN(L)}$		V_{IL}=0.8V	-20		20	uA
$I_{SLEEP-PD}$	nSLEEP Pull-down Current			1		uA
R_{PD}	Internal Pull-down Resistance	All logic inputs except nSLEEP		820		kΩ

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SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
nFAULT (Open-Drain Output)						
V_{OL}	Output low voltage	I_O=5mA			0.5	V
I_{OH}	Output high leakage current	V_O=3.3V			1	uA
Protection Circuits						
V_{IN_RISE}	VIN UVLO Rising Threshold			4.2	4.5	V
V_{IN_HYS}	VIN UVLO Hysteresis			200		mV
V_{REG_RISE}	VREG UVLO Rising Threshold			7.6		V
V_{REG_HYS}	VREG UVLO Hysteresis			1.6		V
V_{SC}	Short-Circuit Threshold Accuracy (MOSFET V_{DS})	V_{SCREF}=1V	0.85	1	1.15	V
		V_{SCREF}=2.4V	2.18	2.4	2.62	V
t_{OC}	OCP Deglitch Time			3		us
t_{SLEEP}	SLEEP Wakeup Time	VREG cap=10uF		250		us
$V_{LSS-OCP}$	LSS OCP threshold		0.4	0.5	0.6	V
T_{TSD}	Thermal Shutdown			175		°C
V_{BSTUV}	BSTx-SWx Falling Threshold			4.3		V
Gate Driver						
V_{FBOOT}	Bootstrap Diode Forward Voltage	I_D=10mA		1		V
V_{REG}	VREG Output Voltage	V_{IN}=6~60V	10.5	11.3	12	V
		V_{IN}=5~6V	8.5			V
I_{OSO}(1)	Maximum source current			1		A
I_{OSI}(1)	Maximum sink current			2		A
R_{UP}	Gate drive pull-up resistance	V_{DS}=1V		6		Ω
R_{HS_DN}	HS gate drive pull-down resistance	V_{DS}=1V	0.2		3	Ω
R_{LS_DN}	LS gate drive pull-down resistance	V_{DS}=1V	1		3	Ω
f_{CP}	Charge pump frequency			110		kHz
t_{DEAD}	Dead Time	DT open		5		us
		R_{DT}=200kΩ		0.74(1)		us
		DT tied to GND		30(1)		ns

(1) Guaranteed by sample characterization, not tested in production.

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TYPICAL CHARACTERISTICS

V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

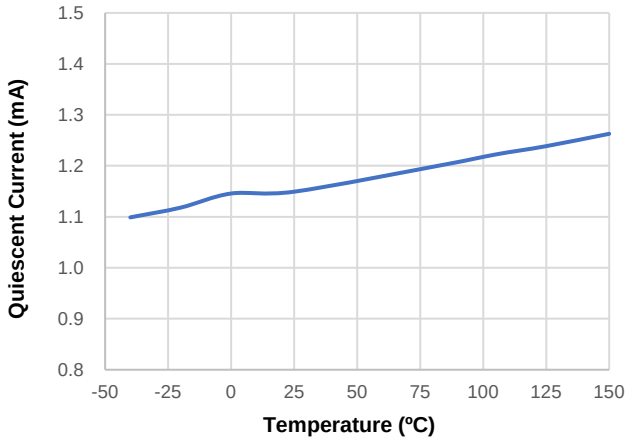


Figure 1. Quiescent Current vs. Temperature

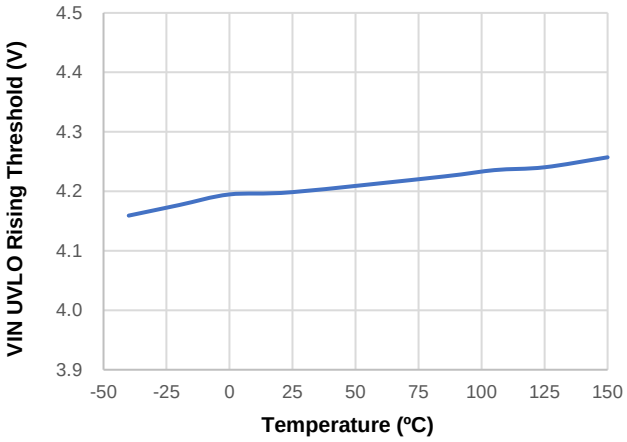


Figure 2. VIN UVLO Rising vs. Temperature

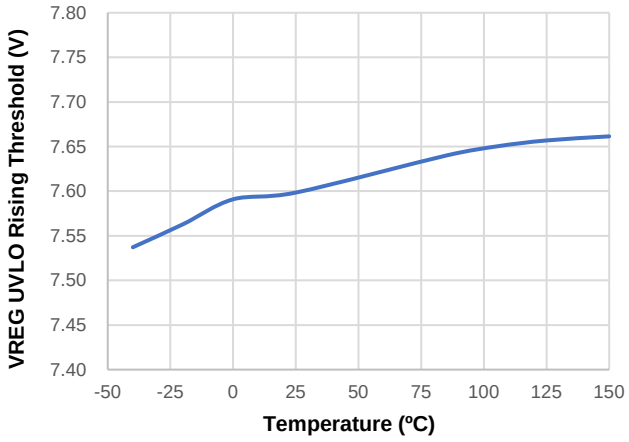


Figure 3. VREG UVLO Rising vs. Temperature

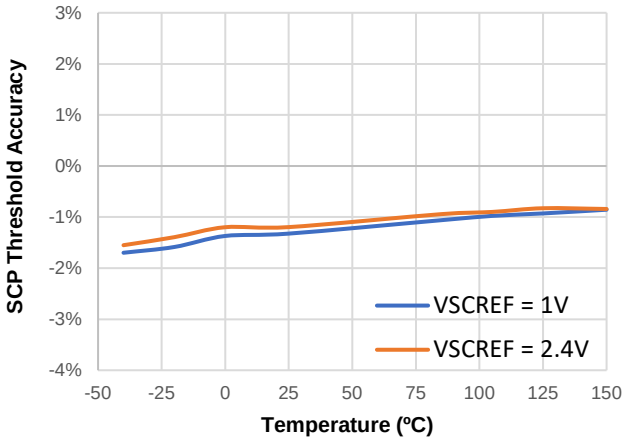


Figure 4. SCP Threshold Accuracy vs. Temperature

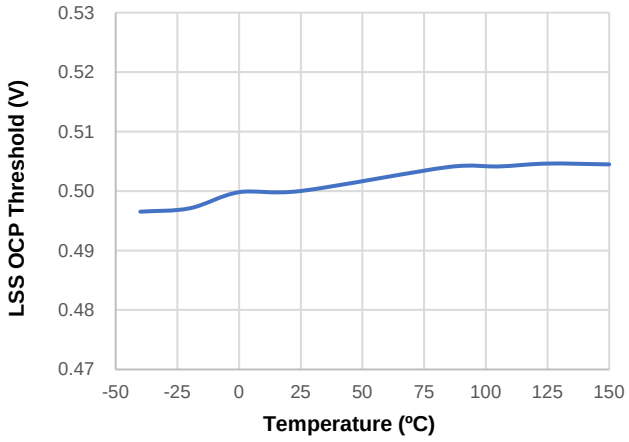


Figure 5. LSS OCP Threshold vs. Temperature

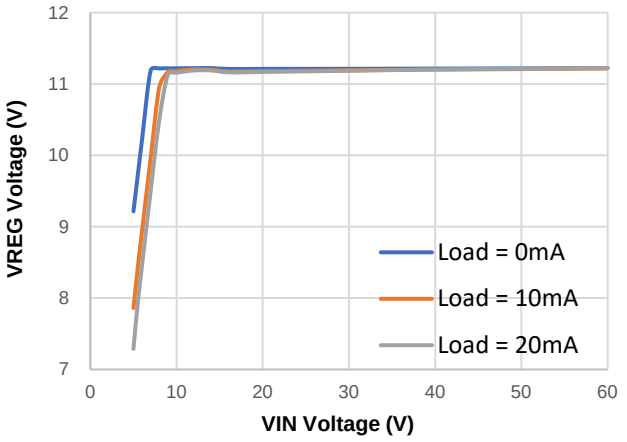


Figure 6. VREG Voltage Regulation

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FUNCTIONAL BLOCK DIAGRAM

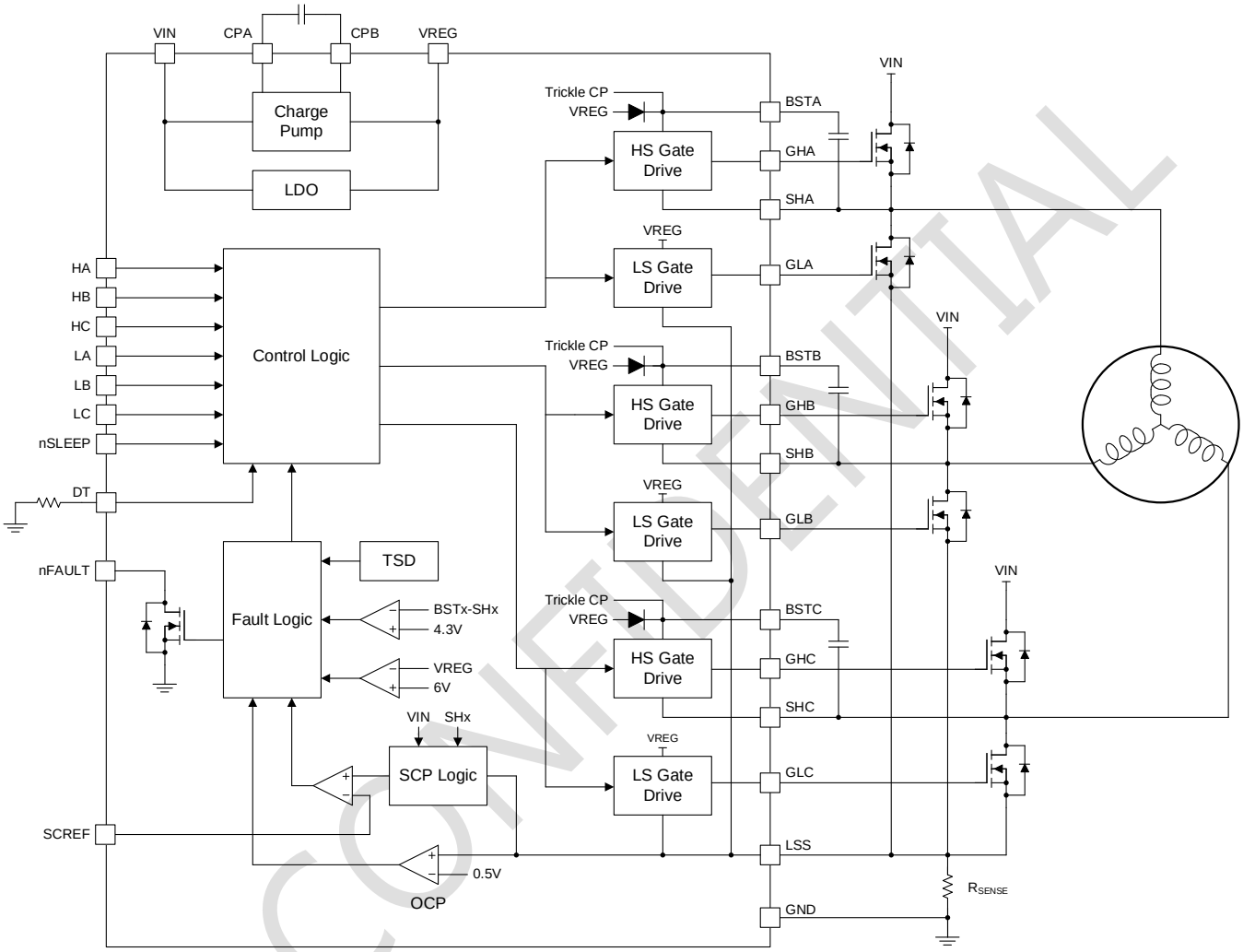


Figure 7. Functional Block Diagram

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OPERATION

Overview

The SCT55611Q is a highly integrated gate driver IC designed for three-phase Brushless DC(BLDC) motor control with the ability to drive three high-side and three low-side N-channel MOSFETs. Each channel can source up to 1A peak current and sink up to 2A peak current, with flexible dead time configuration by an external resistor. It uses a charge pump to generate the gate drive power to operate over a wide input voltage range from 5V to 60V. It also supports 100% duty operation with an internal trickle charge circuit to maintain high-side gate driver voltage. Low-power sleep mode is supported to achieve low stand-by current.

The SCT55611Q provides full protection features, including over current protection, short circuit protection, input undervoltage lockout, gate driver undervoltage lockout, bootstrap undervoltage protection and thermal shutdown protection to timely shut down and properly protect the system from various failures. Meanwhile, these fault conditions are indicated through an open-drain output pin, nFAULT, for real-time monitoring and warning.

3-Phase Gate Drive

The SCT55611Q consists of 3 half-bridge gate drivers (phase A, B, C), which could be used in combination to implement 3-phase motor control, or used separately for any other application. The gate drive power is supplied from VREG, which is regulated at around 11V and generated from an internal charge pump when VIN is low, and from an internal LDO when VIN is high enough. A 10uF ceramic capacitor close to VREG pin and a 470nF ceramic capacitor between CPA and CPB pins are suggested to stabilize the gate drive power for most applications.

An internal trickle charge pump is integrated to support 100% duty operation, where the high-side MOSFET keeps on and the trickle charge circuit provides a small current to balance the leakage on the BSTx node.

All the gate driver outputs have an internal pulldown which is activated when the SCT55611Q is shut down or in sleep mode to prevent unexpected turning-on of MOSFETs. After it is back to normal operation, the internal pulldown is disabled.

Input Logic

The SCT55611Q generates the gate drive outputs based on the input logic signals at HA/B/C and LA/B/C pins. HA/B/C and LA/B/C pins have internal pulldown to avoid noise when floating. Refer to Table 1 for the truth table.

Table 1. Input Logic Truth Table

Hx	Lx	GHx	GLx	SHx
0	0	L	L	Hi-Z
0	1	L	H	GND
1	0	H	L	VIN
1	1	L	L	Hi-Z

Dead Time Adjustment

The DT pin configures the gate drive dead time with an external resistor connected to ground. The dead time could be calculated with Equation (1):

$$t_{dead}(ns) = 3.7 \times R_{DT}(k\Omega) \quad (1)$$

If DT pin is directly tied to ground, a minimum dead time of around 30ns will be applied. If DT pin is left floating, a maximum dead time of around 5us will be applied.

Sleep Mode

The SCT55611Q can enter a low-power sleep mode where most internal circuits are turned off to save power. All the gate drivers are disabled in sleep mode. The sleep mode is entered by pulling nSLEEP pin low, and exited by pulling nSLEEP pin high with a wakeup delay of around 250us. The nSLEEP pin has an internal pulldown so it must

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be pulled high for normal operation.

Over Current Protection

The SCT55611Q protects the system from over-current failure by monitoring LSS pin voltage and timely shutting down when it is over 0.5V. The LSS pin is connected to the sources of the three low-side MOSFETs, and tied to ground through an external sense resistor, whose voltage drop equals the resistance multiplied by the total current of the three phases. For example, if a 50mΩ sense resistor is used, the over current protection will be triggered once the total current exceeds 10A. When an over-current condition is detected for over 3us deglitch time, all the gate driver outputs are driven low immediately and nFAULT pin is pulled low. The SCT55611Q will be latched in the fault state even after the over-current condition is gone, and only reset by toggling nSLEEP pin or power cycle.

Over current protection can be disabled by connecting LSS pin directly to ground or connecting SCREF pin to VREG through a 100kΩ resistor.

Short Circuit Protection

The SCT55611Q protects the system from short-circuit failure by monitoring the drain-to-source voltage drop of the turned-on MOSFET through VIN, SHx and LSS pins. In a short-circuit case, the current running through the MOSFET immediately increases and so does the voltage across the MOSFET. When a voltage drop higher than the short-circuit threshold is detected for over 3us deglitch time, all the gate driver outputs are driven low immediately and nFAULT pin is pulled low. The short-circuit threshold is set by SCREF pin with an external voltage reference. The SCT55611Q will be latched in the fault state even after the short-circuit condition is gone, and only reset by toggling nSLEEP pin or power cycle.

Short circuit protection can be disabled by connecting SCREF pin to VREG through a 100kΩ resistor.

Undervoltage Lockout Protection

The SCT55611Q monitors VIN, VREG and bootstrap voltage and shuts down when any of them falls lower than its undervoltage lockout threshold. In these cases, the SCT55611Q will pull all gate driver outputs low immediately, latched in the fault state and only reset by toggling nSLEEP pin or power cycle. See Electrical Characteristics table for detailed undervoltage lockout thresholds.

Thermal Shutdown

Once the junction temperature of SCT55611Q exceeds 175ºC, the thermal sensing circuit shuts down the device. All the gate driver outputs are driven low immediately and nFAULT pin is pulled low. The SCT55611Q will automatically restart once the junction temperature falls below 155ºC. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

Fault Action and Response

The fault action and response of SCT55611Q are listed in Table 2.

Table 2. Fault Action and Response

Fault	Condition	Report	Gate Driver	Recovery
VIN UVLO	V_{IN} < 4V	None	Pulled low	V_{IN} > 4.2V
VREG UVLO	V_{REG} < 6V	nFAULT	Pulled low	Latched
BST UVLO	BSTx - SWx < 4.3V	nFAULT	Pulled low	Latched
Over-current	V_{LSS} > 0.5V	nFAULT	Pulled low	Latched
Short-circuit	V_{DS_ON} > V_{SCREF}	nFAULT	Pulled low	Latched
Thermal Shutdown	T_J > 175°C	nFAULT	Pulled low	T_J < 155°C

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APPLICATION INFORMATION

Typical Application

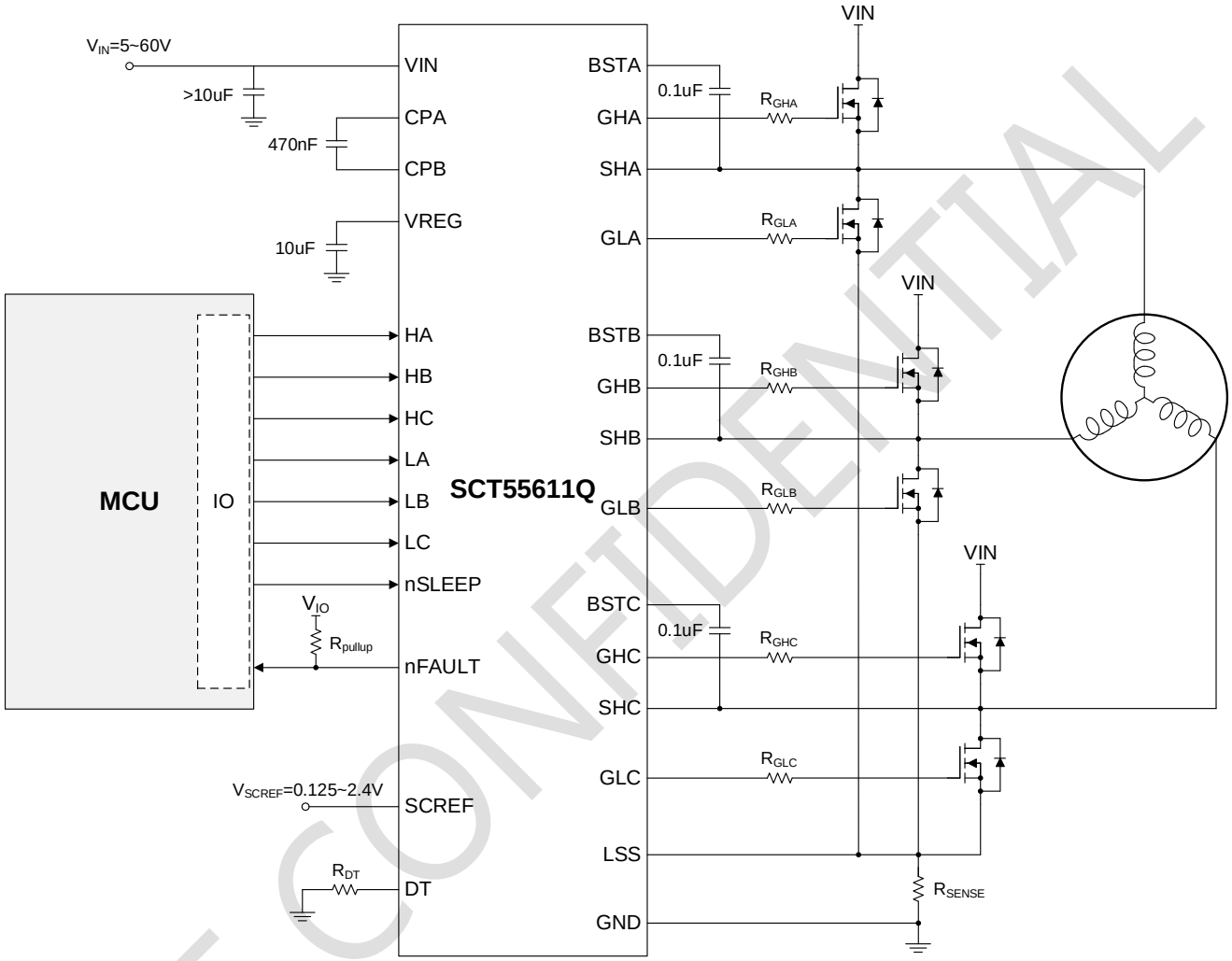


Figure 8. Three-Phase BLDC Motor Driver

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Driver Power Dissipation

Generally, the power dissipation in the SCT55611Q depends on the driver-stage loss and V_{REG} regulation loss.

The power loss of a single gate driver can be estimated by Equation (2):

$$P_{Gtdrv} = Q_g \times V_{REG} \times f_{sw} \quad (2)$$

where

- Q_g is the total gate charge of the power device
- f_{SW} is the switching frequency
- V_{REG} is the gate drive voltage

If the gate resistor R_G applied between the driver output and gate of power device to slow down the switching transition, the power loss of a single gate driver can be estimated by Equation (3):

$$P_{Gtdrv} = \frac{1}{2} \times Q_g \times V_{REG} \times f_{sw} \times \left(\frac{R_{UP}}{R_{UP} + R_G} + \frac{R_{DN}}{R_{DN} + R_G} \right) \quad (3)$$

where

- R_{UP} is the gate driver pull-up resistance
- R_{DN} is the gate driver pull-down resistance
- R_G is the external resistance between the driver output and gate of power device

For a typical three-phase BLDC motor control, always only one of the three half-bridges are switching at f_{SW} during the whole rotation cycle. In this case, the total driver-stage power dissipation can be estimated by one half-bridge, namely a high-side gate driver and a low-side gate driver.

The gate drive voltage V_{REG} is generated from VIN through either a charge pump when VIN is low or a LDO when VIN is high. The power loss of V_{REG} regulation can be estimated referring to Table 3:

Table 3. V_{REG} Regulation Loss

Input Range	Mode	Power Loss Equation
VIN < 16V	Charge Pump	$P_{REG} = \left(2 \times \frac{V_{IN}}{V_{REG}} - 1\right) \times P_{Gtdrv_total}$
VIN > 16V	LDO	$P_{REG} = \left(\frac{V_{IN}}{V_{REG}} - 1\right) \times P_{Gtdrv_total}$

Thermal Considerations

The maximum IC junction temperature should be restricted to 150°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation (4):

$$P_{D(MAX)} = \frac{150 - T_A}{R_{\theta JA}} \quad (4)$$

where

- T_A is the maximum ambient temperature for the application
- $R_{\theta JA}$ is the junction-to-ambient thermal resistance given in the Thermal Information table

The real junction-to-ambient thermal resistance $R_{\theta JA}$ of the package greatly depends on the PCB type, layout, and environmental factor. Soldering the ground pin to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

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Application Waveforms

V_{IN} = 24V, V_{SCREF} = 0.5V, f_{PWM} = 20kHz, T_A = 25°C, unless otherwise noted.

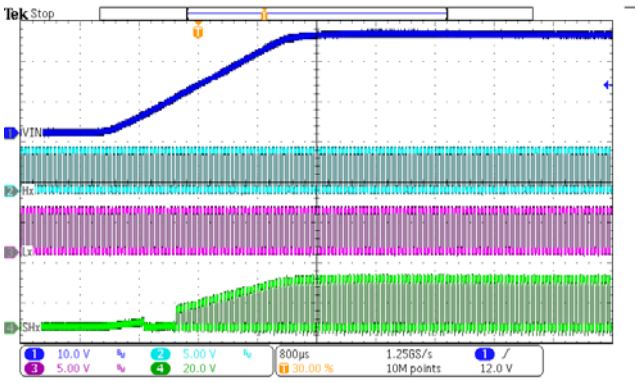


Figure 9. Power Ramp Up

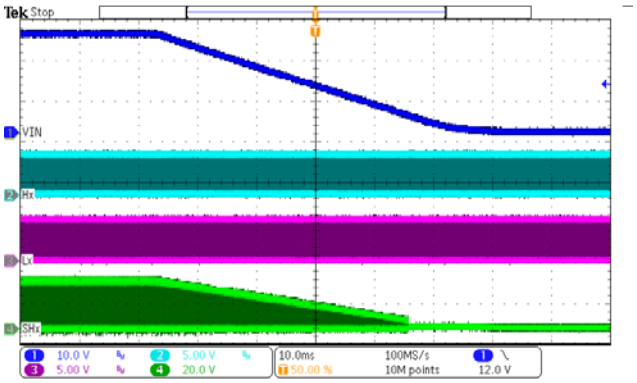


Figure 10. Power Ramp Down

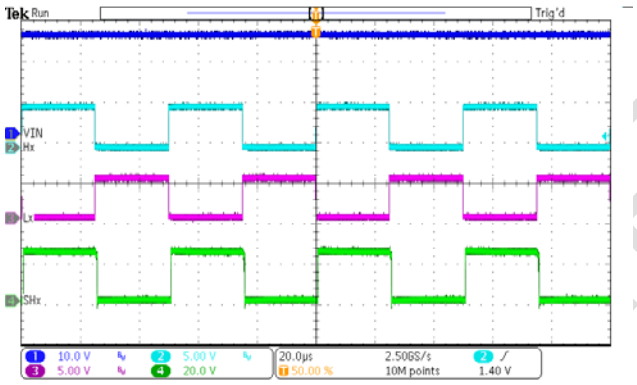


Figure 11. Steady State

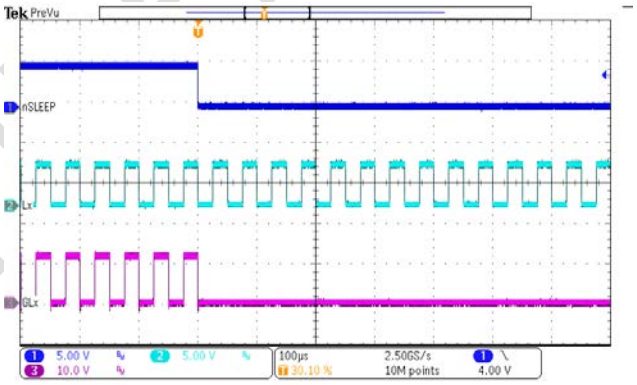


Figure 12. Sleep Mode Entry

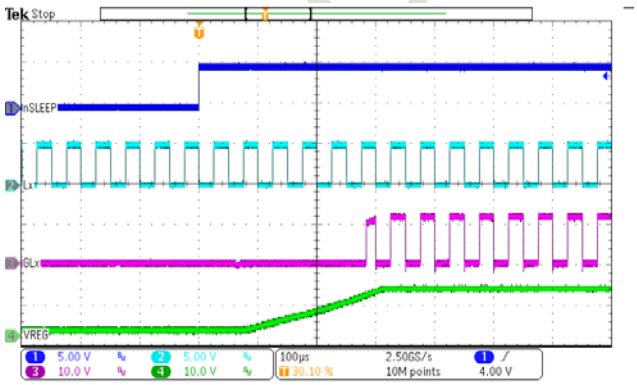


Figure 13. Sleep Mode Recovery

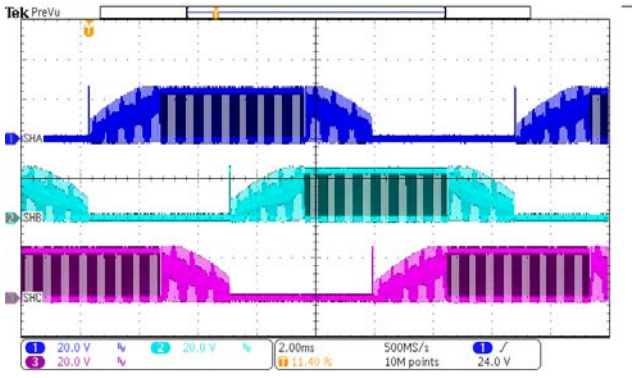


Figure 14. 3-Phase BLDC Motor Operation

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Layout Guideline

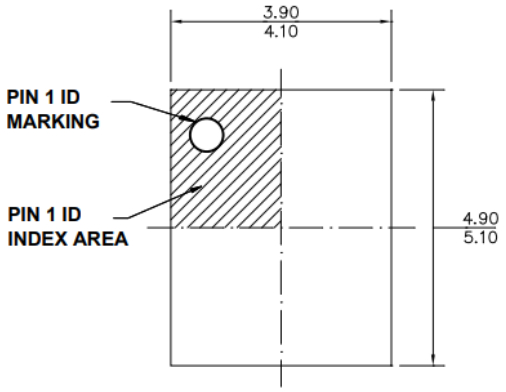
The SCT55611Q provides high output driving current and features very short rising and falling time at the gate of power device. The high di/dt might cause driver output unexpected ringing when the driver output loop is not designed well. The system could suffer from malfunction and EMI noise problems if the power device gate has serious ringing. For better performance, follow the layout guidelines as shown below.

1. Put the SCT55611Q as close as possible to the power device to minimize the gate driving loop including the driver output and power device gate.
2. Place the power supply decoupling capacitors as close as possible to the VIN pin. Low-ESR ceramic capacitors of type X5R or X7R are recommended.
3. Place the VREG capacitor close to VREG pin.
4. Place the charge pump capacitor close to CPA and CPB pins with minimized loop.
5. Place the bootstrap capacitors close to BSTx and SHx pins with minimized loop.
6. For the low-side sense resistor for over current protection, it is recommended to use a wide-package resistor or paralleled resistors to minimize the parasitic inductance introduced between the LSS pin and ground.
7. At least one ground plane is recommended to provide noise shielding and thermal dissipation. The device thermal pad should be soldered to the top-layer ground plane with multiply vias connected to the bottom-layer ground plane to achieve better thermal performance.

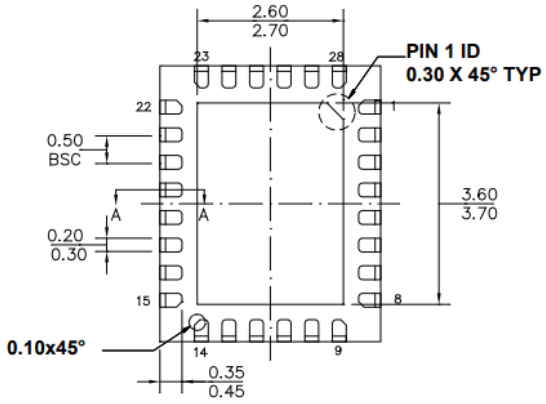
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PACKAGE INFORMATION



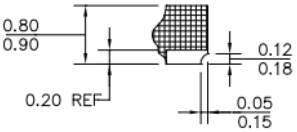
TOP VIEW



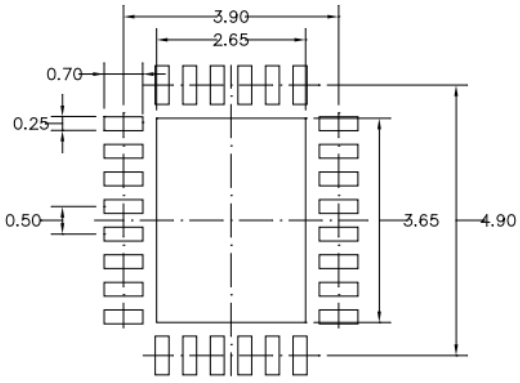
BOTTOM VIEW



SIDE VIEW



SECTION A-A



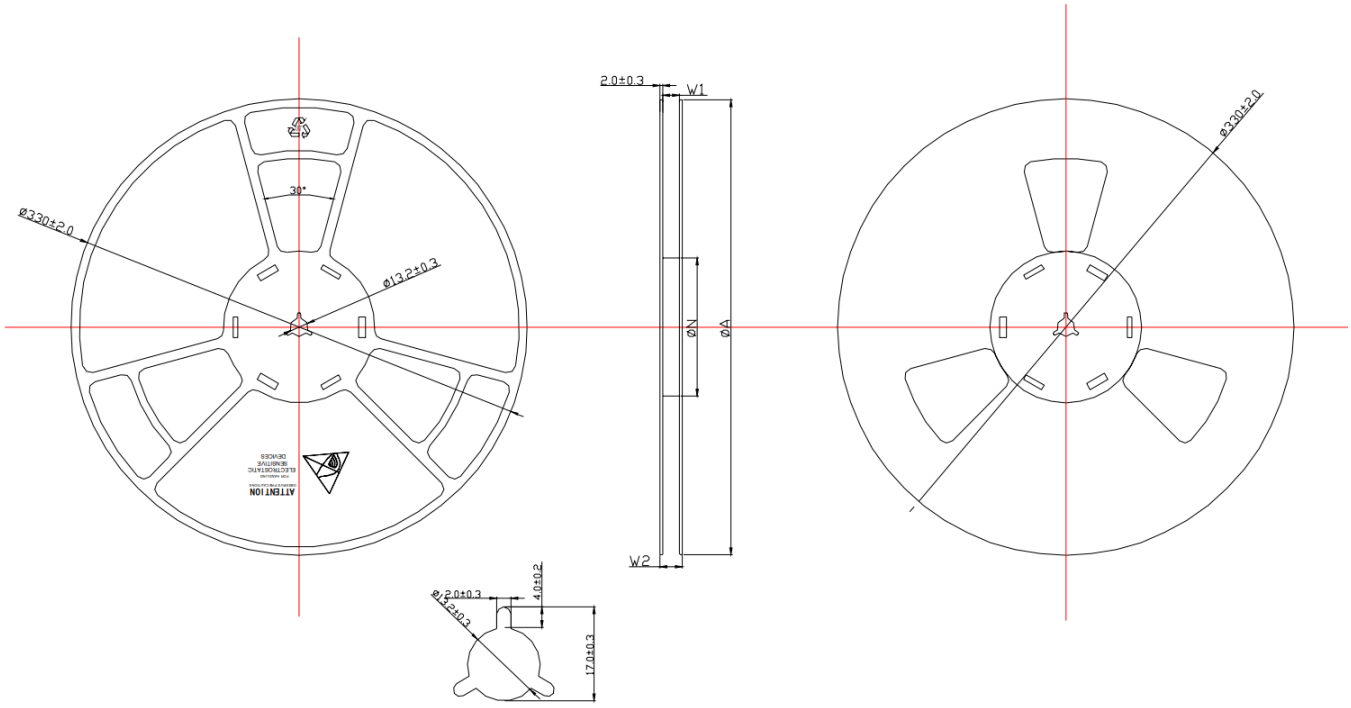
RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) DRAWING CONFIRMS TO JEDEC MO-220.
6) DRAWING IS NOT TO SCALE.

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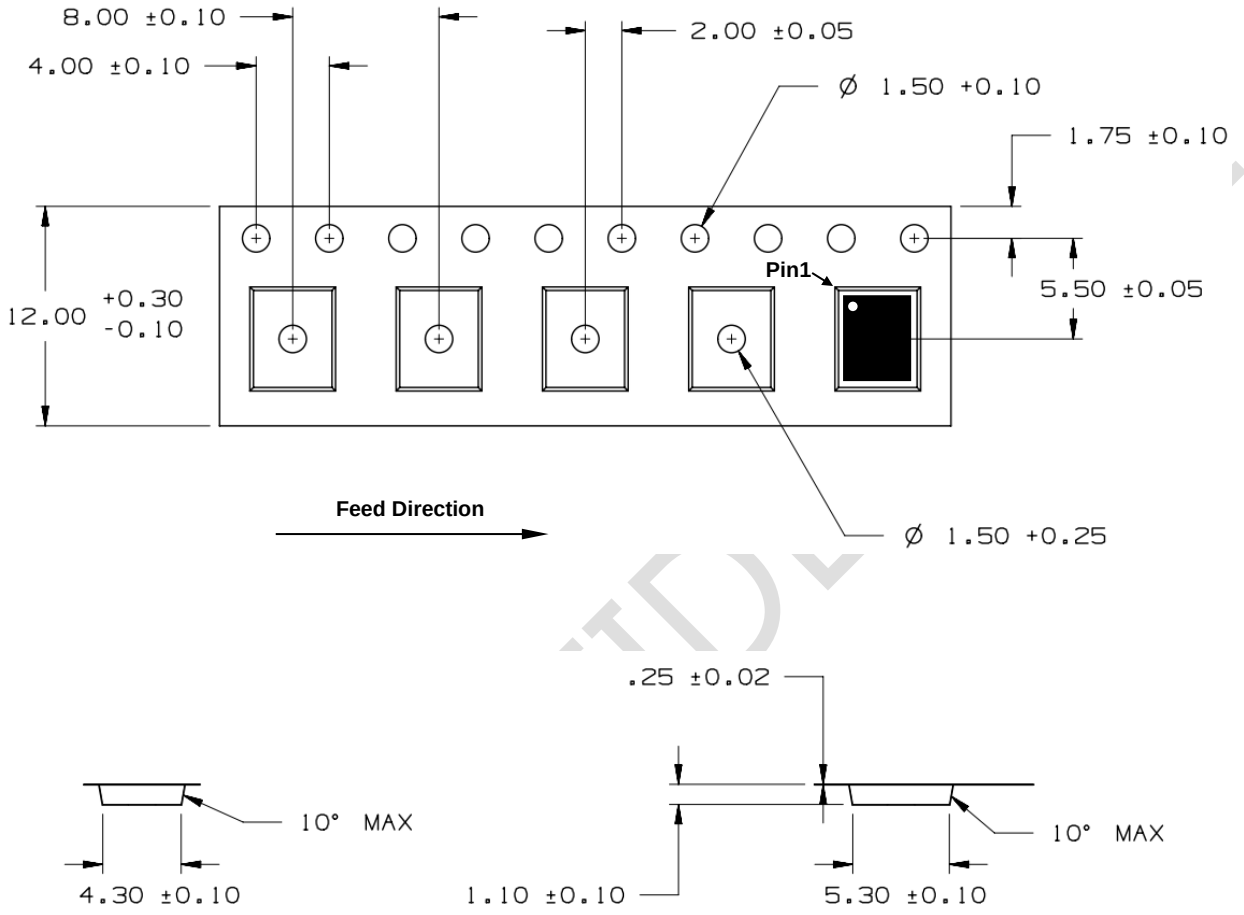
TAPE AND REEL INFORMATION



PRODUCT SPECIFICATIONS				
TYPE WIDTH	ØA	ØN	W1 (Min)	W2 (Max)
12MM	330±2.0	100±1.0	12.4	19.4
16mm	330±2.0	100±1.0	16.4	23.4
24MM	330±2.0	100±1.0	24.4	31.4
32MM	330±2.0	100±1.0	32.4	39.4
44MM	330±2.0	100±1.0	44.4	51.4

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TAPE AND REEL INFORMATION (continued)



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