19V Vin Five-Channel Power Management IC for Automotive Applications

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
- Wide Input Voltage Range: 4V-19V
- Three High-Efficiency Step-Down Converters:
  - HV Buck1: Vout1=3.1V-4V, up to 1.2A
  - LV Buck2: Vout2=1.1-3.3V, up to 1.2A
  - LV Buck3: Vout3=0.6-1.8V, up to 1.2A
  - 2.1MHz Switching Frequency with Optional Integrated Frequency Dither for EMI Mitigation
  - Forced-CCM Operation
- One High PSRR Low-Dropout Regulator (LDO):
  - LDO4: Vout4=2.7-3.3V, up to 300mA
  - High PSRR and Low Noise Design for Analog Power Rail
- One General Low-Dropout Regulator (LDO):
  - LDO5: Vout5=0.8-3.3V, up to 300mA
  - LDO5 Input Pin for Flexible Configuration
- Programmable Power Sequencer for Buck2, Buck3, LDO4 and LDO5
- Power Good Indicator with Open-drain Output
- Output Discharge
- Integrated Protection Features:
  - Programmable Input Under-voltage Protection
  - Input Over-voltage Protection
  - Output Over-voltage/Under-voltage Protection
  - Over-current Protection
  - Thermal Shutdown Protection
- Up to 1MHz I2C Interface with Optional Packet Error Checking (PEC)
- Available in QFN-20L(3mm×3mm) Package with Wettable Flanks

DESCRIPTION

The SCT61250Q is a highly integrated power management IC (PMIC) optimized for automotive camera system. It integrates three high-efficiency synchronous buck converters (HV Buck1, LV Buck2, LV Buck3), one high-PSRR low noise LDO (LDO4) and one general LDO (LDO5) with OV/UV monitoring and flexible power sequence for all outputs.

Buck1 has an input voltage range from 4V to 19V for connections to Power over Coax (PoC). Buck2 and Buck3 are two second stage converters and powered from the output of Buck1. All three buck converters operate in Forced-CCM mode with 2.1MHz switching frequency and optional Frequency Spread Spectrum (FSS) function for EMI mitigation. The output voltages are pre-programmed, which saves external feedback divider and minimizes system solution.

LDO4 is a high PSRR, low noise LDO designed for analog power rail. LDO5 is a general LDO with a separate voltage input pin for flexible configuration. Both LDO4 and LDO5 have pre-programmed output voltage and provide a continuous output current of up to 300mA.

The SCT61250Q integrates protection features including programmable input under-voltage protection, input over-voltage protection, output over-voltage/under-voltage protection, over-current protection and thermal shutdown.

With a compact 3mm×3mm QFN-20L package, the SCT61250Q greatly reduces external components count and PCB space.

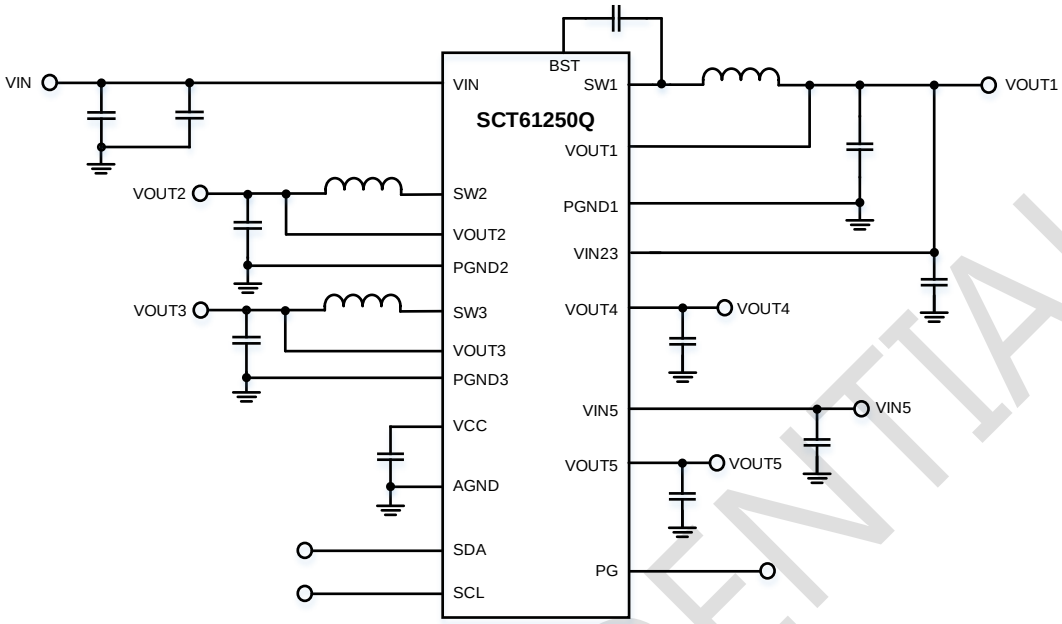
APPLICATIONS

- Automotive Camera Modules
- Compact Multi-channel Power Solution

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TYPICAL APPLICATION



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REVISION HISTORY

Revision 1.0: Release to market.

Revision 1.1: Updated package description, added application information and fixed few typos.

DEVICE ORDER INFORMATION

PART NUMBER	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL
SCT61250Q-xxxxQHBR	Tape & Reel	5000	1250Q	20	QFN3X3-20L	1

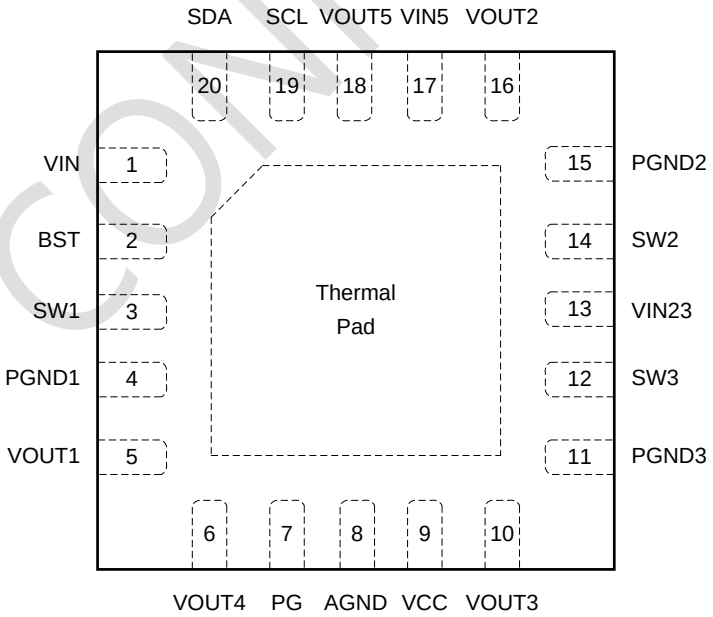
1) "xxxx" is the specific suffix code for different configuration. Contact SCT for details.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN	-0.3	21	V
SW1	-0.3(-1 in 30ns)	21	V
BST-SW1	-0.3	6	V
Others	-0.3	6	V
Operating junction temperature T_J (2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

PIN CONFIGURATION



Top View: 20-Lead QFN 3mm×3mm

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes thermal shutdown protection to protect the device during overload conditions. Junction temperature will exceed 170°C when thermal shutdown protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

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PIN FUNCTIONS

NAME	PIN	PIN FUNCTION
VIN	1	**Input supply for the device and Buck1.** A decoupling capacitor to ground is recommended to be placed close to VIN pin to minimize switching spikes.
BST	2	**Bootstrap capacitor connection pin for Buck1.** Connect a 0.1uF ceramic capacitor between this pin and SW1.
SW1	3	**Buck1 switch node.** SW is the output of the internal power switch. Connect to an external inductor using a wide PCB trace.
PGND1	4	**Power ground for Buck1.** Should be electrically connected to the system power ground plane with the shortest and lowest-impedance connection possible.
VOUT1	5	**Feedback for Buck1 and power source for LDO4.** Connect VOUT1 pin to Buck1 output directly. A decoupling capacitor to ground is recommended to be placed close to VOUT1 pin to minimize switching spikes.
VOUT4	6	**LDO4 output.** Connect a 4.7uF ceramic capacitor or higher between this pin and ground.
PG	7	**Open-drain power good indication.** High state of this pin indicates all channels work properly and low state indicates power rails are not ready or a fault condition. Connect this pin to high level through a pull-up resistor. Float this pin if not used.
AGND	8	**Analog ground.** AGND is the reference GND for the internal logic and signal circuit. AGND is not internally connected to power ground. Make sure AGND connected to power ground in PCB.
VCC	9	**Internal VCC regulator output.** Power supply to the internal control circuit and gate drivers. A 1uF capacitor to ground close to this pin is required.
VOUT3	10	**Feedback for Buck3.** Connect VOUT3 pin to the Buck3 output directly.
PGND3	11	**Power ground for Buck3.** Should be electrically connected to the system power ground plane with the shortest and lowest-impedance connection possible.
SW3	12	**Buck3 switch node.** SW is the output of the internal power switch. Connect to an external inductor using a wide PCB trace.
VIN23	13	**Input supply for Buck2 and Buck3.** VIN23 is assumed to be connected to the output of Buck1. Place a 10μF ceramic decoupling capacitor or higher close to VIN23 pin.
SW2	14	**Buck2 switch node.** SW is the output of the internal power switch. Connect to an external inductor using a wide PCB trace.
PGND2	15	**Power ground for Buck2.** Should be electrically connected to the system power ground plane with the shortest and lowest-impedance connection possible.
VOUT2	16	**Feedback for Buck2.** Connect VOUT2 pin to the Buck2 output directly.
VIN5	17	**Input supply for LDO5.** Place a 4.7μF ceramic decoupling capacitor or higher close to VIN5 pin.
VOUT5	18	**LDO5 output.** Connect a 4.7uF ceramic capacitor between this pin and ground.
SCL	19	**Serial clock line.** Connect this pin to ground if not used.
SDA	20	**Serial data line.** Open-Drain I/O. Connect this pin to high level with a pull-up resistor. Connect this pin to ground if not used.

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RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted.

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	VIN Input voltage range	4	19	V
V_{IN23}	VIN23 Input voltage range	3	4	V
V_{IN5}	VIN5 Input voltage range	1	4	V
V_{OUT1}	HV Buck1 output voltage range	3.1	4	V
V_{OUT2}	LV Buck2 output voltage range	1.1	3.3	V
V_{OUT3}	LV Buck3 output voltage range	0.6	1.8	V
V_{OUT4}	LDO4 output voltage range	2.7	3.3	V
V_{OUT5}	LDO5 output voltage range	0.8	3.3	V
T_J	Operating junction temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per AEC-Q100-002	-2	+2	kV
	Charged Device Model(CDM), per AEC-Q100-011	-1	+1	kV

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	QFN-20L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	55.52	°C/W
ψ_{JT}	Junction-to-top characterization parameter(1)	5.7	
ψ_{JB}	Junction-to-board characterization parameter(1)	12.06	
$R_{\theta JC\ (top)}$	Junction to case (top) thermal resistance(1)	60.6	
$R_{\theta JB}$	Junction to board thermal resistance(1)	12.42	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT61250Q is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT61250Q. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

Typical values correspond to V_{IN} = 10V, T_J = -40~150°C, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Input voltage range		4		19	V
V_{IN_UV}	Input under-voltage rising threshold	VIN_UV[1:0]=01		4.5		V
		VIN_UV[1:0]=10		5		V
		VIN_UV[1:0]=11		7.3		V
$V_{IN_UV_HYS}$	Input under-voltage hysteresis			500		mV
I_Q	Quiescent current from VIN	No load, non-switching		1	2	mA
I_{Q_ACTIVE}(1)	Quiescent current from VIN	No load, switching		10		mA

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SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
VCC Power						
V_{CC}	Internal linear regulator voltage			5		V
V_{CC_UV}	VCC under-voltage rising threshold			2.8		V
$V_{CC_UV_HYS}$	VCC under-voltage hysteresis			200		mV
V_{CC_OV}	VCC over-voltage rising threshold			5.4		V
$V_{CC_OV_HYS}$	VCC over-voltage hysteresis			200		mV
Oscillator and Timing						
f_{SW}	Switching frequency	Buck1/2/3		2.1		MHz
f_{FSS_RANGE}	Spread spectrum range	FSS_RANGE[0]=0		5		%
		FSS_RANGE[0]=1		10		%
f_{FSS}	Spread spectrum frequency	FSS_PERIOD[0]=0		4.5		kHz
		FSS_PERIOD[0]=1		9		kHz
t_{SS}	Soft start time	SS_TIME[0]=0		0.5		ms
		SS_TIME[0]=1		2		ms
t_{PG_DELAY}	PG rising delay time	PG_DLY[0]=0		3		ms
		PG_DLY[0]=1		10		ms
t_{Hiccup}	Hiccup time	HIC_TIME[0]=0		3		ms
		HIC_TIME[0]=1		10		ms
HV BUCK1						
V_{OUT1}	Output voltage configurable range		3.1		4	V
V_{OUT1_ACC}	Output voltage accuracy		-2		+2	%
R_{DSON_HS1}	High-side switch on-resistance	V_{CC}=5V		265		mΩ
R_{DSON_LS1}	Low-side switch on-resistance	V_{CC}=5V		155		mΩ
I_{LIM_HS1}	High-side switch peak current limit			1.8		A
I_{LIM_LSP1}	Low-side switch valley current limit			1.2		A
I_{LIM_LSN1}	Low-side reverse current limit			0.8		A
R_{DIS1}	Output discharge resistance	Output disabled		70		Ω
t_{ON_MIN1}(1)	Minimum on-time			60		ns
LV BUCK2						
V_{IN23}	Supply voltage range		3		4	V
V_{OUT2}	Output voltage configurable range		1.1		3.3	V
V_{OUT2_ACC}	Output voltage accuracy		-2		+2	%
R_{DSON_HS2}	High-side switch on-resistance			220		mΩ
R_{DSON_LS2}	Low-side switch on-resistance			120		mΩ
I_{LIM_HS2}	High-side switch peak current limit			2		A

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SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
I_{LIM_LSP2}	Low-side switch valley current limit			1.8		A
I_{LIM_LSN2}	Low-side reverse current limit			1.3		A
R_{DIS2}	Output discharge resistance	Output disabled		70		Ω
t_{ON_MIN2}(1)	Minimum on-time			60		ns
LV BUCK3						
V_{IN23}	Supply voltage range		3		4	V
V_{OUT3}	Output voltage configurable range		0.6		1.8	V
V_{OUT3_ACC}	Output voltage accuracy		-2		+2	%
R_{DSON_HS3}	High-side switch on-resistance			220		mΩ
R_{DSON_LS3}	Low-side switch on-resistance			120		mΩ
I_{LIM_HS3}	High-side switch peak current limit			2		A
I_{LIM_LSP3}	Low-side switch valley current limit			1.8		A
I_{LIM_LSN3}	Low-side reverse current limit			1.3		A
R_{DIS3}	Output discharge resistance	Output disabled		70		Ω
t_{ON_MIN3}(1)	Minimum on-time			60		ns
LDO4						
V_{LDO4}	Output voltage configurable range		2.7		3.3	V
V_{LDO4_ACC}	Output voltage accuracy		-2		+2	%
V_{LDO4_DROP}	Dropout voltage	V_{OUT1}=3.3V, V_{LDO4} set to 3.3V, I_{LDO4}=300mA		110		mV
L_{LINE_REG4}	Line Regulation	V_{OUT1}=3.1V to 4V, V_{LDO4} set to 2.8V, I_{LDO4}=100mA		0.01		%/V
L_{LOAD_REG4}	Load Regulation	V_{OUT1}=3.3V, V_{LDO4} set to 2.8V, I_{LDO4}=10mA to 300mA		0.2		%
I_{LIM_OCP4}	Over current limit	V_{OUT1}=3.3V, V_{LDO4} set to 2.8V		400		mA
PSRR(1)	Power supply rejection ratio	V_{OUT1}=3.3V, V_{LDO4}=2.8V, C_{LDO4}=4.7uF, I_{LDO4}=50mA, @ 1kHz		60		dB
		V_{OUT1}=3.3V, V_{LDO4}=2.8V, C_{LDO4}=4.7uF, I_{LDO4}=50mA, @ 10kHz		60		dB
		V_{OUT1}=3.3V, V_{LDO4}=2.8V, C_{LDO4}=4.7uF, I_{LDO4}=50mA, @ 100kHz		60		dB
		V_{OUT1}=3.3V, V_{LDO4}=2.8V, C_{LDO4}=4.7uF, I_{LDO4}=50mA, @ 1MHz		40		dB
N_{RMS}(1)	RMS noise	V_{OUT1}=3.3V, V_{LDO4}=2.8V, C_{LDO4}=4.7uF, I_{LDO4}=100mA, from 10Hz to 100kHz		30		μV_{RMS}
R_{DIS4}	Output discharge resistance	Output disabled		70		Ω

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SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
LDO5						
V_{IN5}	Supply voltage range		1		4	V
V_{LDO5}	Output voltage configurable range		0.8		3.3	V
V_{LDO5_ACC}	Output voltage accuracy		-2		+2	%
V_{LDO5_DROP}	Dropout voltage	V_{IN5}=1.8V, V_{LDO5} set to 1.8V, I_{LDO5}=300mA		140		mV
L_{LINE_REG5}	Line Regulation	V_{IN5}=1.3V to 4V, V_{LDO5} set to 1V, I_{LDO5}=100mA		0.01		%/V
L_{LOAD_REG5}	Load Regulation	V_{IN5}=1.8V, V_{LDO5} set to 1V, I_{LDO5}=10mA to 300mA		0.8		%
I_{LIM_OCP5}	Over current limit	V_{IN5}=1.8V, V_{LDO5} set to 1V		400		mA
R_{DIS5}	Output discharge resistance			70		Ω
Protection						
V_{OUT1_OVP}	Buck1 output over-voltage rising threshold	OV1[1:0]=00		105		%
		OV1[1:0]=01		110		%
		OV1[1:0]=10		115		%
		OV1[1:0]=11		120		%
V_{OUT1_UVP}	Buck1 output under-voltage falling threshold	UV1[1:0]=00		95		%
		UV1[1:0]=01		90		%
		UV1[1:0]=10		85		%
		UV1[1:0]=11		80		%
$V_{OUT2/3/4/5_OVP}$	Buck2/3/LDO4/5 output over-voltage rising threshold	OV2/3/4/5[1:0]=01		105		%
		OV2/3/4/5[1:0]=10		106		%
		OV2/3/4/5[1:0]=11		110		%
$V_{OUT2/3/4/5_UVP}$	Buck2/3/LDO4/5 output under-voltage falling threshold	UV2/3/4/5[1:0]=01		95		%
		UV2/3/4/5[1:0]=10		94		%
		UV2/3/4/5[1:0]=11		90		%
V_{IN_OVP}	Input over-voltage rising threshold			20		V
$V_{IN_OVP_HYS}$	Input over-voltage hysteresis			1		V
T_{SD}	Thermal shutdown rising threshold			170		°C
T_{SD_HYS}	Thermal shutdown hysteresis			20		°C
PG						
V_{OL_PG}	Open-drain output low level voltage	I_{SINK}=1mA			0.1	V
I_{LKG_PG}	Open-drain output high leakage current		-1		1	uA
I2C Interface(1)						
V_{IH}	High level input voltage		1.4			V
V_{IL}	Low level input voltage				0.4	V
V_{OL}	Low level output voltage	I_{SINK}=4mA			0.4	V

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SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency				1	MHz
t_{LOW}	Low period of the SCL clock		500			ns
t_{HIGH}	High period of the SCL clock		260			ns
t_{HD_STA}	Hold time (repeated) START condition		260			ns
t_{SU_STA}	Set-up time for a repeated START condition		260			ns
t_{HD_DAT}	Data hold time		0			ns
t_{SU_DAT}	Data set-up time		50			ns
t_{SU_STO}	Set-up time for STOP condition		260			ns
t_r	Rise time of both SCL and SDA signals				120	ns
t_f	Fall time of both SCL and SDA signals				120	ns
C_B	Capacitive load for each bus line				550	pF

(1) Guaranteed by sample characterization, not tested in production.

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TYPICAL CHARACTERISTICS

V_{IN} = 10V, V_{OUT1} = 3.3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{OUT4} = 2.8V, V_{OUT5} = 1V, L1 = 2.2uH, L2 = L3 = 1uH, T_A = 25°C, unless otherwise noted.

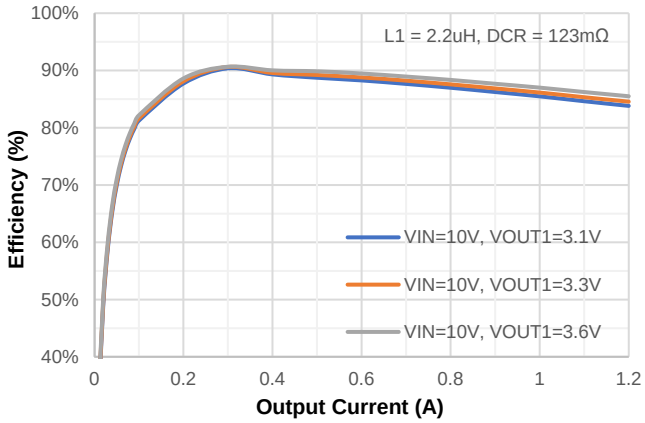


Figure 1. Buck1 Efficiency vs. Load Current

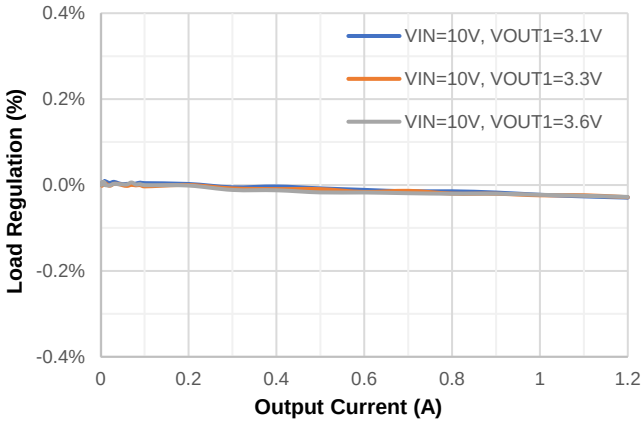


Figure 2. Buck1 Load Regulation

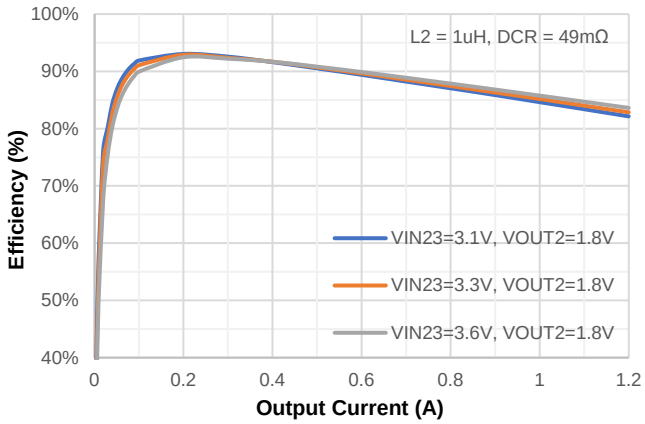


Figure 3. Buck2 Efficiency vs. Load Current

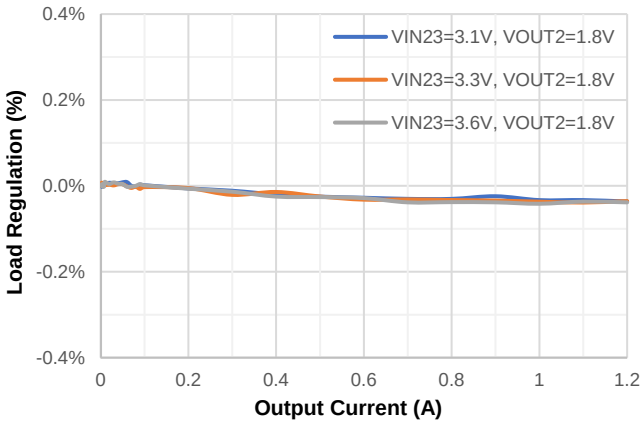


Figure 4. Buck2 Load Regulation

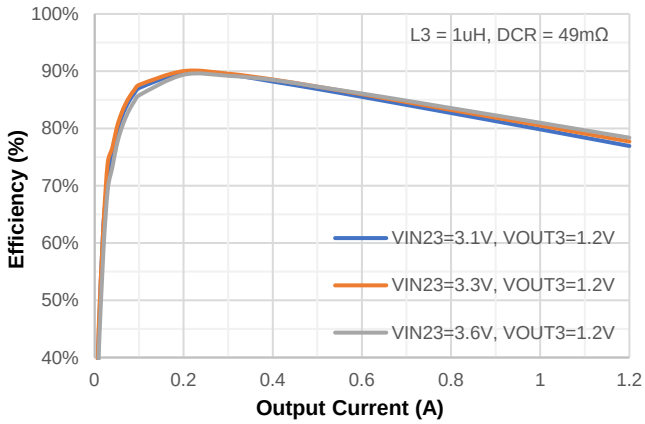


Figure 5. Buck3 Efficiency vs. Load Current

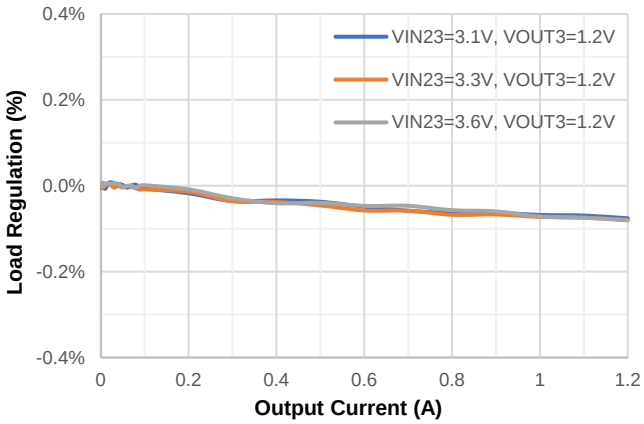


Figure 6. Buck3 Load Regulation

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TYPICAL CHARACTERISTICS (continued)

V_{IN} = 10V, V_{OUT1} = 3.3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{OUT4} = 2.8V, V_{OUT5} = 1V, L1 = 2.2uH, L2 = L3 = 1uH, T_A = 25°C, unless otherwise noted.

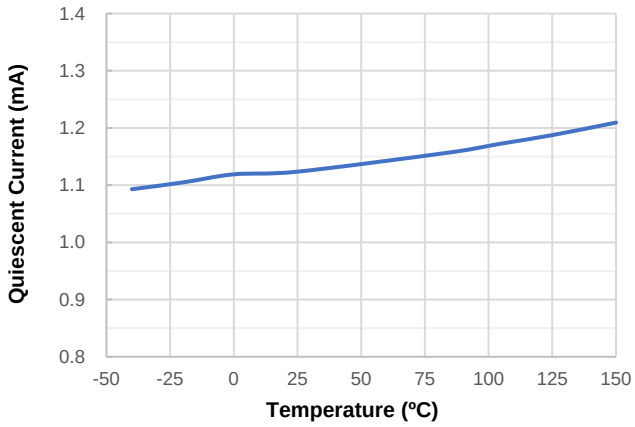


Figure 7. Quiescent Current (rails off) vs. Temperature

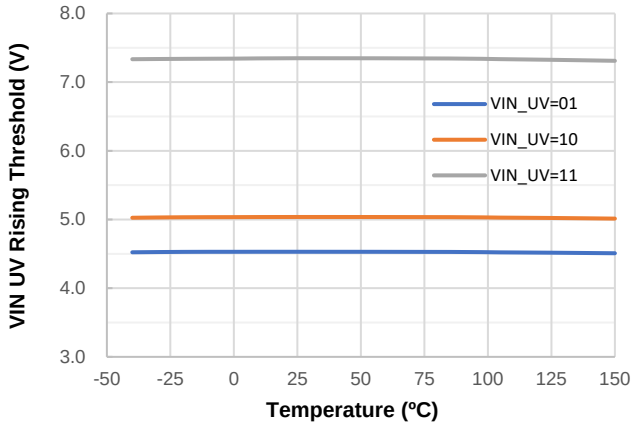


Figure 8. VIN UV Rising Threshold vs. Temperature

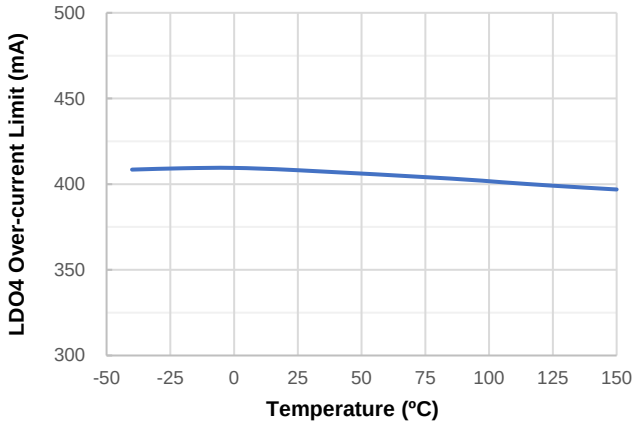


Figure 9. LDO4 Over-current Limit vs. Temperature

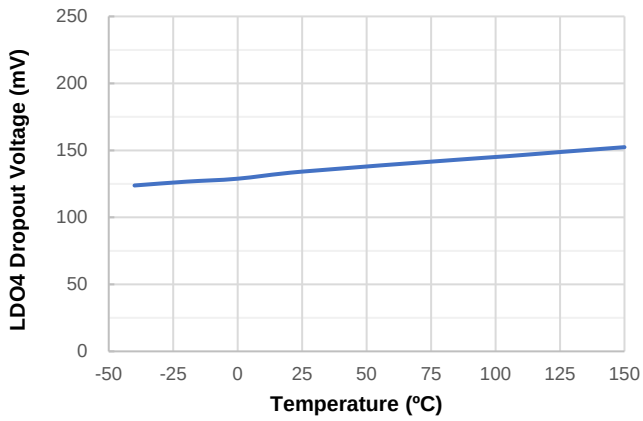


Figure 10. LDO4 Dropout Voltage vs. Temperature

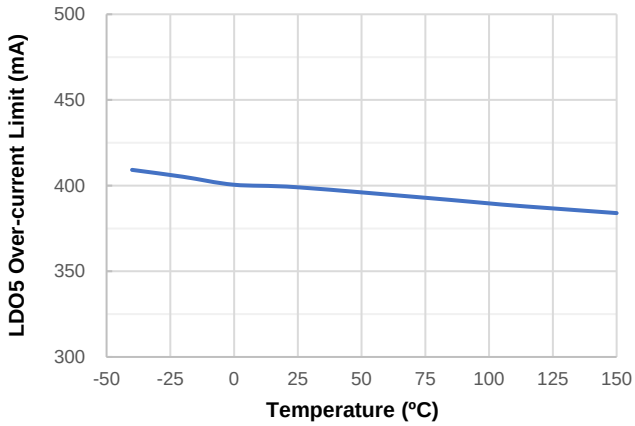


Figure 11. LDO5 Over-current Limit vs. Temperature

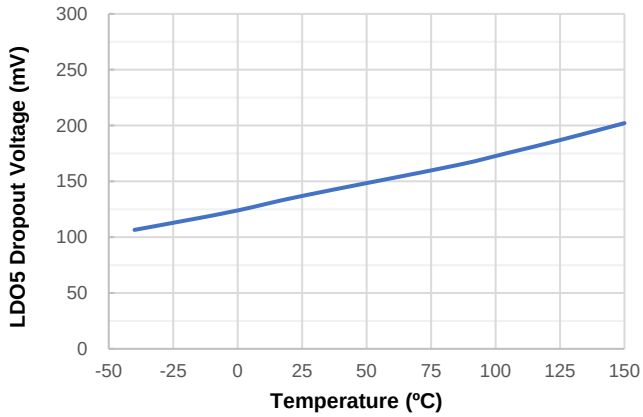


Figure 12. LDO5 Dropout Voltage vs. Temperature

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FUNCTIONAL BLOCK DIAGRAM

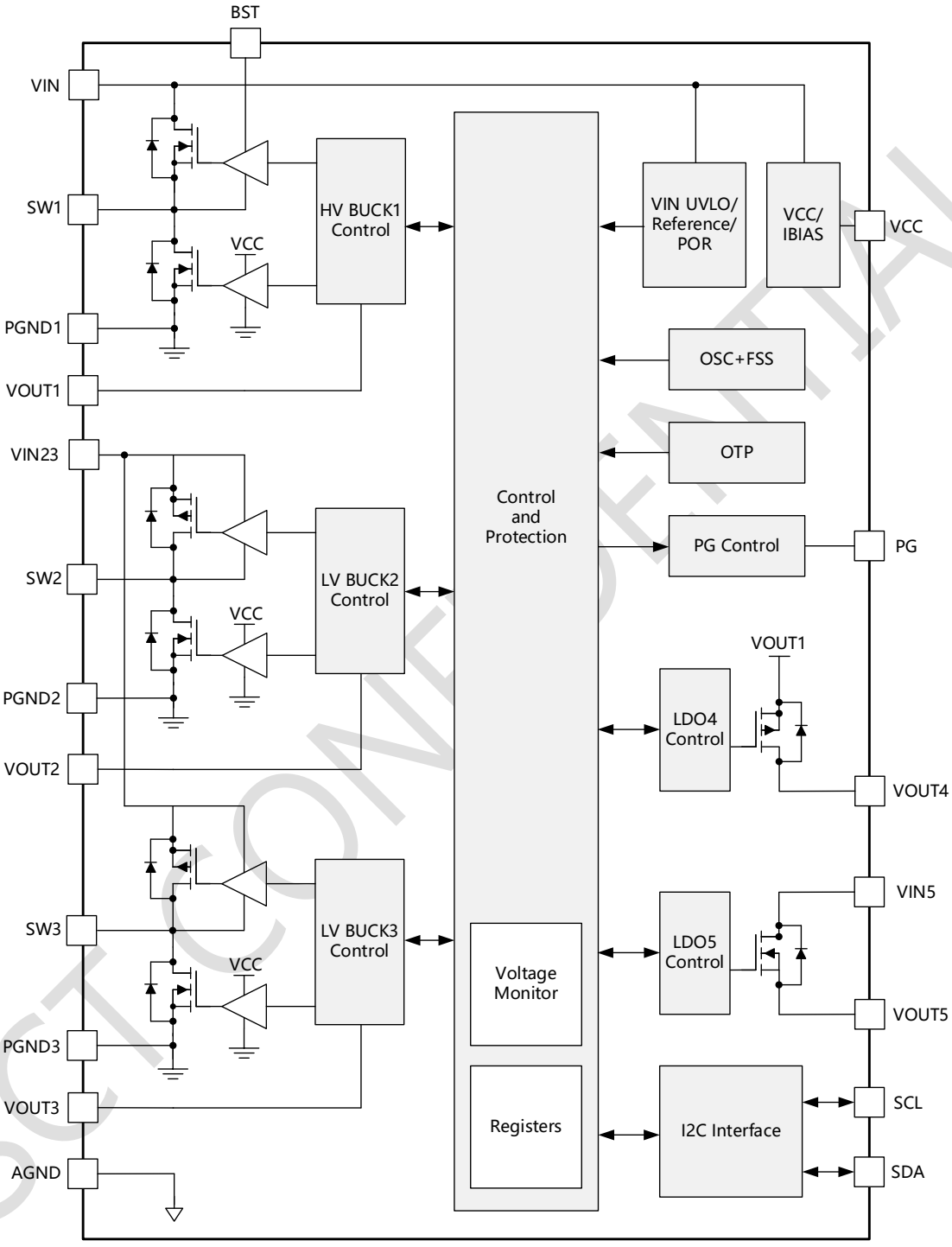


Figure 13. Functional Block Diagram

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OPERATION

Overview

The SCT61250Q is a highly integrated power management IC (PMIC) optimized for automotive camera system. It integrates three high-efficiency synchronous buck converters (HV Buck1, LV Buck2, LV Buck3), one high-PSRR low noise LDO (LDO4) and one general LDO (LDO5) with over-voltage/under-voltage monitoring on all outputs. The output voltage and power sequence of each channel are pre-programmed to achieve a flexible and minimized power solution.

Buck1 has an input voltage range from 4V to 19V for connections to Power over Coax (PoC). Buck2 and Buck3 are two second stage converters and generally powered from the output of Buck1. All three buck converters can provide a continuous output current of up to 1.2A and operate in Forced-CCM (Forced Continuous Conduction Mode) with 2.1MHz switching frequency and optional Frequency Spread Spectrum (FSS) for EMI mitigation.

LDO4 is a high PSRR, low noise LDO designed for analog power rail. LDO5 is a general LDO with a separate voltage input pin for flexible configuration. Both LDO4 and LDO5 can provide a continuous output current of up to 300mA.

The SCT61250Q integrates full protection features including programmable input under-voltage protection, input over-voltage protection, output over-voltage/under-voltage protection, over-current protection and thermal shutdown.

Operating State Machine

The operation state machine of SCT61250Q is shown in Figure 14. The power rail action and system function in each state are listed in Table 1.

Table 1. PMIC Operation in Each State

<table>
<tr><th rowspan="2">State</th><th colspan="5">Power Rail</th><th colspan="4">Function</th></tr>
<tr><th>Buck1</th><th>Buck2</th><th>Buck3</th><th>LDO4</th><th>LDO5</th><th>PG</th><th>I2C</th><th>TSD</th><th>Register</th></tr>
<tr><td>IDLE</td><td rowspan="3">OFF</td><td rowspan="3">OFF</td><td rowspan="3">OFF</td><td rowspan="3">OFF</td><td rowspan="3">OFF</td><td>Hi-Z</td><td rowspan="2">OFF</td><td rowspan="2">OFF</td><td>Reset</td></tr>
<tr><td>LOADOTP</td><td rowspan="2">Low</td><td rowspan="3">\</td></tr>
<tr><td>DEEPSAFE</td><td rowspan="2">ON</td><td rowspan="2">ON</td></tr>
<tr><td>POWERUP</td><td rowspan="2">ON</td><td rowspan="2">ON</td><td rowspan="2">ON</td><td rowspan="2">ON</td><td rowspan="2">ON</td></tr>
<tr><td>NORMAL</td><td>High</td></tr>
</table>

IDLE State

The device enters IDLE state whenever VCC is below VCC UV threshold. All functional blocks are disabled and all registers are reset. VCC is powered from VIN through internal linear regulator after power-on. The device will exit IDLE state and transit to LOADOTP state when VCC reaches its UV rising threshold.

LOADOTP State

Once the device enters LOADOTP state, OTP data will be loaded into corresponding registers. After OTP loaded, DEEPSAFE state will be entered.

DEEPSAFE State

In DEEPSAFE state, all channels are off and PG pin is low. The device is held and waits for all conditions met to power up. To exit DEEPSAFE state, VIN should be higher than V_{IN_UV} threshold and no other critical fault like thermal shutdown is triggered. For a normal power-on, the device will transit to POWERUP state almost immediately if all conditions are met when entering DEEPSAFE state.

The device would also enter DEEPSAFE state when any of the deep safe events shown in Table 2 occurs after startup. After a deep safe event triggered, all power rails are shut down immediately and simultaneously while I2C interface keeps alive, allowing user to communicate with the device and read the status registers to locate the

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specific fault. The device will stay in DEEPSAFE state in latch mode, or transit to POWERUP state once the deep safe event discontinued and the hiccup timer expired in hiccup mode. The latch or hiccup mode could be selected in **PROT_MODE[0]**.

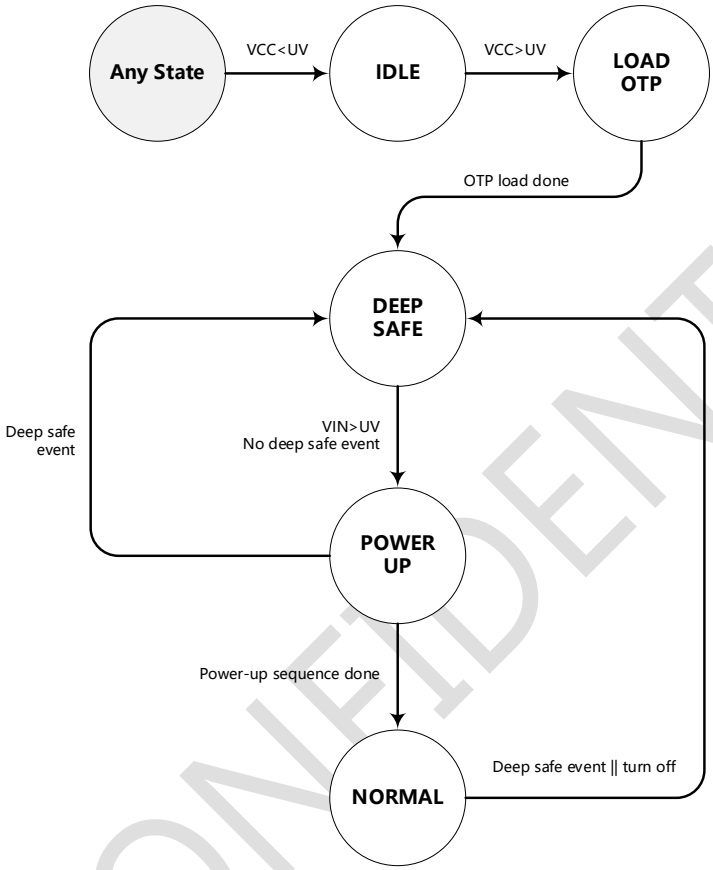


Figure 14. Operating State Machine and Transitions

POWERUP State

In POWERUP state, all power rails will be built up following the OTP-programmed sequence. HV Buck1 is always the first one to power up, and the other channels then will start up one-by-one according to the configuration in **SEQ[4:0]**. The soft-start time of each channel could be selected in **SS_TIME[0]**. If all channels finish soft-start within power good range, the PG rising delay timer starts and the duration is configured in **PG_DLY[0]**. Once the timer is expired, the device will enter NORMAL state and PG pin will be pulled high. See Figure 18 for a detailed power-on sequence. If any deep safe event occurs in POWERUP state, the device will transit to DEEPSAFE state directly.

NORMAL State

Normal state is the normal operation state of the device with all enabled channels on. PG pin is pulled high upon entering the state and all output rails are continuously monitored. When operating in NORMAL state, the device will transit to DEEPSAFE state once any deep safe event occurs.

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Table 2. Deep Safe Event

Deep Safe Event	Status Bit
Buck1 output is out of OV/UV range.	OV1[0], UV1[0]
Buck2 output is out of OV/UV range.	OV2[0], UV2[0]
Buck3 output is out of OV/UV range.	OV3[0], UV3[0]
LDO4 output is out of OV/UV range.	OV4[0], UV4[0]
LDO5 output is out of OV/UV range.	OV5[0], UV5[0]
VIN is below under-voltage threshold.	VIN_UV[0]
VIN is above over-voltage threshold.	VIN_OV[0]
VIN23 is above over-voltage threshold (typ. 5.4V).	VIN23_OV[0]
VIN5 is above over-voltage threshold (typ. 5.4V).	VIN5_OV[0]
VCC is above over-voltage threshold.	VCC_OV[0]
Thermal shutdown.	TSD[0]

High Efficiency Buck Converters

All three buck converters employ 2.1MHz fixed frequency peak current mode control. The forced continuous conduction mode realizes low output voltage ripple and good transient response at all load condition. The output voltage, power sequence, soft-start time and loop compensation are pre-programmed without any setting by external components, which makes the device easy to use by minimizing the off-chip component count.

For Buck1, an external 100nF bootstrap capacitor between BST and SW1 pin is required to power high-side power switch gate driver. The bootstrap capacitor is charged from an integrated regulator when high-side power switch is off and low-side power switch is on.

The buck converters have proprietary designed gate driver scheme to resist switching node ringing without sacrificing switch turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the switch hard switching.

Under-voltage/Over-voltage Protection

If any channel's output falls below the under-voltage protection threshold or exceeds the over-voltage protection threshold, all channels will shut off, and then keep off in latch mode or automatically restart in hiccup mode, which is set by **PROT_MODE[0]**. For latch mode, the device will only restart after a power recycle. For hiccup mode, the device will automatically restart with the programmed power sequence after a hiccup time set by **HIC_TIME[0]**. During the hiccup time, all channels' output will be discharged.

Over Current Protection

The three buck converters implement over current protection with cycle-by-cycle limit for both high-side switch peak current and also low-side switch valley current to avoid inductor current running away during unexpected overload or output hard short condition. When the high-side switch is on, the device monitors the increased inductor current through the relevant operating main power switch. Once the inductor current exceeds the peak current limit threshold, the high-side switch turns off immediately and the low-side switch turns on to conduct and decrease the inductor current. The high-side switch does not turn on again until the inductor current falls below the valley current limit threshold. When overload or hard short happens, the converter cannot provide enough output current to satisfy loading requirement though the inductor current has already been clamped at current limit, thus the output voltage drops and the output under-voltage protection would be triggered. Once output under-voltage protection triggered, the device will shut down all channels. The device will keep off until power recycle if in latch mode, or attempt to restart constantly until overload or hard short removed if in hiccup mode.

The two LDOs have internal current limit that protects the regulator during overload or output hard short condition.

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Once the current limit reached, the output voltage drops and the under-voltage protection would be triggered. The device then shuts down all channels and enters hiccup or latch protection mode according to the configuration. The latch mode would immediately protect the system from further failure while the hiccup mode could automatically restart the device once overload or hard short removed.

Thermal Shutdown

The thermal shutdown protects the device from damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 170°C, thermal shutdown will be triggered. The device will shut down all channels immediately and enter hiccup mode or latch mode according to the configuration. When the junction temperature falls below 150°C in hiccup mode, the device will restart with the programmed power sequence.

Status Bits

The SCT61250Q provides four status registers, STATUS1~4, to record all kinds of warnings, errors, or faults during operation. Once being set, these status bits will not be automatically reset until VCC under-voltage (e.g., VIN power off). To clear these status bits manually, write '1' to corresponding status bit via I2C.

Frequency Spread Spectrum

To meet CISPR and automotive EMI compliances, the SCT61250Q implements Frequency Spread Spectrum (FSS) function. The FSS circuitry shifts the 2.1MHz switching frequency of three buck converters within ±5/±10% range and 4.5/9kHz period, which are configured in **FSS_RANGE[0]** and **FSS_PERIOD[0]**. The FSS feature guarantees the switching frequency does not drop into 1.8MHz AM band limit.

Active Output Discharge

In order to discharge the residual voltage on the output capacitors, all channels have active discharge path from their output to ground. The discharge path will be activated whenever the channel is in off state.

Power Good

The PG pin goes logic high after all channels built up successfully with the programmed power sequence. There is a delay time between the last channel finishing soft-start and PG pin pulled high, programmed by **PG_DLY[0]**. When any deep safe event (listed in Table 2) triggered during normal operation, the PG pin will assert low at once, along with all channels shut down. The device will then enter either hiccup mode or latch mode according to the configuration.

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I2C Interface

The SCT61250Q integrates a two-wire serial interface for bidirectional communications between the device and the master through the bus. The I2C protocol defines two bus lines, the serial data line (SDA) and the serial clock line (SCL). The device is assigned with a unique chip address 0x38 by default and operates as a slave. The master drives the SCL line and transfer bidirectional data through SDA line. Both the SCL and the SDA lines need a pull-up resistor connected to bus voltage since high state is the default state when bus is idle. The device supports Standard mode (up to 100kHz), Fast-mode (up to 400kHz) and Fast-mode Plus (up to 1MHz). The internal filtering ignores spikes and noises on the bus line to preserve data integrity. The maximum capacitive load for each bus line is given in Electrical Characteristic thus the number of Interfaces is limited.

Data Validity

The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low.

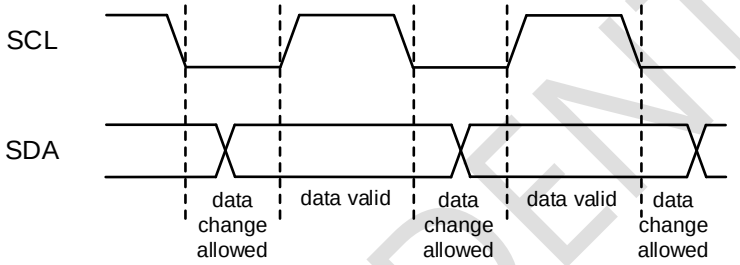


Figure 15. Data Validity Diagram

START and STOP Conditions

The data transfer always generates START and STOP conditions to announce the process. A high to low transition on the SDA line while SCL is high defines a START condition. A low to high transition on the SDA line while SCL is high defines a STOP condition. Both the START and STOP conditions are generated by the master on the bus.

The bus is considered to be busy after START condition and released after STOP condition. A repeated START condition during transmission is also valid and will be regarded as a new START condition.

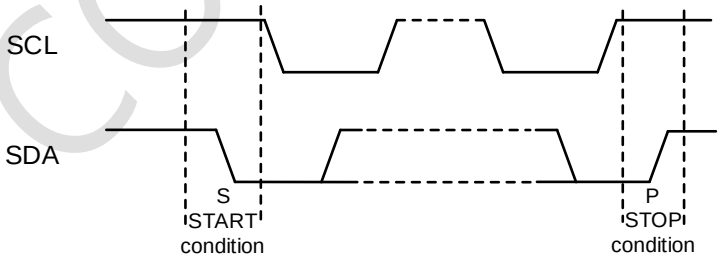


Figure 16. START and STOP Conditions Diagram

Data Transmission

The transferred byte consists of eight bits with the Most Significant Bit (MSB) first. After each byte is transferred, the master will release the SDA line and generate the ninth acknowledge clock pulse on SCL line. The device will pull the SDA line low during this acknowledge clock, to announce a successful reception and next byte may be sent. If the master is receiver and the last byte is received, it still generates the ninth acknowledge clock pulse but SDA line will not be pulled low. It's called not acknowledge signal and indicates the end of transmission.

After the START condition, the master must send a slave address as the first addressing byte. The slave address is seven bits long followed by an eighth R/W bit. The R/W bit defines the data direction. Set the R/W bit to 0 to indicate write command, and a 1 indicates read command.

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Packet Error Checking (PEC)

The SCT61250Q supports optional packet error checking (PEC) byte during the I2C communication. PEC can significantly increase fault coverage on the I2C interface. The PEC byte is implemented through CRC-8 polynomial of x8 + x2 + x +1. The PEC byte does not take ACK, NACK, START, STOP, Repeated START bits into calculation. The PEC byte is calculated with the register address and data byte over the entire message from the first START condition. Note that the slave address is not involved in the calculation both in write and read command. When PEC is enabled, the device will reject the write command if the master send an incorrect PEC byte. When in read mode with PEC enabled, the master should acknowledge the data byte thus then the device will send the PEC byte. PEC function can be enabled or disabled by **PEC_EN[0]**.

Write Data Format

A write to the device includes transmission of the following:

- START condition
- Slave address with the write bit set to 0
- 1 byte of data to register address
- 1 byte of data to the command register
- STOP condition

Read Data Format

A read from the device includes the following:

- Transmission of a START condition
- Slave address with the write bit set to 0
- 1 byte of data to register address
- Restart condition
- Slave address with read bit set to 1
- 1 byte of data to the command register
- STOP condition

Figure 17 illustrates the proper format for one frame.

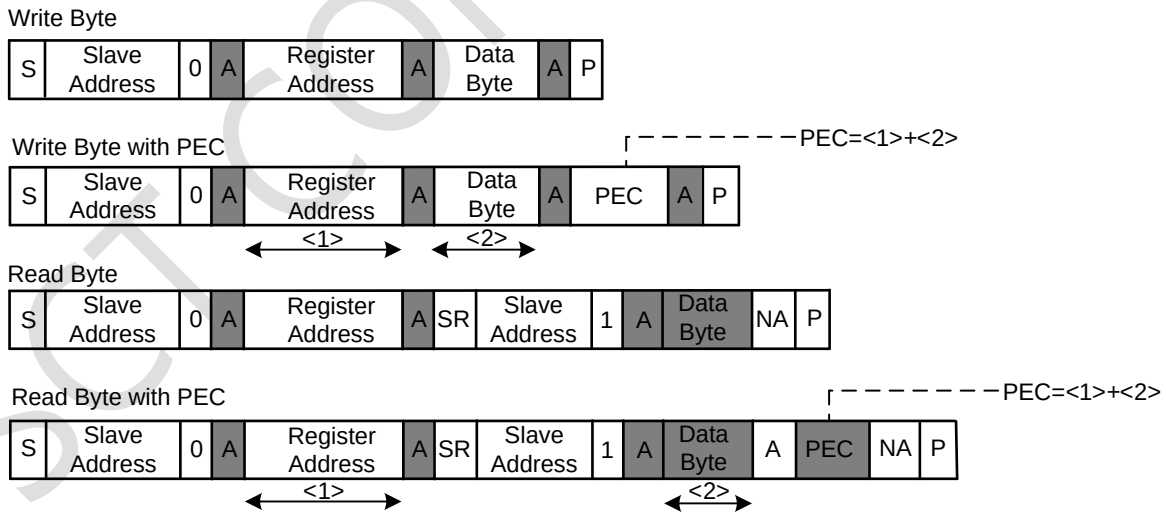


Figure 17. Transmission Data Format

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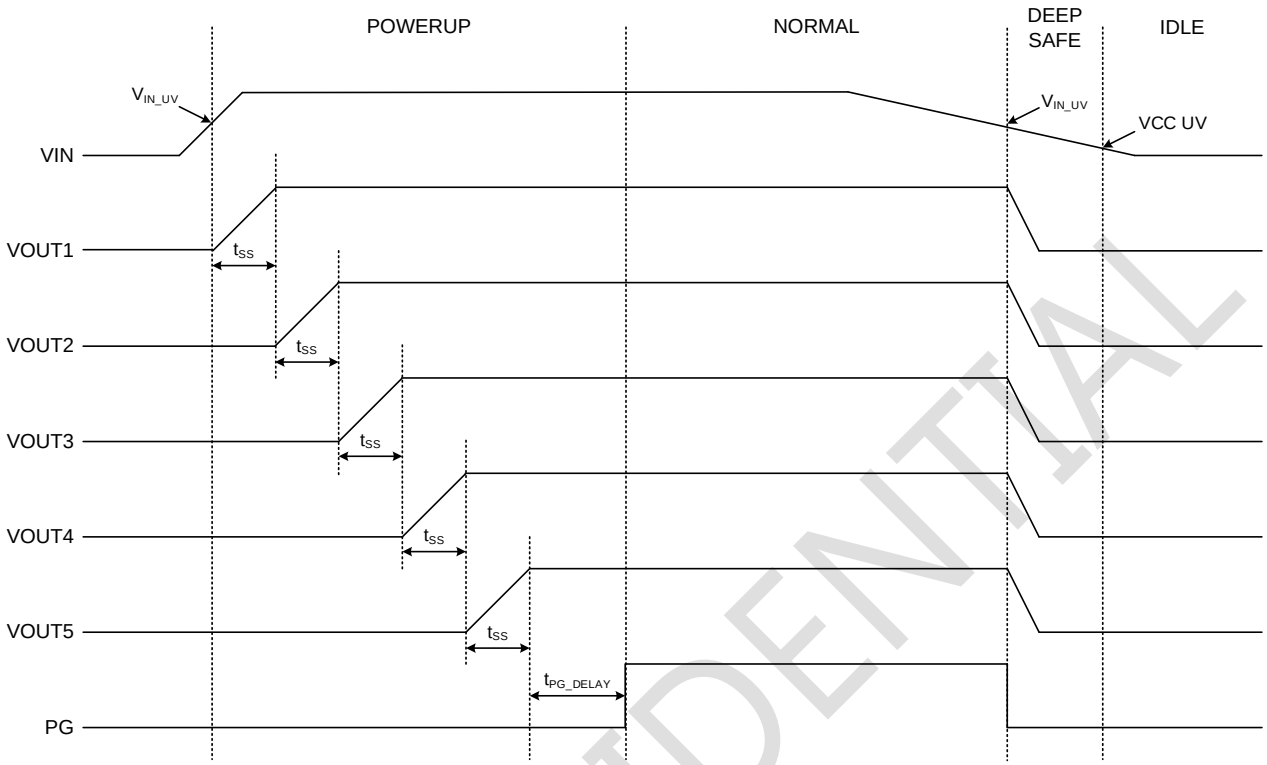


Figure 18. Power On/Off Sequence

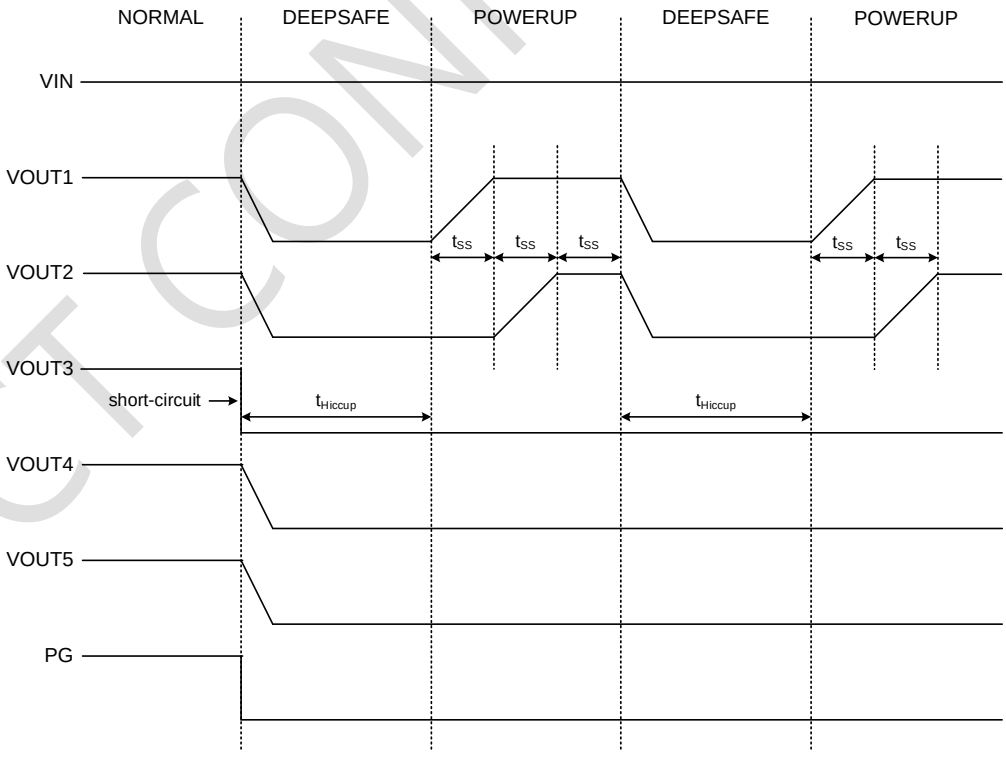


Figure 19. Deep Safe Event in Hiccup Mode

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APPLICATION INFORMATION

Typical Application

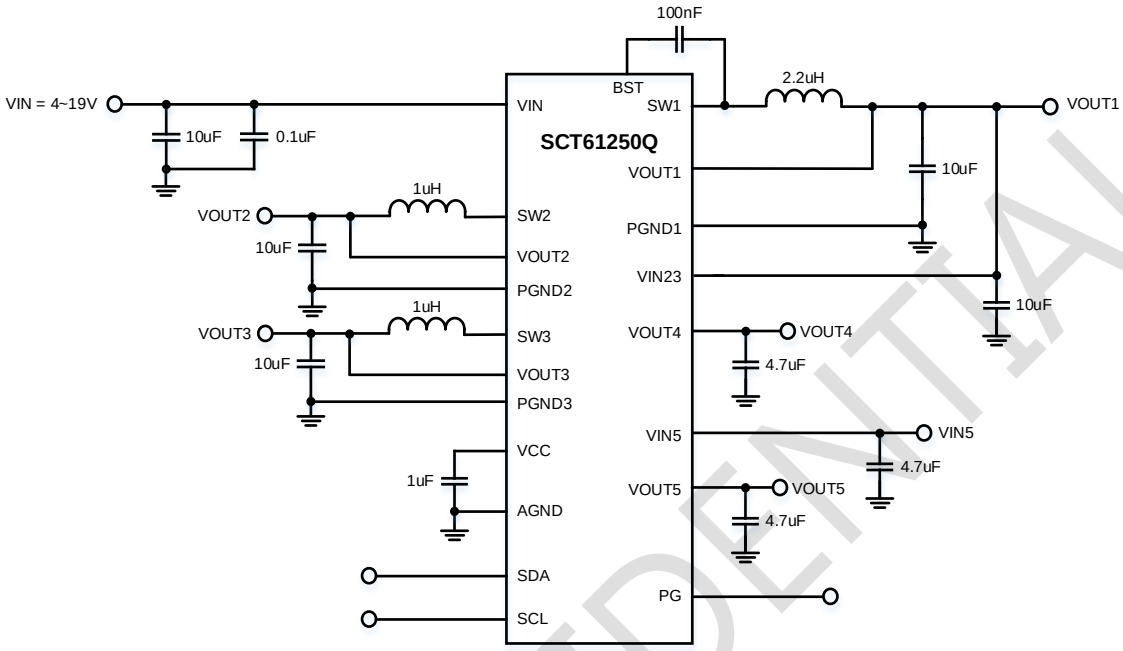


Figure 20. Application Schematics, 4V to 19V Input

Design Parameters	Example Value
Input Voltage	Nominal 10V
Output Voltage	Buck1: 3.3V Buck2: 1.8V Buck3: 1.2V LDO4: 2.8V LDO5: 1V
Maximum Output Current	Buck1: 1.2A Buck2: 1.2A Buck3: 1.2A LDO4: 300mA LDO5: 300mA
Switching Frequency	2.1MHz
Output Voltage Ripple (Peak-to-Peak)	Buck1: <10mV Buck2: <5mV Buck3: <5mV

The SCT61250Q is featured with minimized external components and any feedback divider or configuration resistor could be saved. For typical application, the recommended inductance and capacitance for each power rail are listed in Table 3. Higher inductance and capacitance for lower output ripple are also acceptable.

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Table 3. Recommended BOM for Typical Application

Power Rail	Switching Frequency	Inductor	Output Capacitor
Buck1	2.1MHz	2.2uH	10uF
Buck2	2.1MHz	1uH	10uF
Buck3	2.1MHz	1uH	10uF (V_{OUT3} > 1V) 20uF (V_{OUT3} ≤ 1V)
LDO4	-	-	4.7uF
LDO5	-	-	4.7uF

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Application Waveforms

V_{IN} = 10V, V_{OUT1} = 3.3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{OUT4} = 2.8V, V_{OUT5} = 1V, L1 = 2.2uH, L2 = L3 = 1uH, T_A = 25°C, unless otherwise noted.

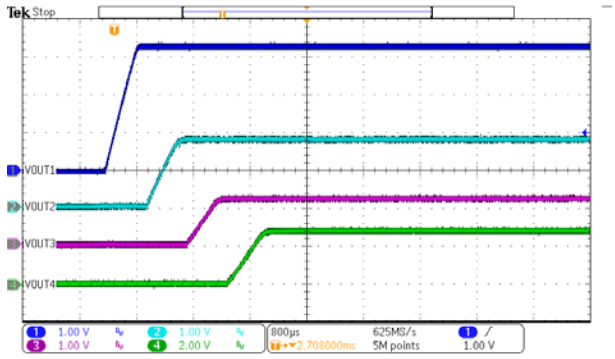


Figure 21. Power On Sequence I

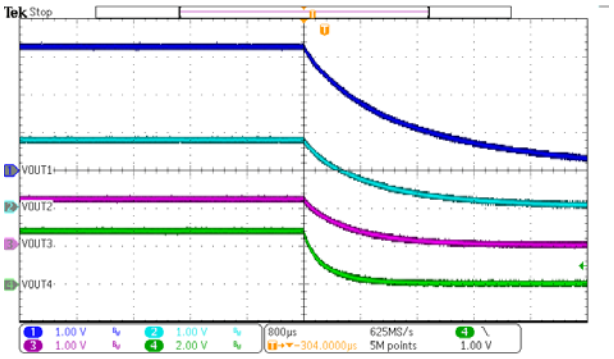


Figure 22. Power Off Sequence I

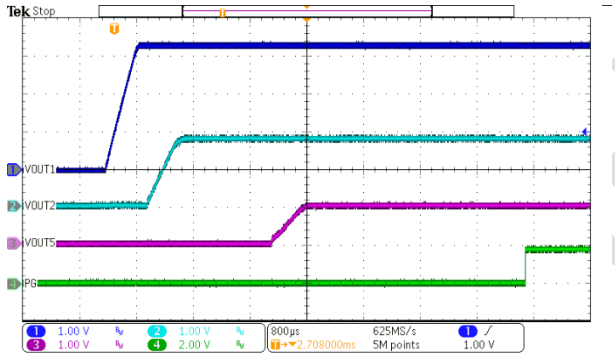


Figure 23. Power On Sequence II

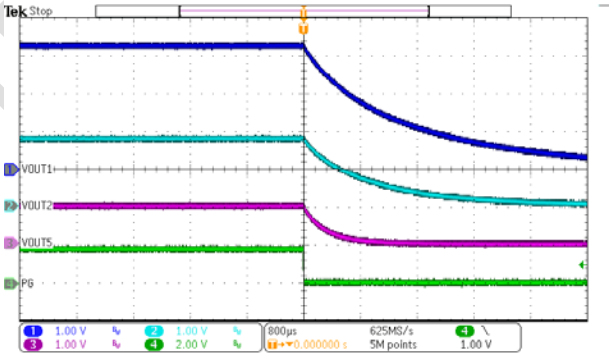


Figure 24. Power Off Sequence II

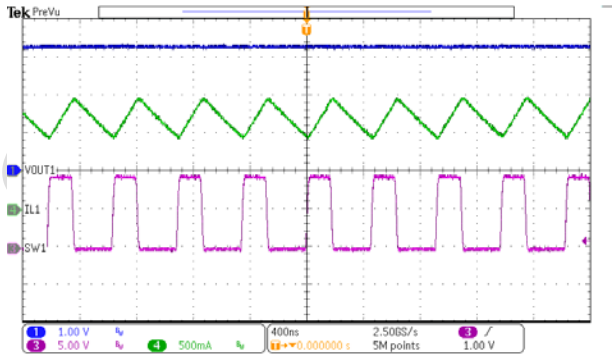


Figure 25. Buck1 Steady State, Load=1.2A

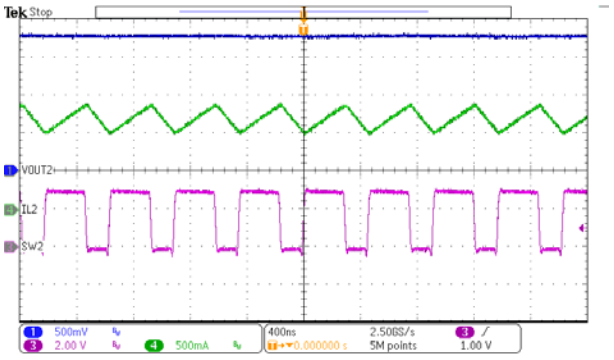


Figure 26. Buck2 Steady State, Load=1.2A

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Application Waveforms (continued)

V_{IN} = 10V, V_{OUT1} = 3.3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{OUT4} = 2.8V, V_{OUT5} = 1V, L1 = 2.2uH, L2 = L3 = 1uH, T_A = 25°C, unless otherwise noted.

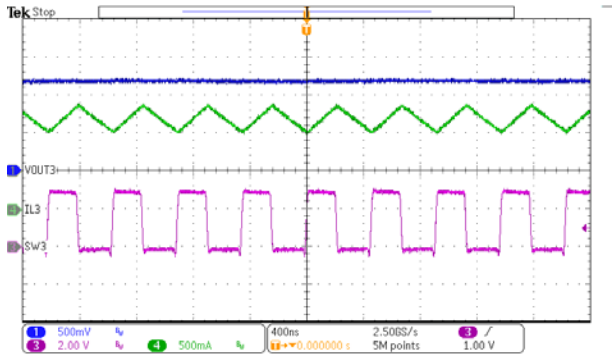


Figure 27. Buck3 Steady State, Load=1.2A

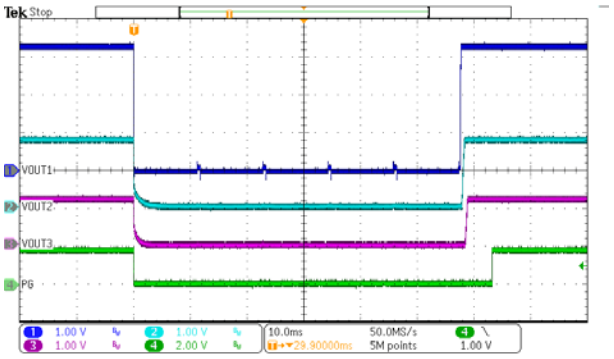


Figure 28. Buck1 Short-circuit and Recovery

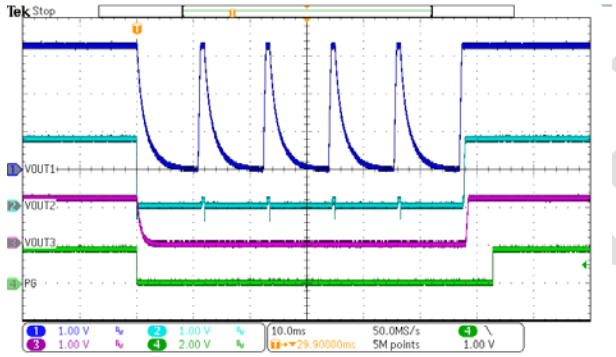


Figure 29. Buck2 Short-circuit and Recovery

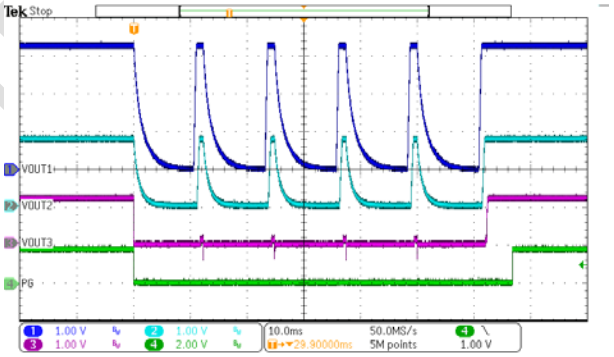


Figure 30. Buck3 Short-circuit and Recovery

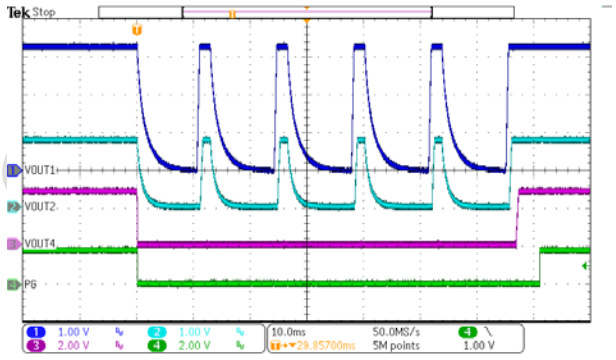


Figure 31. LDO4 Short-circuit and Recovery

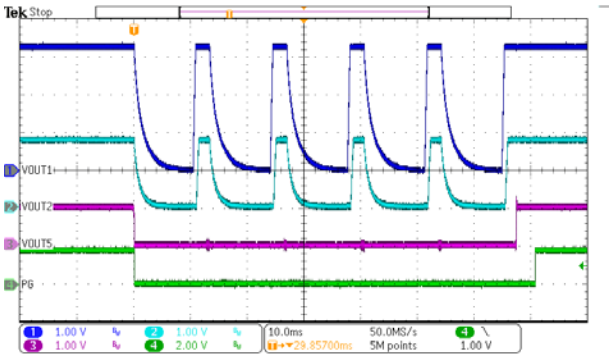


Figure 32. LDO5 Short-circuit and Recovery

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Layout Guideline

Proper PCB layout is critical for device's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The rule of thumb is to make ground trace lowest impedance and power is distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over-heat area.
2. Place a low ESR ceramic capacitor as close to VIN, VIN23 and VIN5 pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impedance of grounding.
4. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias.
5. Output inductor should be placed close to the SW pin. The switching area of the PCB conductor should be minimized to prevent excessive capacitive coupling.
6. Connect AGND to PGND plane at a single point.

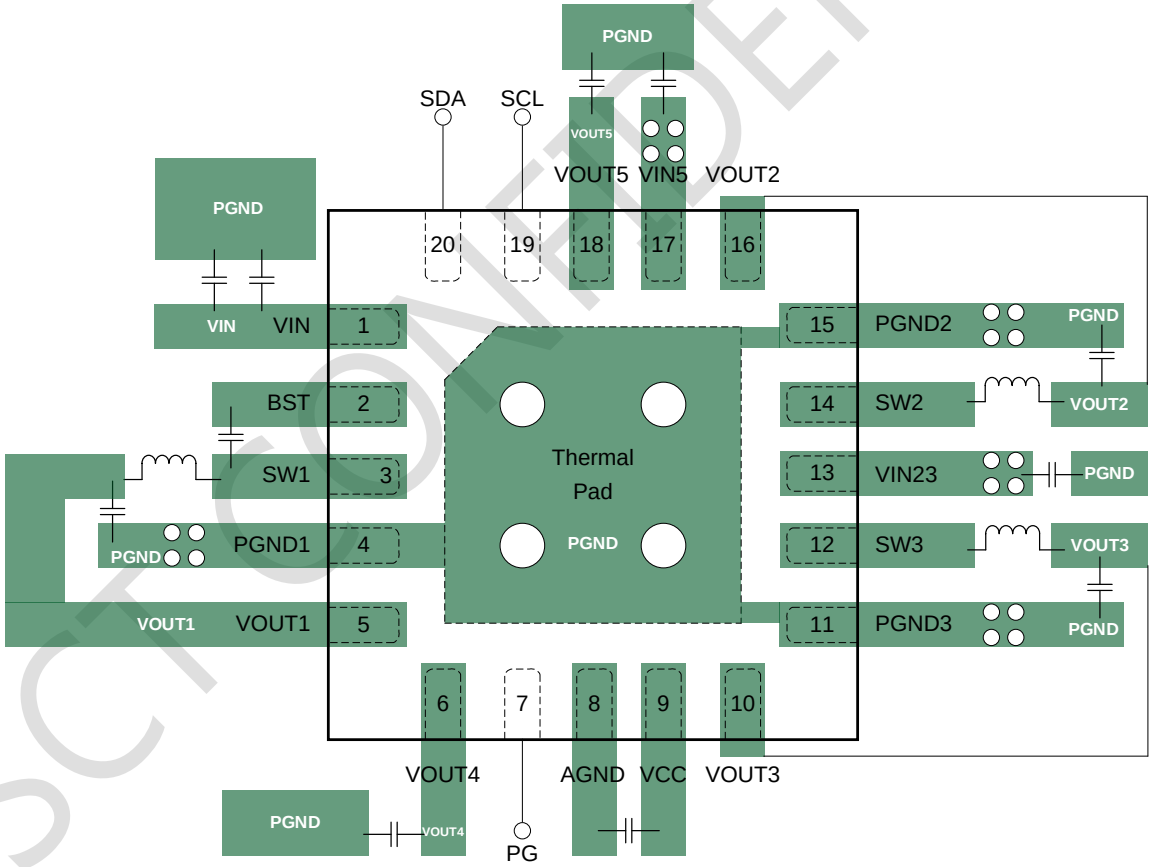


Figure 33. PCB Layout Example

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REGISTER MAP

ADDRESS	REGISTER	DEFAULT VALUE	OTP ACCESS	I2C WRITE LOCK
0x00	CHIPID	-	Y	-
0x01	CTRL_EN	-	Y	Y
0x02	CONFIG_SYS1	-	Y	Y
0x03	CONFIG_SYS2	-	Y	Y
0x04	CONFIG_SYS3	-	Y	Y
0x05	CONFIG_SYS4	-	Y	Y
0x06	CONFIG_VO145	-	Y	-
0x07	CONFIG_VO23	-	Y	-
0x08	CONFIG_SEQ	-	Y	Y
0x09	STATUS1	-	N	N
0x0A	STATUS2	-	N	N
0x0B	STATUS3	-	N	N
0x0C	STATUS4	-	N	N
0x1F	STATE	-	N	N
0x3F	I2C_LOCK	-	N	N

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REGISTER DESCRIPTION

CHIPID [7:0]			
ADDRESS: 0x00			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:0]	CONFIG_ID	R	Chip Configuration Identification. This is a unique number identifying the factory configuration of the device. This helps identify/verify the configuration without having to look at all configuration registers.

CTRL_EN [7:0]			
ADDRESS: 0x01			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	PEC_EN	W/R	Packet Error Checking Enable. Set this bit to 1 to enable PEC or 0 to disable PEC. 0: Disabled 1: Enabled
[6]	HIC_TIME	W/R	Hiccup time selection for hiccup mode. After any protection triggered, the device will keep all channels off for at least this hiccup time and then start a new power-up sequence. 0: 3ms 1: 10ms
[5]	PROT_MODE	W/R	Protection mode selection. 0: Hiccup Mode 1: Latch Mode
[4]	EN5	W/R	Enable for LDO5. 0: Disabled 1: Enabled
[3]	EN4	W/R	Enable for LDO4. 0: Disabled 1: Enabled
[2]	EN3	W/R	Enable for LV Buck3. 0: Disabled 1: Enabled
[1]	EN2	W/R	Enable for LV Buck2. 0: Disabled 1: Enabled
[0]	EN_ALL	W/R	Enable for all channels. 0: Disabled 1: Enabled

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CONFIG_SYS1 [7:0]			
ADDRESS: 0x02			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	FSS_PERIOD	W/R	Frequency spread spectrum period. 0: 4.5kHz 1: 9kHz
[6]	FSS_RANGE	W/R	Frequency spread spectrum range. 0: ±5% 1: ±10%
[5]	FSS_EN	W/R	Enable for frequency spread spectrum. 0: Disabled 1: Enabled
[4]	RESERVED	R	/
[3:2]	OVUV_DEG	W/R	OV rising/UV falling deglitch time for all output monitors. 00: 40us 01: 80us 10: 120us 11: 160us
[1:0]	VIN_UV	W/R	VIN under-voltage lockout threshold selection. 00: Reserved 01: Rising=4.5V / Falling=4V 10: Rising=5.0V / Falling=4.5V 11: Rising=7.3V / Falling=6.8V

CONFIG_SYS2 [7:0]			
ADDRESS: 0x03			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:6]	OV5	W/R	LDO5 output over-voltage threshold selection. 00: Reserved 01: 105% 10: 106% 11: 110%
[5:4]	OV4	W/R	LDO4 output over-voltage threshold selection. 00: Reserved 01: 105% 10: 106% 11: 110%
[3:2]	OV3	W/R	Buck3 output over-voltage threshold selection. 00: Reserved 01: 105% 10: 106% 11: 110%
[1:0]	OV2	W/R	Buck2 output over-voltage threshold selection. 00: Reserved 01: 105% 10: 106% 11: 110%

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CONFIG_SYS3 [7:0]			
ADDRESS: 0x04			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:6]	OV1	W/R	Buck1 output over-voltage threshold selection. 00: 105% 01: 110% 10: 115% 11: 120%
[5:4]	UV5	W/R	LDO5 output under-voltage threshold selection. 00: Reserved 01: 95% 10: 94% 11: 90%
[3:2]	UV4	W/R	LDO4 output under-voltage threshold selection. 00: Reserved 01: 95% 10: 94% 11: 90%
[1:0]	UV3	W/R	Buck3 output under-voltage threshold selection. 00: Reserved 01: 95% 10: 94% 11: 90%

CONFIG_SYS4 [7:0]			
ADDRESS: 0x05			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:6]	UV2	W/R	Buck2 output under-voltage threshold selection. 00: Reserved 01: 95% 10: 94% 11: 90%
[5:4]	UV1	W/R	Buck1 output under-voltage threshold selection. 00: 95% 01: 90% 10: 85% 11: 80%
[3:0]	RESERVED	R	/

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CONFIG_VO145 [7:0]			
ADDRESS: 0x06			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:5]	VOUT1	R	Buck1 output voltage setting. 000: 3.1V 001: 3.2V 010: 3.3V 011: 3.4V 100: 3.5V 101: 3.6V 110: 4V 111: Reserved
[4:3]	VOUT4	R	LDO4 output voltage setting. 00: 2.7V 01: 2.8V 10: 2.9V 11: 3.3V
[2:0]	VOUT5	R	LDO5 output voltage setting. 000: 0.8V 001: 0.85V 010: 0.9V 011: 1V 100: 1.1V 101: 1.2V 110: 1.8V 111: 3.3V

CONFIG_VO23 [7:0]			
ADDRESS: 0x07			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:4]	VOUT2	R	Buck2 output voltage setting. 0000: 1.1V 0001: 1.15V 0010: 1.2V … 1101: 1.75V 1110: 1.8V (50mV step from 1.1V to 1.8V, V_{OUT2} = 1.1V + VOUT2[3:0] × 0.05V) 1111: 3.3V
[3:0]	VOUT3	R	Buck3 output voltage setting. 0000: 0.6V 0001: 0.65V 0010: 0.7V … 1101: 1.25V 1110: 1.3V (50mV step from 0.6V to 1.3V, V_{OUT3} = 0.6V + VOUT3[3:0] × 0.05V) 1111: 1.8V

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CONFIG_SEQ [7:0]			
ADDRESS: 0x08			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:3]	SEQ	W/R	Power-up sequence configuration. Buck1 is always the first to power up. The other four channels could be powered up one by one with any sequence. There are 24 kinds of settings in total. 00000: Buck2, Buck3, LDO4, LDO5 00001: Buck2, Buck3, LDO5, LDO4 00010: Buck2, LDO4, Buck3, LDO5 00011: Buck2, LDO4, LDO5, Buck3 00100: Buck2, LDO5, Buck3, LDO4 00101: Buck2, LDO5, LDO4, Buck3 01000: Buck3, Buck2, LDO4, LDO5 01001: Buck3, Buck2, LDO5, LDO4 01010: Buck3, LDO4, Buck2, LDO5 01011: Buck3, LDO4, LDO5, Buck2 01100: Buck3, LDO5, Buck2, LDO4 01101: Buck3, LDO5, LDO4, Buck2 10000: LDO4, Buck2, Buck3, LDO5 10001: LDO4, Buck2, LDO5, Buck3 10010: LDO4, Buck3, Buck2, LDO5 10011: LDO4, Buck3, LDO5, Buck2 10100: LDO4, LDO5, Buck2, Buck3 10101: LDO4, LDO5, Buck3, Buck2 11000: LDO5, Buck2, Buck3, LDO4 11001: LDO5, Buck2, LDO4, Buck3 11010: LDO5, Buck3, Buck2, LDO4 11011: LDO5, Buck3, LDO4, Buck2 11100: LDO5, LDO4, Buck2, Buck3 11101: LDO5, LDO4, Buck3, Buck2 Others: RESERVED.
[2]	SS_TIME	W/R	Soft-start time of all channels. 0: 0.5ms 1: 2ms
[1]	PG_DLY	W/R	PG rising delay time after all channels finish soft-start. 0: 3ms 1: 10ms
[0]	RESERVED	R	/

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STATUS1 [7:0]			
ADDRESS: 0x09			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	UV5	W1C/R	LDO5 output under-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[6]	UV4	W1C/R	LDO4 output under-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[5]	UV3	W1C/R	Buck3 output under-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[4]	UV2	W1C/R	Buck2 output under-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[3]	UV1	W1C/R	Buck1 output under-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[2]	OV5	W1C/R	LDO5 output over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[1]	OV4	W1C/R	LDO4 output over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[0]	OV3	W1C/R	Buck3 output over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.

STATUS2 [7:0]			
ADDRESS: 0x0A			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	OV2	W1C/R	Buck2 output over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[6]	OV1	W1C/R	Buck1 output over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[5:0]	RESERVED	R	/

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STATUS3 [7:0]			
ADDRESS: 0x0B			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:6]	RESERVED	R	/
[5]	VIN_OV	W1C/R	VIN over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[4]	VIN23_OV	W1C/R	VIN23 over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[3]	VIN5_OV	W1C/R	VIN5 over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[2]	VCC_OV	W1C/R	VCC over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[1]	TSD	W1C/R	Thermal shutdown status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[0]	I2C_PEC_ERR	W1C/R	I2C PEC error status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.

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STATUS4 [7:0]			
ADDRESS: 0x0C			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:2]	RESERVED	R	/
[1]	VIN_UV	W1C/ R	VIN under-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[0]	RESERVED	R	/

STATE [7:0]			
ADDRESS: 0x1F			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:3]	RESERVED	R	/
[2:0]	SYS_STATE	R	System state machine real-time status. 000: IDLE 001: LOADOTP 100: DEEPSAFE 101: NORMAL 111: POWERUP Others: Reserved

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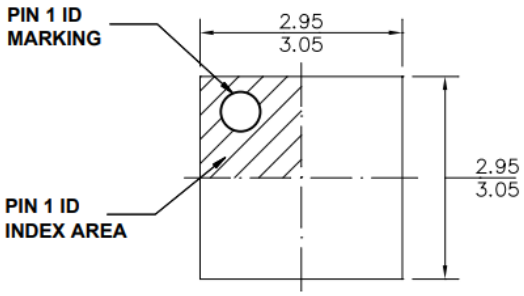
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I2C_LOCK [7:0]			
ADDRESS: 0x3F			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:1]	RESERVED	R	/
[0]	I2C_LOCK	W/R	Write “1” to this bit to unlock I2C write operation for registers under protection (see Register Map), or “0” to lock it off. 0: I2C write operation is invalid. 1: I2C write operation is valid.

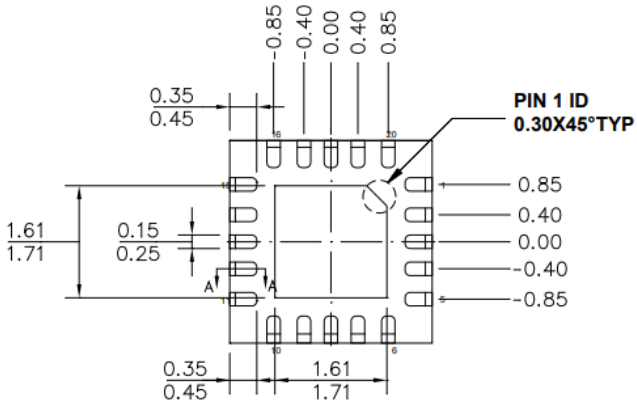
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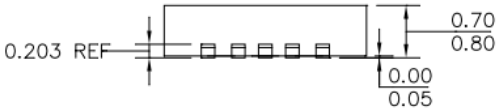
PACKAGE INFORMATION



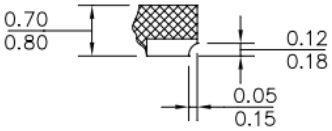
TOP VIEW



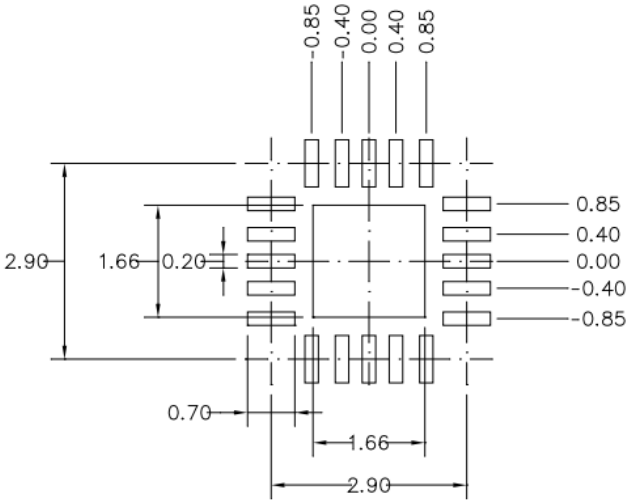
BOTTOM VIEW



SIDE VIEW



SECTION A-A



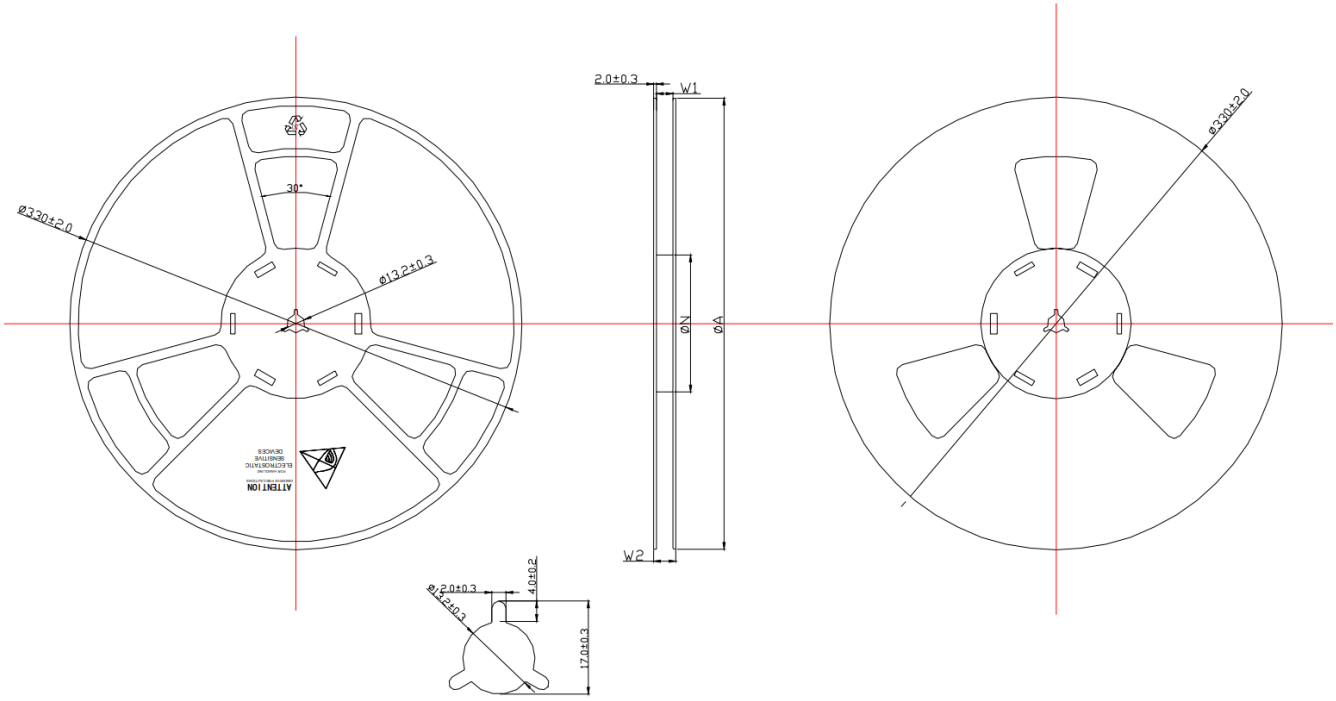
RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) DRAWING CONFIRMS TO JEDEC MO-220.
6) DRAWING IS NOT TO SCALE.

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TAPE AND REEL INFORMATION

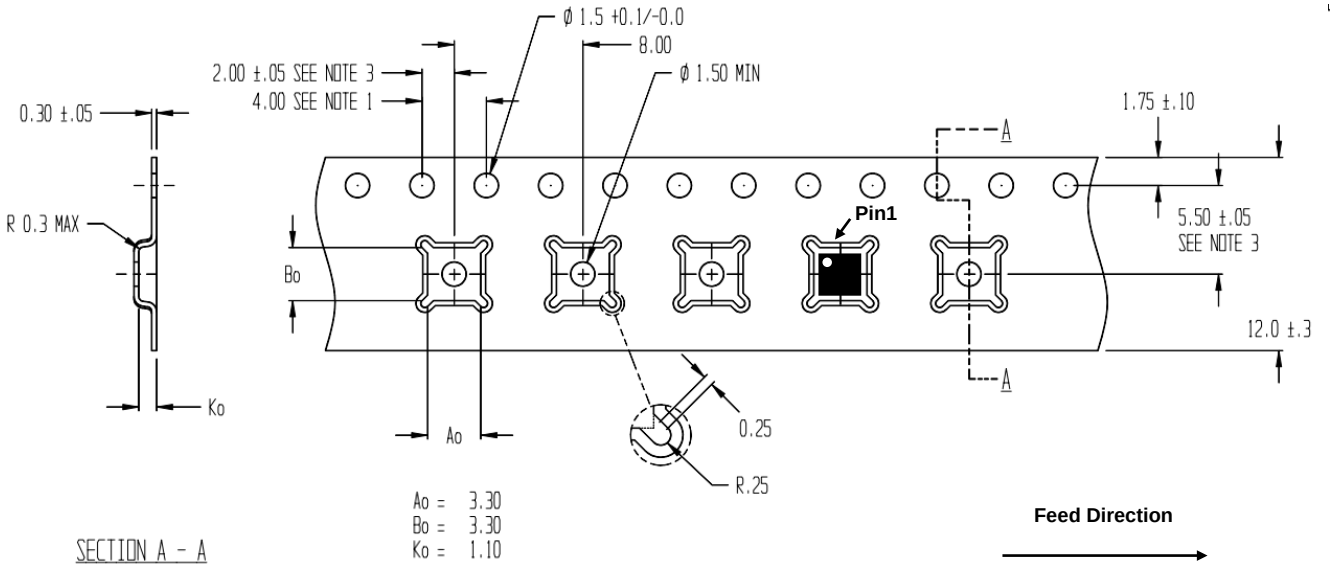


PRODUCT SPECIFICATIONS				
TYPE WIDTH	ØA	ØN	W1 (Min)	W2 (Max)
12MM	330±2.0	100±1.0	12.4	19.4
16mm	330±2.0	100±1.0	16.4	23.4
24MM	330±2.0	100±1.0	24.4	31.4
32MM	330±2.0	100±1.0	32.4	39.4
44MM	330±2.0	100±1.0	44.4	51.4

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TAPE AND REEL INFORMATION (continued)



NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

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