17V Vin, 3A Synchronous Step-down DCDC Converter

FEATURES

- Wide Input Voltage: 4.2V-17V
- 3A Continuous Output Current with Integrated 50mΩ /24mΩ FETs
- Wide Output Voltage Range:0.8V-7V
- Quiescent Current 220μA
- Cycle-by-Cycle Current Limiting
- Internal 3ms Soft-Start Limits the inrush current
- Fixed 800kHz Switching Frequency
- Input Under-Voltage Lockout
- Power save mode at light load
- Over-Temperature Protection
- Available in a SOT563 and SOT23-6L Package

APPLICATIONS

- Flat Panel Digital TV and Monitors
- Surveillance
- Set Top Boxes
- Networking Systems
- Consumer Electronics
- General Purpose

DESCRIPTION

The SCT2230D is a fully integrated high efficiency synchronous step-down DCDC converter capable of delivering 3A current. The devices operate over a wide input voltage range from 4.2V to 17V and fully integrate high-side power MOSFETs and synchronous MOSFETs with very low Rdson to minimize the conduction loss.

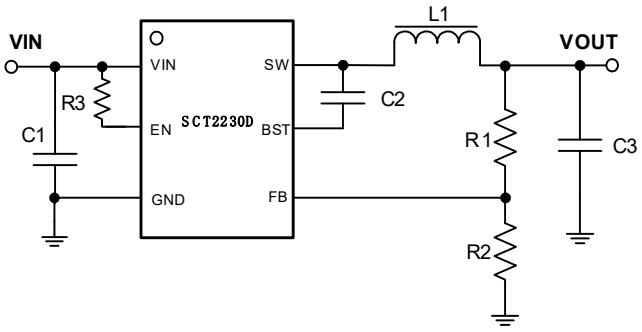
With 800 kHz switching frequency, low output voltage ripple, small external inductor and capacitor size are achieved. SCT2230D adopts adaptive constant ON-time control architecture to achieve fast load transient responses for step-down applications.

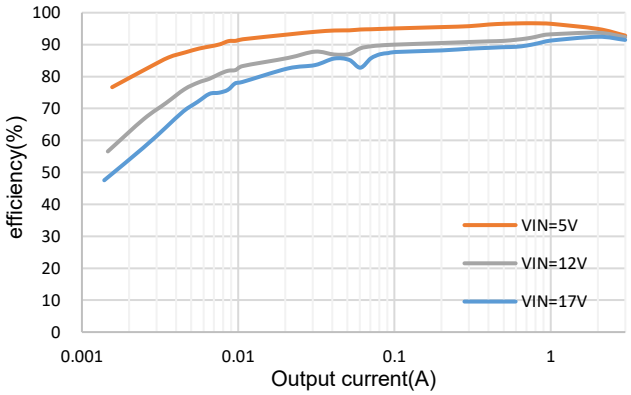
The SCT2230D operates in power saving mode, which maintains high efficiency during light load operation.

It includes full protection features, such as over current protection, output under-voltage protection, input under-voltage lockout, and thermal shutdown.

The SCT2230D requires a minimal number of external components and is available in a space-saving SOT563 and SOT23-6L package

TYPICAL APPLICATION





Efficiency, VOUT=3.3V

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Production

Revision 1.1: Update EC for OC and OT value

Revision 1.2: Update PACKAGE to SOT23-6L

Revision 1.3: Update DEVICE ORDER INFORMATION

Revision 1.4: Update Recommended Component Selections and Recommended Inductor and Resistor Range

Revision 1.5: Update THERMAL INFORMATION

Revision 1.6: Update ABS T_J max information

Revision 1.7: Update PIN FUNCTIONS description and adjust the resistor value in Typical Application

DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL
SCT2230DTVAR	Tape & Reel	5000	230D	6	SOT563-6L	3
SCT2230DTVDR	Tape & Reel	3000	230D	6	SOT23-6L	3

ABSOLUTE MAXIMUM RATING

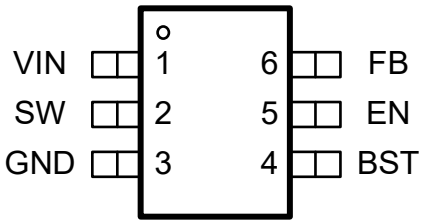
Over operating free-air temperature unless otherwise noted(1)

SYMBOL	MIN	MAX	UNIT
V_{IN}	-0.3	19	V
V_{SW}	-1	19	V
V_{SW} （<10ns）	-2.5	21	V
V_{BST}	V_{SW}-0.3	V_{SW}+6	V
V_{FB} ,V_{EN}	-0.3	6.5	V
Operating junction temperature T_J(2)	-40	150	ºC
Storage temperature T_{STG}	-65	150	ºC

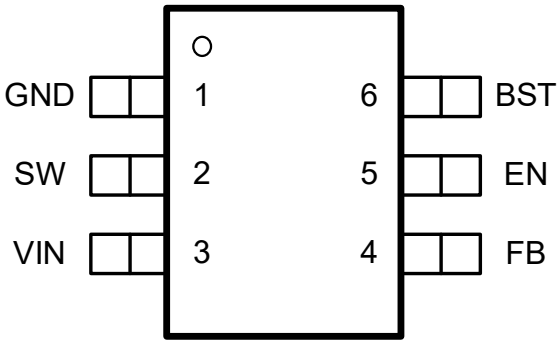
(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN CONFIGURATION



Top View: SOT563 Top View 1.6mm x 1.6mm, Plastic



Top View: SOT23-6L 2.8mm x 2.8mm, Plastic

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PIN FUNCTIONS

NAME	PIN		PIN FUNCTION
	SOT563	SOT23-6	
VIN	1	3	Power supply input. VIN supplies the power to the IC, as well as the step-down converter switches. Drive VIN with a 4.2V to 17V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See Input Capacitor.
SW	2	2	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BST to power the high-side switch.
GND	3	1	Power ground. Must be soldered directly to ground plane.
BST	4	6	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BST pin and SW node.
EN	5	5	Enable logic input. The device has precision enable thresholds 1.215V rising / 1.12V falling for programmable UVLO threshold and hysteresis. The voltage applied to this pin must not exceed 6.5V.
FB	6	4	Buck converter output feedback sensing voltage. Connect a resistor divider from VOUT to FB to set up output voltage. The device regulates FB to the internal reference of 0.8V typical.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	4.2	17	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(1)	-0.5	+0.5	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	SOT563	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance (1) (2)	93.93	°C/W
ψ_{JT}	Junction-to-top characterization parameter (2)	14	
ψ_{JB}	Junction-to-board characterization parameter (2)	26.65	
$R_{\theta JB}$	Junction-to-board thermal resistance (2)	26.84	
$R_{\theta JC(top)}$	Junction to case(top) thermal resistance (1) (2)	99.86	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2230D are mounted, and external environmental factors. The PCB board is a heat sink that is soldered

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to the leads and thermal pad of the SCT2230D. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.
(2) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		4.2		17	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising		4.0 350		V mV
I_{SD}	Shutdown current	EN=0, No load, VIN=12V		1.2		uA
I_Q	Quiescent current	EN=2V, No load, No switching. VIN=12V. BST-SW=5V		220		uA
Enable, Soft Start and Working Modes						
V_{EN_H}	Enable high threshold			1.215		V
V_{EN_L}	Enable low threshold			1.12		V
Power MOSFETs						
R_{DSON_H}	High side FET on-resistance			50		mΩ
R_{DSON_L}	Low side FET on-resistance			24		mΩ
Feedback and Error Amplifier						
V_{FB}	Feedback Voltage	T_J=25°C, CCM	0.788	0.8	0.812	V
Current Limit						
I_{LIM_LSD}	LSD valley current limit		3.5	4.4	5.3	A
Switching Frequency						
F_{SW}	Switching frequency	V_{IN}=12V, V_{OUT}=5V		800		kHz
t_{ON_MIN}	Minimum on-time			70		ns
t_{OFF_MIN}	Minimum off-time			220		ns
Soft Start Time						
t_{SS}	Internal soft-start time			3		ms
Protection						
T_{SD}	Thermal shutdown threshold Hysteresis	T_J rising		155 30		°C

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TYPICAL CHARACTERISTIC0

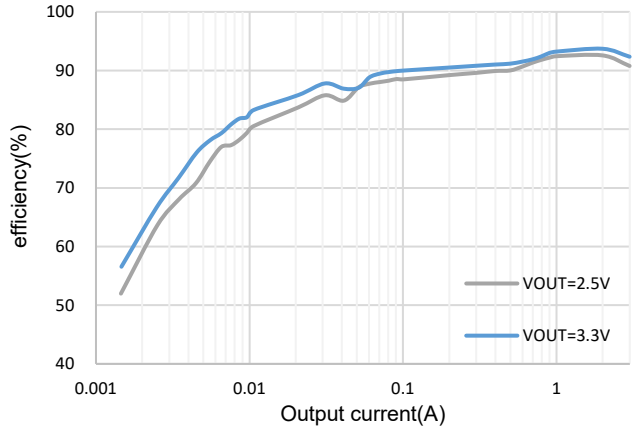


Figure 1. Efficiency vs Load Current(VIN=12V)

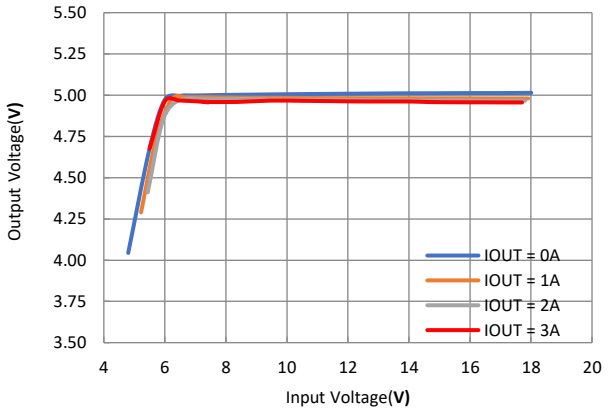


Figure 2. Line Regulation

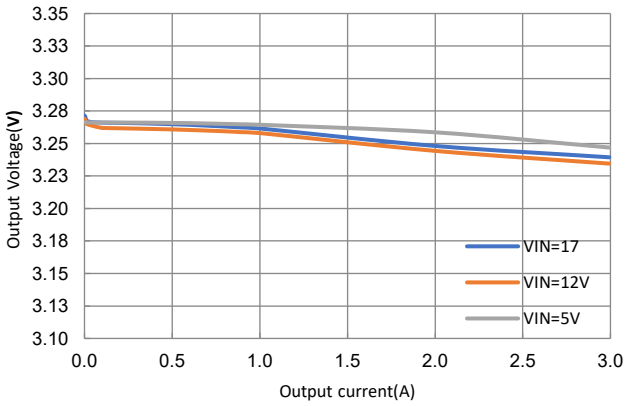


Figure 3. Load Regulation

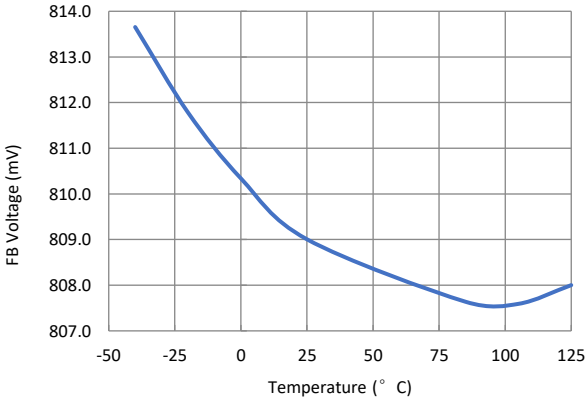


Figure 4. FB Voltage Vs. Temperature

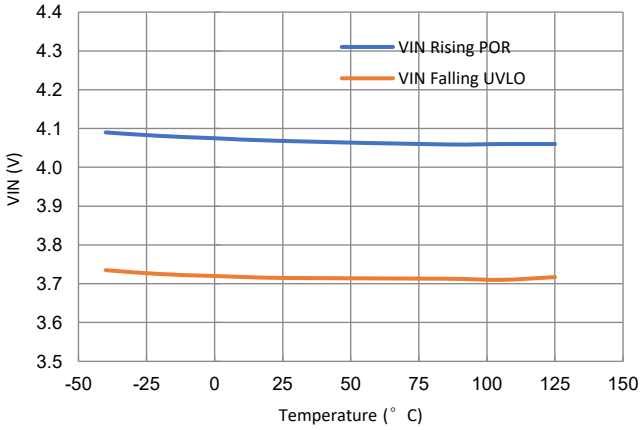


Figure 5. UVLO Vs. Temperature

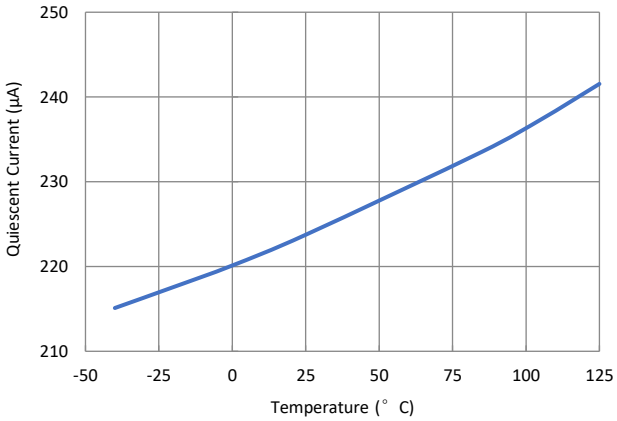
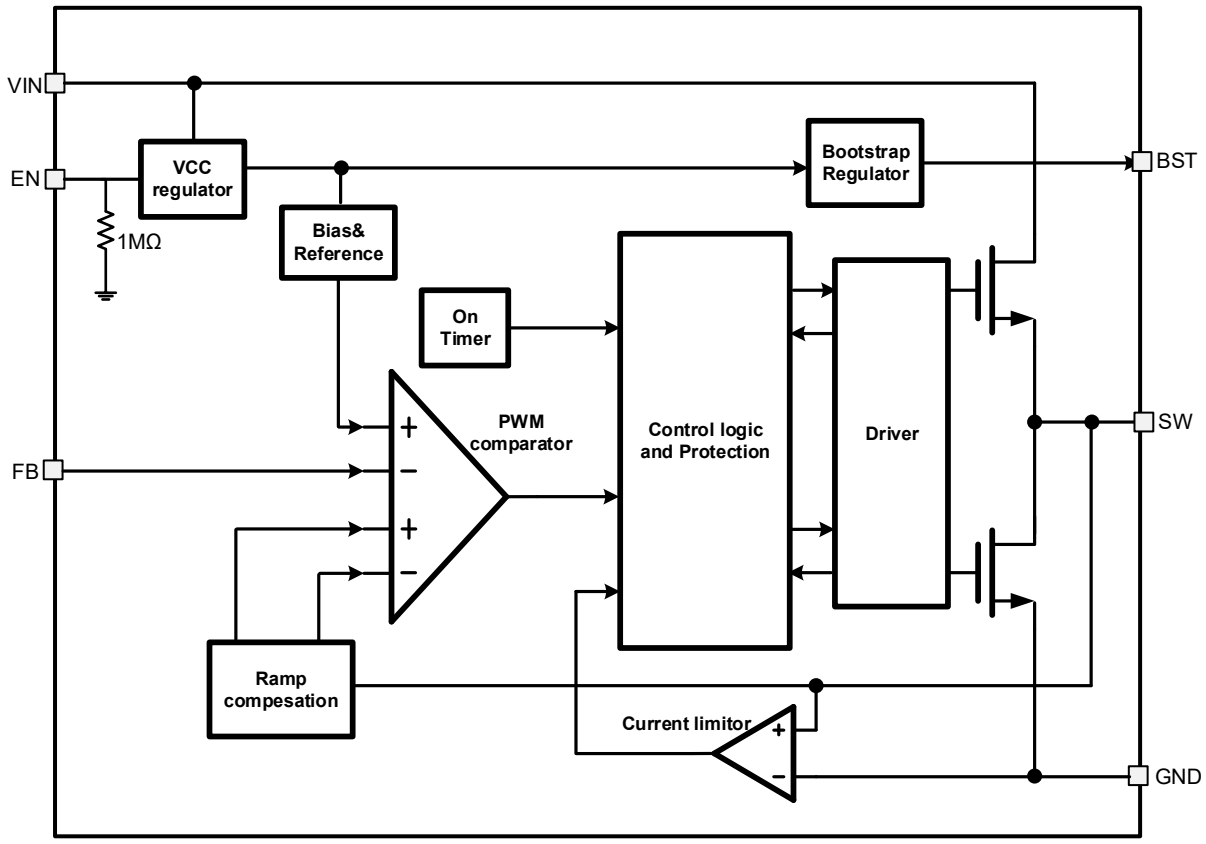


Figure 6. Quiescent Current Vs. Temperature

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FUNCTIONAL BLOCK DIAGRAM



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OPERATION

Adaptive On-time Control

The SCT2230D device is 4.2-17V input, 3A output, synchronous step-down converters with internal power MOSFETs. Adaptive constant on-time (ACOT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET is turned on for a fixed one shot time ON-time period. The one shot time is calculated by the converter's input voltage (VIN) and the output voltage (VOUT) cycle-by-cycle based to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. SCT2230D turns off high-side MOSFET after the fixed on time and turns on the low-side MOSFET. SCT2230D turns off the low-side MOSFET once the output voltage dropped below the output regulation, the one-shot timer then reset and the high-side MOSFET is turned on again. The on-time is inversely proportional to the input voltage and proportional to the output voltage. It can be calculated using the following equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_S} \quad (1)$$

Where:

VOUT is the output voltage.
VIN is the input voltage.
fs is the switching frequency.

After an ON-time period, the regulator goes into the OFF-time period. The OFF-time period length depends on VFB in most cases. It will end when the FB voltage decreases below 0.8V, at which point the ON-time period is triggered. If the OFF-time period is less than the minimum OFF time, the minimum OFF time will be applied, which is around 220ns typical.

Power Saving Mode (PSM)

The SCT2230D is designed with Power Save Mode (PSM) at light load conditions for high power efficiency. The regulator automatically reduces the switching frequency and extends Toff while no Ton changing during the light load condition to get high efficiency and low output ripple. As the output current decreases from heavy load condition, the inductor current decreases as well, eventually nearing zero current, this is the boundary between CCM and DCM. The low side MOSFET is turned off when the inductor current reaches zero level. The load is provided only by output capacitor, when FB voltage is lower than 0.8V, the next ON cycle begins. When the output current increases from light to heavy load the switching frequency increases to keep output voltage. The transition point to light load operation can be calculated using the following equation (2):

$$I_{LOAD} = \frac{V_{IN} - V_{OUT}}{2L} \times T_{ON} \quad (2)$$

Where:

TON is on-time

VIN Power

The SCT2230D is designed to operate from an input voltage supply range between 4.2V to 17V, at least 0.1uF decoupling ceramic cap is recommended to bypass the supply noise. If the input supply locates more than a few inches from the converter, an additional electrolytic or tantalum bulk capacitor or with recommended 10uF may be required in addition to the local ceramic bypass capacitors.

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Under Voltage Lockout UVLO

The SCT2230D Under Voltage Lock Out (UVLO) default startup threshold is typical 4V with VIN rising and shutdown threshold is 3.65V with VIN falling. The more accurate UVLO threshold can be programmed through the precision enable threshold of EN pin.

Enable and Start up

When applying a voltage higher than the EN high threshold (typical 1.215V/rise), the SCT2230D enables all functions and the device starts soft-start phase. The SCT2230D has the built in 3ms soft-start time to prevent the output overshoot and inrush current. When EN pin is pulled low, the internal SS net will be discharged to ground. Buck operation is disabled when EN voltage falls below its lower threshold (typically 1.12V/fall).

An internal 1MΩ resistor from EN to GND allow EN float to shut down the chip. EN is clamped internally using a 5V series diode. For applications where a specified VIN UVLO voltage needs to be set, EN connects a resistor R3 to VIN to form a voltage divider with a 1M resistor inside the chip for the configuration of VIN UVLO voltage, as shown in Figure 7. The resistor distributor R3 is calculated by Equation (3).

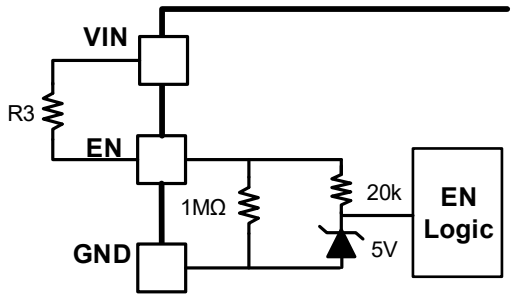


Figure 7. Adjustable VIN UVLO

$$R3 = \frac{(V_{start} - V_{ENR}) \times R}{V_{ENR}} \quad (3)$$

$$\text{Vstop} = V_{ENF} \times \frac{R + R_3}{R} \quad (4)$$

Where:

- Vstart: Vin rise threshold to enable the device
- Vstop: Vin fall threshold to disable the device
- V_{ENR}=1.215V
- V_{EMF}=1.12V
- R=1MΩ

Over Current Protection (OCP) and Hiccup Mode

In each switching cycle, the inductor current is sensed by monitoring the low-side MOSFET during the OFF period. When the voltage between GND pin and SW pin is lower than the over current threshold voltage, the OCP will be

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triggered and the controller keeps the OFF state. A new switching cycle will begin only when the measured voltage is higher than limit voltage. If output loading continues to increase, output will drop below the UVP, and SS pin is discharged such that output is 0V. Then the device will count for 7 cycles of soft-start time for hiccup waiting time and restart normally after 7 cycles' soft-start period.

Bootstrap Voltage Regulator

An external bootstrap capacitor between BST and SW pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

Thermal Shutdown

Once the junction temperature in the SCT2230D exceeds 155°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 125°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

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APPLICATION INFORMATION

Typical Application

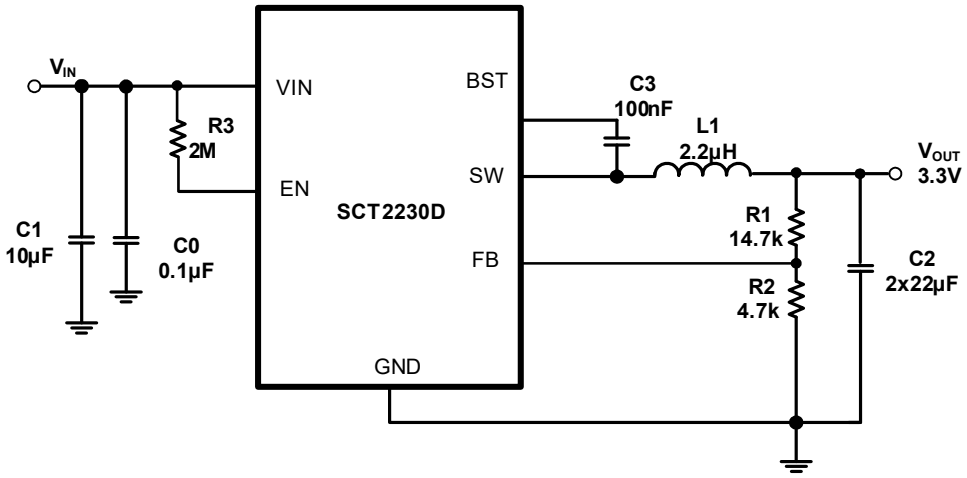


Figure 8. 12V Input, 3.3V/3A Output

Design Parameters

Design Parameters	Example Value
Input Voltage	12V
Output Voltage	3.3V
Output Current	3A
Switching Frequency	800kHz

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Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A ceramic capacitor 10μF is recommended for the decoupling capacitor and a 0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin of the SCT2230D.

Use Equation (5) to calculate the input voltage ripple:

$$\Delta V_{IN} = \frac{I_{OUT}}{C_{IN} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

Where:

- C_{IN} is the input capacitor value
- f_{sw} is the converter switching frequency
- I_{OUT} is the maximum load current

Due to the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the VIN pin. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, a 25V/10uF input ceramic capacitor is recommended for most of applications. Choose the right capacitor value carefully with considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

Inductor Selection

The performance of inductor affects the power supply's steady state operation, transient behavior, loop stability, and buck converter efficiency. The inductor value, DC resistance (DCR), and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DCR, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the maximum input voltage, minimum output voltage, maxim load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a buck converter, calculate the inductor minimum value as shown in equation (6).

$$L_{INDMIN} = \frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{V_{INMAX} \times K_{IND} \times I_{OUT} \times f_{SW}} \quad (6)$$

Where:

- K_{IND} is the coefficient of inductor ripple current relative to the maximum output current.

Therefore, the peak switching current of inductor, I_{LPEAK}, is calculated as in equation (7).

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$$I_{LPEAK} = I_{OUT} + K_{IND} \times \frac{I_{OUT}}{2} \quad (7)$$

Set the current limit of the SCT2230D higher than the peak current I_{LPEAK} and select the inductor with the saturation current higher than the current limit. The inductor's DC resistance (DCR) and the core loss significantly affect the efficiency of power conversion. Core loss is related to the core material and different inductors have different core loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss.

Table 1 lists recommended inductors for the SCT2230D. Verify whether the recommended inductor can support the user's target application with the previous calculations and bench evaluation. In this application, the WE's inductor 744311220 is used on SCT2230D evaluation board.

Table 1. Recommended Inductors

Part Number	L (uH)	DCR Max (mΩ)	Saturation Current/Heat Rating Current (A)	Size Max (LxWxH mm)	Vendor
744311220	2.2	11.4	13	7.3x7.2x3.8	Wurth Electronik

Output Feedback Resistor Divider Selection

The SCT2230D features external programmable output voltage by using a resistor divider network R1 and R2 as shown in the typical application circuit Figure 8. Use equation (8) to calculate the resistor divider values.

$$R_1 = \frac{(V_{OUT} - V_{ref}) \times R_2}{V_{ref}} \quad (8)$$

Table 2. Recommended Component Selections

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	C1 (μF)	C2 (μF)	C3 (nF)
1.2	1.5	3	1.5	10	2 x 22	100
1.5	2.61	3	1.5	10	2 x 22	100
1.8	10.2	8.2	2.2	10	2 x 22	100
2.5	10	4.7	2.2	10	2 x 22	100
3.3	14.7	4.7	2.2	10	2 x 22	100
5.0	10.5	2	3.3	10	2 x 22	100

Table 3. Recommended Inductor and Resistor Range

Output Voltage (V)	L (μH)	R2 (kΩ)
VOUT ≤ 2	1 ≤ L < 2	< 3.5
	2 ≤ L < 4.7	< 10
	L ≥ 4.7	< 35
2 < VOUT ≤ 3.3	1 ≤ L < 2	< 2
	2 ≤ L < 4.7	< 5
	L ≥ 4.7	< 15
3.3 < VOUT ≤ 5	1 ≤ L < 2	< 1.5
	2 ≤ L < 4.7	< 3
	L ≥ 4.7	< 8

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Application Waveforms

Vin=12V, Vout=3.3V, unless otherwise noted

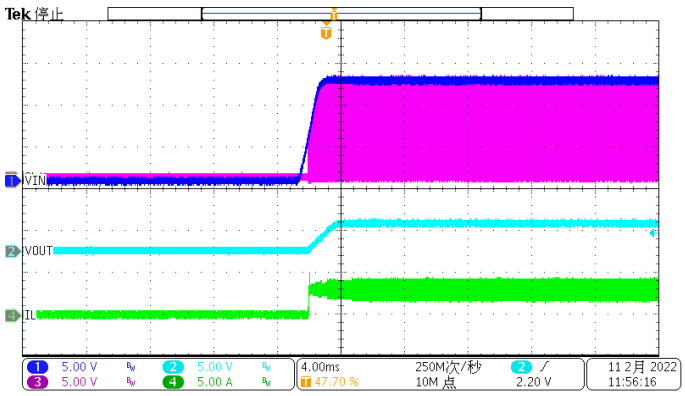


Figure 9. Power up

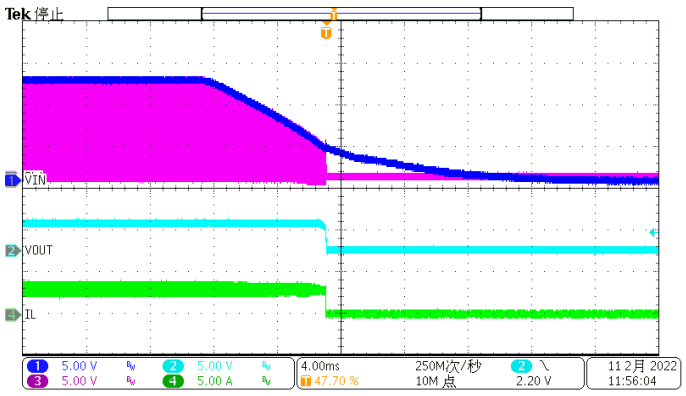


Figure 10. Power down

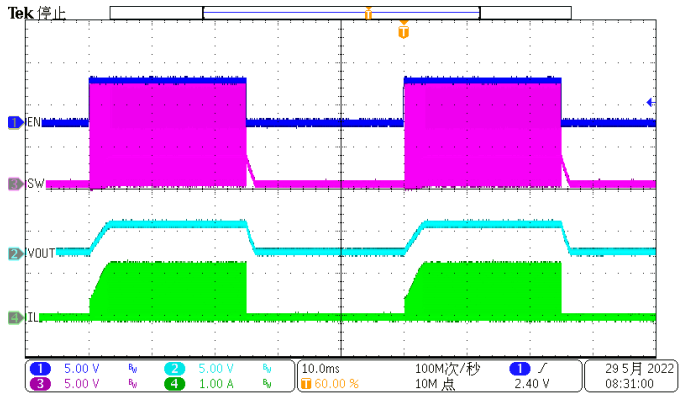


Figure 11. EN toggle（Iout=0.1A）

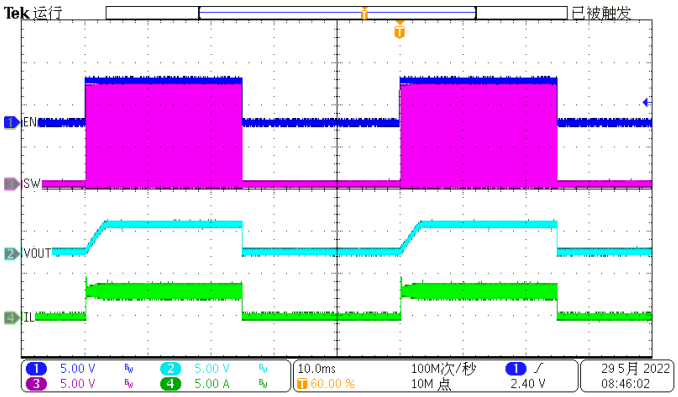


Figure 12. EN toggle（Iout=3A）

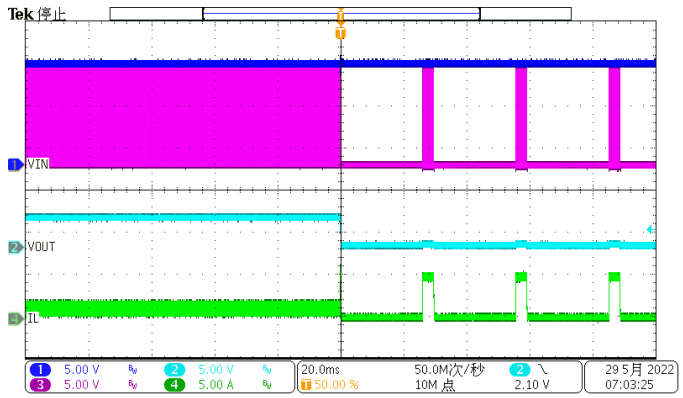


Figure 13. Over Current Protection (1A to hard short)

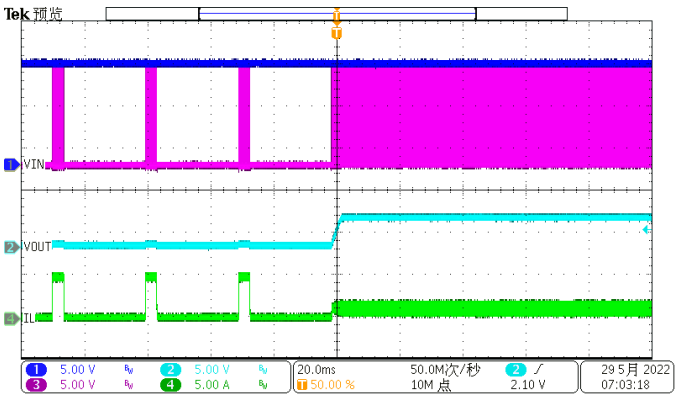


Figure 14. Over Current Release (1A to hard short)

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Application Waveforms

Vin=12V, Vout=5V, unless otherwise noted

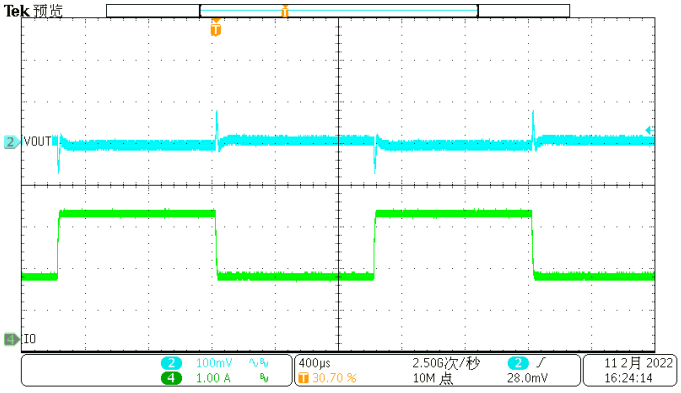


Figure 15. Load Transient (1.5A-3A, 1.6A/us)

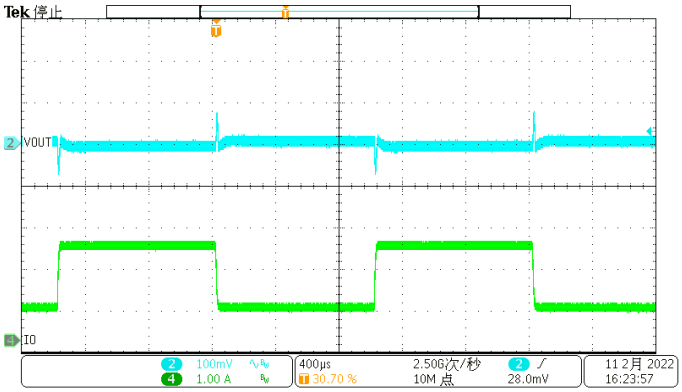


Figure 16. Load Transient (0.75A-2.25A, 1.6A/us)

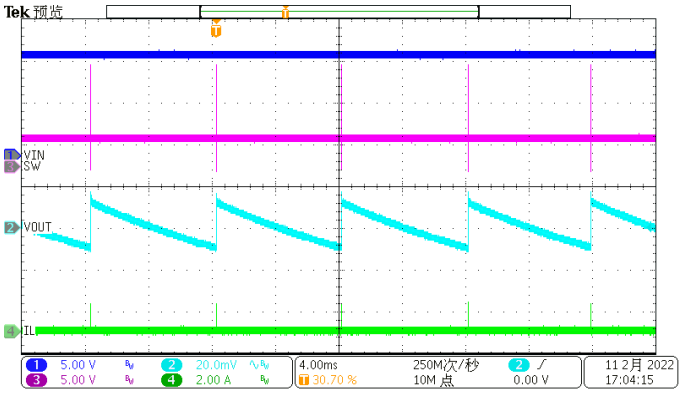


Figure 17. Output Ripple (Iload=0A)

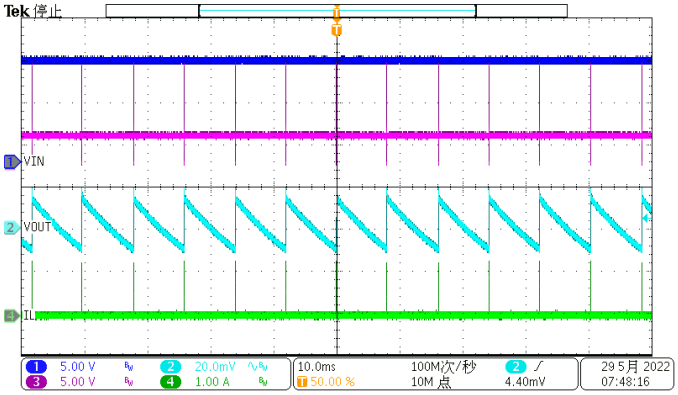


Figure 18. Output Ripple (Iload=0.1A)

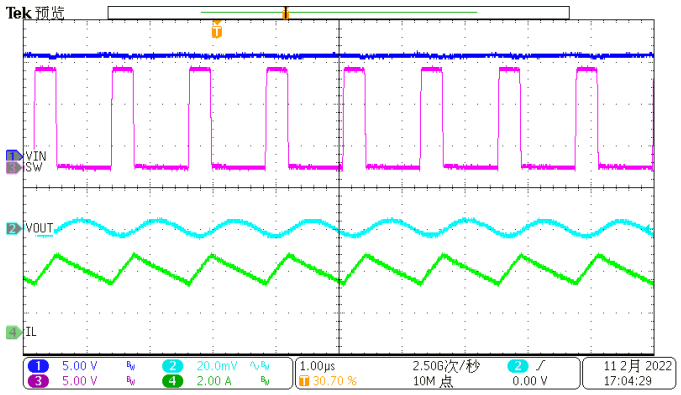


Figure 19. Output Ripple (Iload=3A)

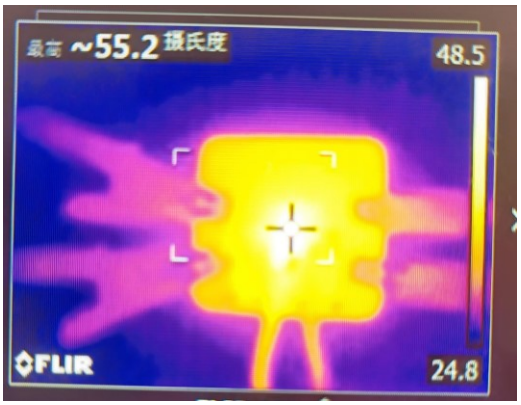


Figure 20. Thermal, 12VIN, 3.3Vout, 3A(SOT563)

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Layout Guideline

The regulator could suffer from instability and noise problems without carefully layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be very close to the VIN pin and GND pin to reduce the input supply ripple. Place the capacitor as close to VIN pin as possible to reduce high frequency ringing voltage on SW pin as well. Figure 21, Figure 22 is the recommended PCB layout of SCT2230D.

The layout needs be done with well consideration of the thermal. A large top layer ground plate using multiple thermal vias is used to improve the thermal dissipation. The bottom layer is a large ground plane connected to the top layer ground by vias.

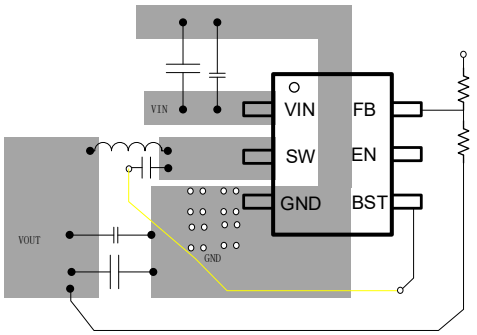


Figure 21.SOT563 PCB Layout Example

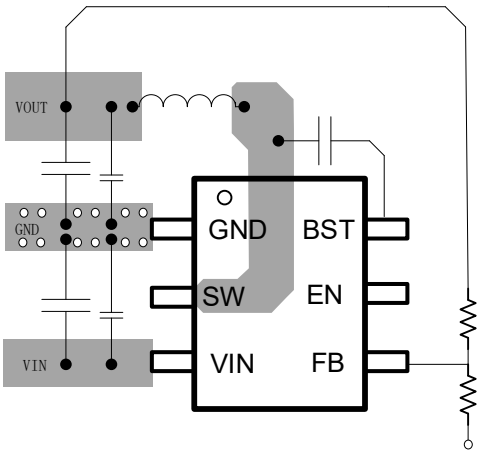


Figure 22.SOT23-6 PCB Layout Example

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Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation (9).

$$P_{D(MAX)} = \frac{125 - TC_A}{R_{\psi JA}} \quad (9)$$

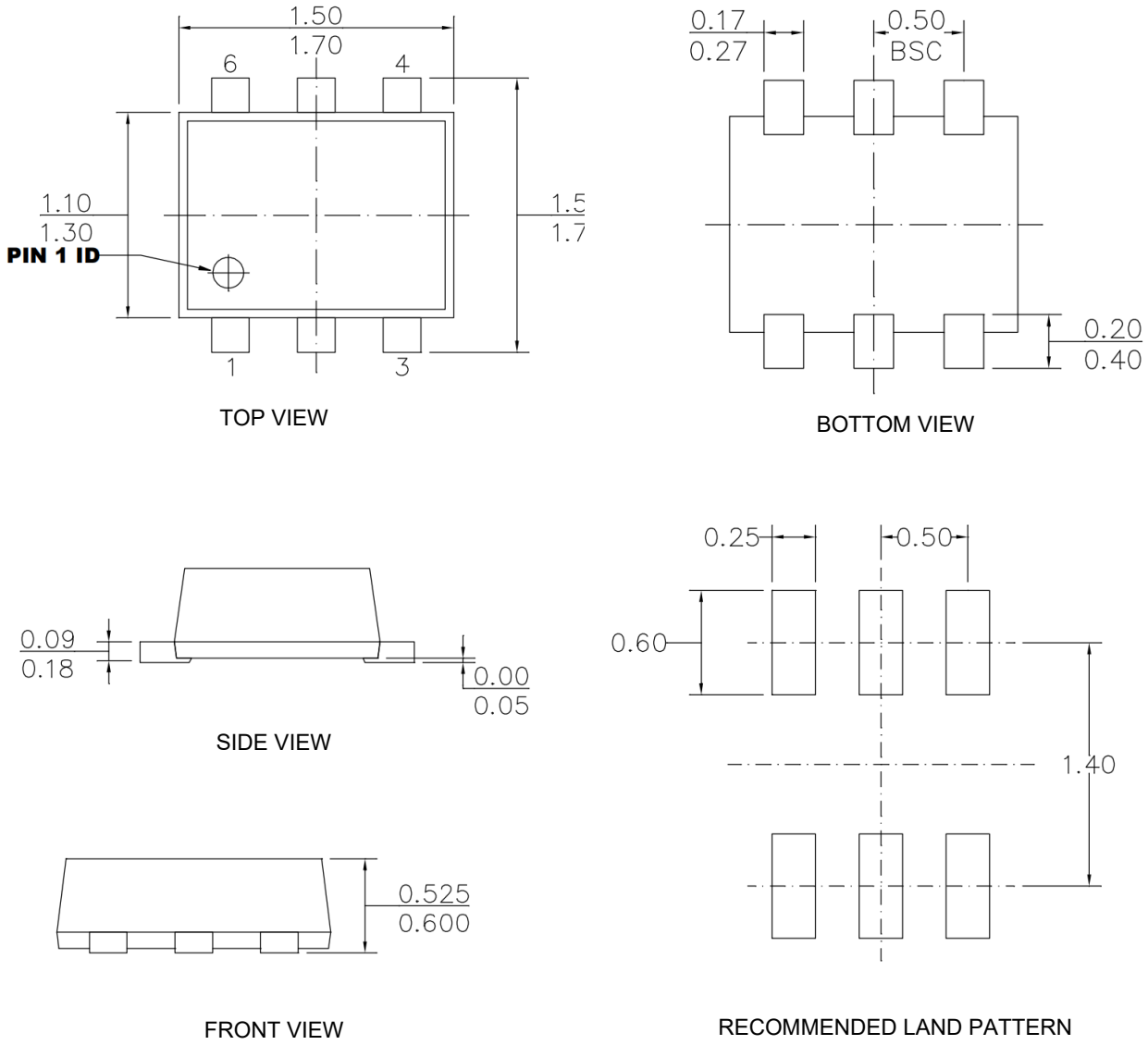
where

- T_A is the maximum ambient temperature for the application.
- $R_{\psi JA}$ is the junction-to-ambient thermal resistance.

The real junction-to-ambient thermal resistance $R_{\psi JA}$ of the package greatly depends on the PCB type, layout, thermal pad connection and environmental factor. Using thick PCB copper and soldering the GND to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also enhance the thermal capability.

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PACKAGE INFORMATION

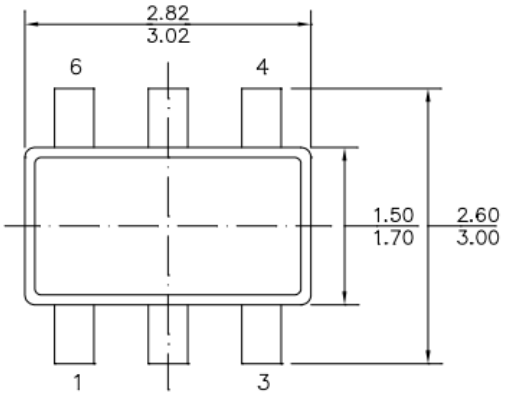


SOT563-6L Package Outline Dimensions

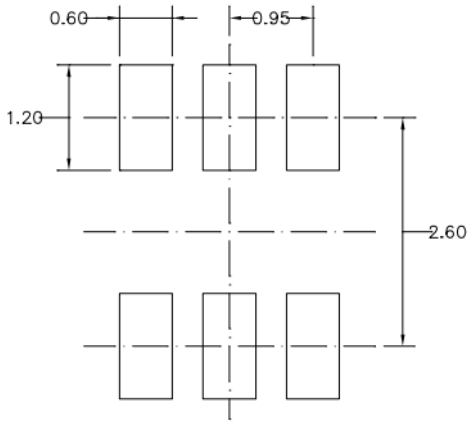
NOTE:

1. THE LEAD SIDE IS WETTABLE.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4. JEDEC REFERENCE IS MO-220.
5. DRAWING IS NOT TO SCALE.

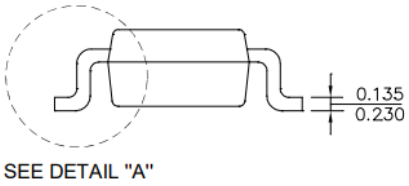
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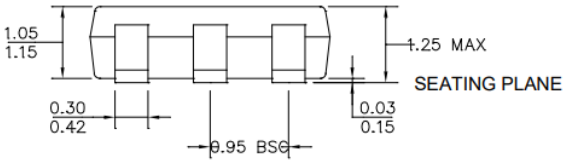
TOP VIEW



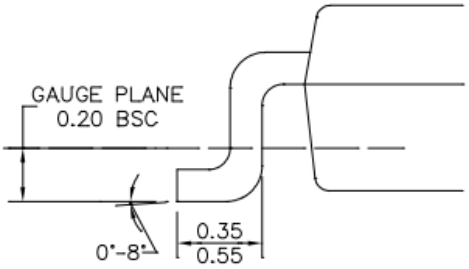
BOTTOM VIEW



SIDE VIEW



FRONT VIEW



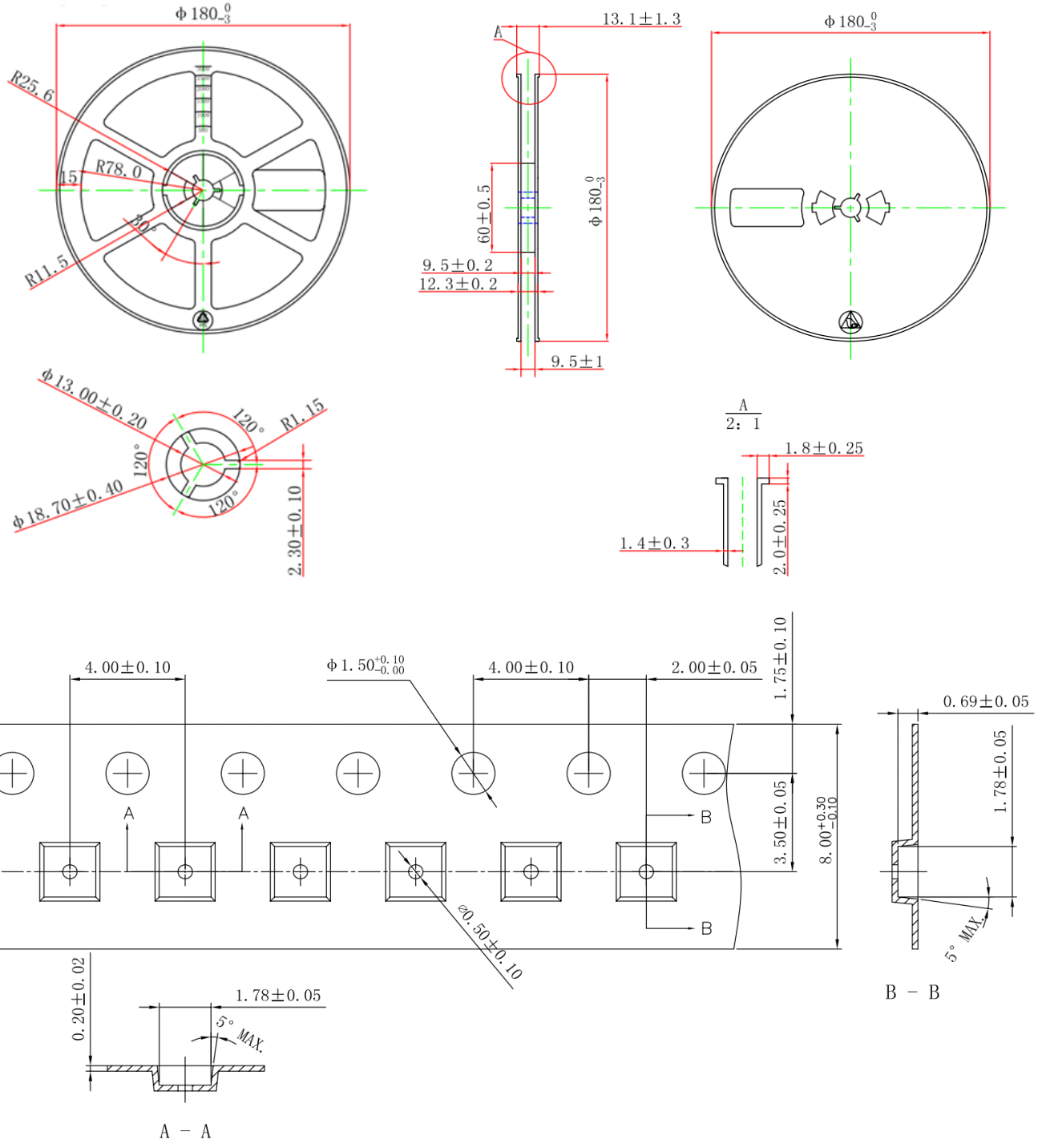
RECOMMENDED LAND PATTERN

SOT23-6L Package Outline Dimensions

NOTE:

6. THE LEAD SIDE IS WETTABLE.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
9. JEDEC REFERENCE IS MO-220.
10. DRAWING IS NOT TO SCALE.

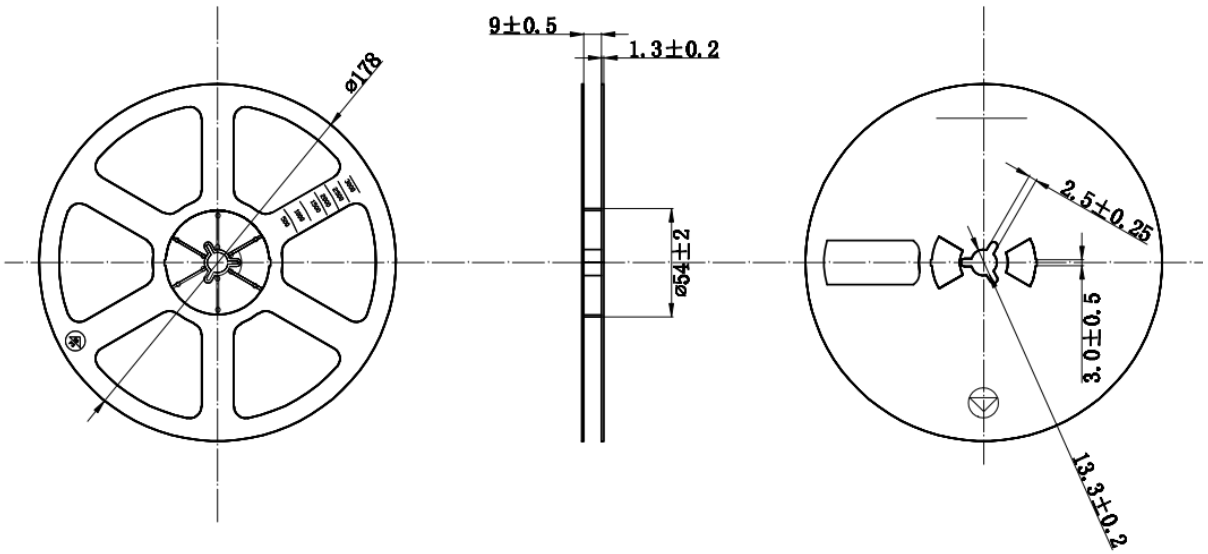
TAPE AND REEL INFORMATION



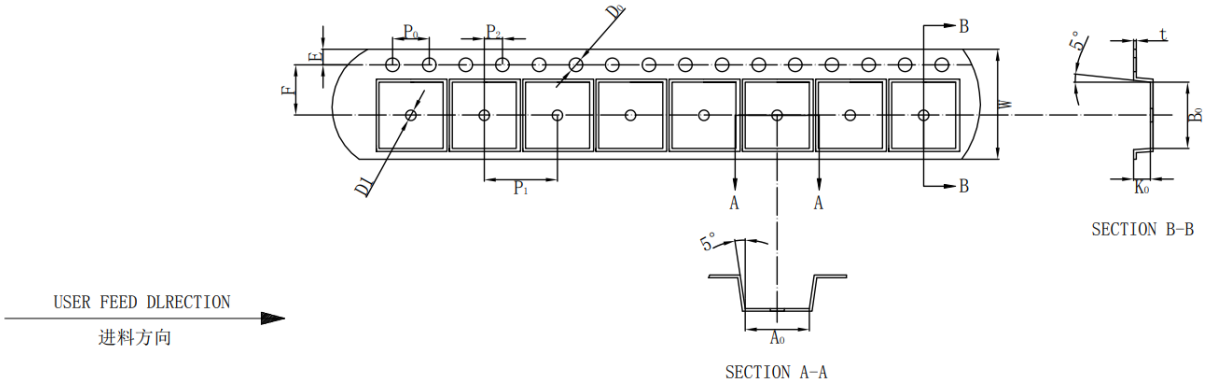
TAPE DIMENSIONS

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TAPE AND REEL INFORMATION



ITEM	W	Ao	Bo	Ko	E	F	D1	D_0	P_0	P_1	P_2	t
MIN	7.80	3.15	3.25	1.28	1.65	3.45	—	—	3.90	3.90	1.95	0.20
NOM	8.00	3.25	3.30	1.38	1.75	3.50	1.00	1.50	4.00	4.00	2.00	0.25
MAX	8.20	3.35	3.40	1.48	1.85	3.55	1.10	1.60	4.10	4.10	2.05	0.30



TAPE DIMENSIONS