3V-40V Vin, 500mA, Ultra-Low Quiescent Current LDO with Power-Good

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H3A
  - Device CDM ESD Classification Level C3
- Wide Input Range: 3V-40V
- With up to 45V Transient Input Voltage
- Maximum Output Current: 500mA
- Output Voltage:
  - 3.3V and 5V (Fixed Output)
  - 1.25V~25V (Adjustable Output Version)
- Output Voltage Accuracy:
  - T_J= 25℃：±1%
  - T_J= -40℃~ 125℃：±2%
- Ultra-Low Quiescent Current: 2.6μA
- Low Dropout Voltage：
  - 149mV at 150mA load current(ESOP-8L package)
  - 165mV at 150mA load current(TO252-4L package)
- Support Output Capacitors Range:
  - 3.3uF~220uF
  - Low-ESR: 0.001Ω~ 5 Ω
- 1.5ms Internal Soft-start Time
- Current Limit Protection with VIN_HIGH Control
- Precision Enable Threshold for Programmable Input Voltage Under-Voltage Lock Out Protection (UVLO) Threshold and Hysteresis
- Power-Good and Programmable Power-Good delay
- Over-Temperature Protection
- Available Package：ESOP-8L/TO252-4L

APPLICATIONS

- Automotive Head Units
- Headlights
- Body Control Modules
- Inverter and Motor Controls

DESCRIPTION

The SCT71405Q series products is a low-dropout linear regulator designed to operate with a wide input-voltage range from 3V to 40V and 500mA output current with enable control and Power-Good feature. The SCT71405Q series products is stable with 3.3uF~220uF output capacitors, and 10uF ceramic capacitor is recommended.

Only 2.6μA typical quiescent current at light load makes the SCT71405Q series products ideal choices for portable devices with battery power supply and an optimal solution for powering microcontrollers (MCUs) and CAN/LIN transceivers in always-on systems.

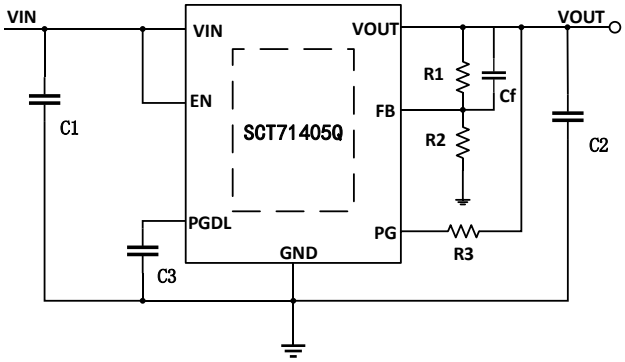
The SCT71405Q series products implements power good circuit (PG) which indicates that output voltage is in regulation, and the Power-Good delay is Programmable. This signal could be used for power sequencing or as a microcontroller reset.

The SCT71405Q series products integrated short-circuit and overcurrent protection with VIN_HIGH Control feature, which makes the device more reliable during transient high-load current faults or shorting events.

The SCT71405Q series products provide fixed 3.3V and 5V output voltage versions, and also provide adjustable output version which can adjust the output voltage from 1.25V to 25V.

The SCT71405Q series products is available in ESOP-8L and TO252-4L packages, for other package options, please contact SCT sales.

TYPICAL APPLICATION



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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Release to production(ESOP-8L package).

Revision 1.1: Update the ELECTRICAL CHARACTERISTICS.

Revision 1.2: Update DEVICE ORDER INFORMATION, TAPE AND REEL INFORMATION and THERMAL INFORMATION.

Revision 1.3: Update the line regulation, load regulation and the functional block diagram.

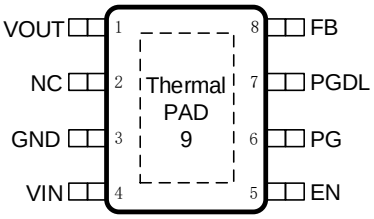
Revision 1.4: Update figure 3 and figure 9. Update the MSL in device order information table.

DEVICE ORDER INFORMATION

Orderable Device	Output Voltage	Package	Package Marking	PINS	MSL	Transport Media, Quantity
SCT71405A00QSTER	Adjustable	ESOP-8L	5A00Q	8	3	Tape & Reel, 4000
SCT71405F50BQSTER	Fixed 5.0V	ESOP-8L	F50BQ	8	3	Tape & Reel, 4000
SCT71405F33BQSTER	Fixed 3.3V	ESOP-8L	F33BQ	8	3	Tape & Reel, 4000
SCT71405F50QOWCR	Fixed 5.0V	TO252-4L	5F50Q	4	3	Tape & Reel, 2500
SCT71405F33QOWCR	Fixed 3.3V	TO252-4L	5F33Q	4	3	Tape & Reel, 2500
SCT71405F50AQOWCR	Fixed 5.0V	TO252-4L	F50AQ	4	3	Tape & Reel, 2500

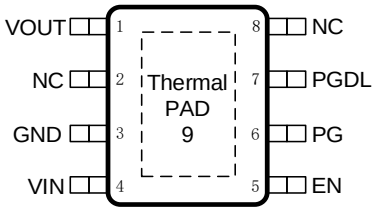
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PIN CONFIGURATION



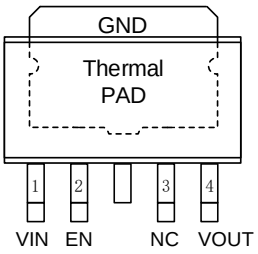
SCT71405A00QSTER

ESOP-8L Package



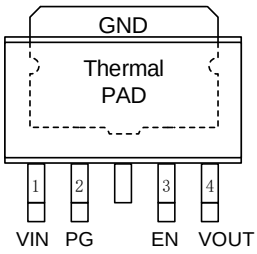
SCT71405FxxBQSTER

ESOP-8L Package



SCT71405FxxQOWCR

TO252-4L Package



SCT71405FxxAQOWCR

TO252-4L Package

PIN FUNCTIONS

NAME	PIN FUNCTION		
	ESOP-8L	ESOP-8L	
VOUT	1	1	Regulated output voltage pin.
NC	2	2,8	No connection.
GND	3	3	Ground reference pin.
VIN	4	4	Input voltage pin.
EN	5	5	Enable input pin.
PG	6	6	Power-good pin.
PGDL	7	7	Programmable Power-Good Delay Time.
FB	8	—	Feedback Input for Output Adjustable Version.
Thermal Pad	9	9	Connect the thermal pad to a large area GND plane for improved thermal performance.

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NAME	PIN FUNCTION		
	TO252-4L	TO252-4L	
VOUT	4	4	Regulated output voltage pin.
NC	3	—	No connection.
VIN	1	1	Input voltage pin.
EN	2	3	Enable input pin.
PG	—	2	Power-good pin.
Thermal Pad	5	5	Connect the thermal pad to a large area GND plane for improved thermal performance.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3	40	V
V_{OUT}	Fixed Output voltage(TO252-4L package)	3.3	5	V
	Fixed Output voltage(ESOP-8L package)	3.3	5	V
	Adjustable Output Version	1.25	25	V
V_{EN}	Enable input voltage	0	V_{IN}	V
V_{PG}	Power-good pin voltage	0	5	V
C_{IN}	Input capacitor	2.2	--	uF
C_{OUT}	Output capacitor	3.3	220	uF
ESR	Output capacitor ESR requirements	0.001	5	Ω
T_A	Operating ambient temperature	-40	125	°C
T_J	Operating junction temperature	-40	125	°C

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted (1)

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Maximum input voltage range	-0.3	45	V
V_{OUT}	Maximum output voltage range	-0.3	25	V
V_{EN}	Maximum enable input voltage	-0.3	V_{IN}	V
V_{PG}	Maximum power-good pin voltage	-0.3	25	V
V_{PGDL}	Maximum power-good delay pin voltage	-0.3	5.5	V
V_{FB}	Maximum feedback pin voltage	-0.3	5.5	V
T_J (2)	Junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

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ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-4.5	+4.5	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins(2)	-2	+2	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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THERMAL INFORMATION

The value of $R_{\theta JA}$ and $R_{\theta JC}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. Because they were simulated in accordance with JESD 51-7. They do not represent the performance obtained in an actual application. For design information see Power Dissipation and Thermal Performance section.

The value of $R_{\theta JA_EVM}$ is the tested results based on our EVM, and is more useful for thermal design. Even if it still do not represent the thermal performance of customer's PCB design, but it was a good starting point for thermal performance design.

The PCB information of our EVM: 4-layer, both the inner and outer layers are 1oz Cu, 50mm x 30mm size.

The values given in this table are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB), thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the device. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual values of the below table.

PARAMETER（4-layer）	THERMAL METRIC	ESOP-8L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance	52.18	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.2	
Ψ_{JB}	Junction-to-board characterization parameter	16.58	
$R_{\theta JCtop}$	Junction to case thermal resistance	83.77	
$R_{\theta JA_EVM}$	junction to ambient thermal resistance	33.21	
PARAMETER（4-layer）	**THERMAL METRIC**	**TO252-4L**	**UNIT**
$R_{\theta JA}$	Junction to ambient thermal resistance	29.63	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	6.54	
Ψ_{JB}	Junction-to-board characterization parameter	13.35	
$R_{\theta JCtop}$	Junction to case thermal resistance	50.45	
$R_{\theta JA_EVM}$	junction to ambient thermal resistance	24.22	

(1) $R_{\theta JA}$ is junction to ambient thermal resistance, based on JESD51-7.

(2) $R_{\theta JC}$ is junction to case thermal resistance, based on JESD51-7.

(3) $R_{\theta JA_EVM}$ is junction to ambient thermal resistance, which is tested on SCT EVM.

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ELECTRICAL CHARACTERISTICS

V_{IN}=V_{OUT}+1V, C_{OUT}=10uF, T_J= -40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating input voltage		3		40	V
V_{UVLO}	V_{IN} UVLO Threshold	V_{IN} rising		2.49	2.81	V
	Hysteresis(ESOP-8L package)			60		mV
	Hysteresis(TO252-4L package)			30		mV
I_{SHDN}	Shutdown current from VIN pin	EN=0, V_{OUT}=3.3V, V_{IN}=4.3V		0.29		μA
		EN=0, V_{OUT}=5V, V_{IN}=6V		0.43		μA
		EN=0, V_{OUT}=3.3V/5V, V_{IN}=12V		0.7		μA
I_Q	Quiescent current from GND pin	EN float, no load, V_{IN}=V_{OUT}+1V （not include I_{FB}）		2.6		μA
		EN float, no load, V_{IN}=12V （not include I_{FB}）		2.9		μA
		EN float, no load, V_{IN}=V_{OUT}+1V （Fixed Output voltage）		4.2		μA
		EN float, no load, V_{IN}=12V （Fixed Output voltage）		4.4		μA
Regulated Output Voltage and Current						
V_{OUT}	Output voltage accuracy	T_J= 25°C	-1%		1%	
		T_J= -40°C~125°C	-2%		2%	
ΔV_{OUT}	Line regulation	V_{IN}=V_{OUT}+1V to 40V, Iout=1mA		1	10	mV
	Load regulation	Iout=1mA to 500mA		10	70	mV
V_{REF}	Reference voltage of FB	T_J= 25°C	1.238	1.25	1.262	V
		T_J= -40°C~125°C	1.225	1.25	1.275	V
V_{DROP}	Dropout voltage(1) (ESOP-8L package)	V_{IN}=V_{OUT}-0.1V ,Iout =100mA		98		mV
		V_{IN}=V_{OUT}-0.1V ,Iout =150mA		149		mV
		V_{IN}=V_{OUT}-0.1V ,Iout =500mA		663		mV
V_{DROP}	Dropout voltage(TO252-4L package)	V_{IN}=V_{OUT}-0.1V ,Iout =100mA		108		mV
		V_{IN}=V_{OUT}-0.1V ,Iout =150mA		165		mV
		V_{IN}=V_{OUT}-0.1V ,Iout =500mA		730		mV
I_{OUT}	Output current	V_{OUT} in regulation	0		500	mA
I_{SC_VINLOW}	Short current limit	V_{OUT}=0V, VIN<30V	520	700	850	mA
$I_{SC_VINHIGH}$	Short current limit	V_{OUT}=0V, VIN>30V		430		mA
PSRR	Power supply rejection ratio(2)	I_{OUT}=10mA, f=1kHz, C_{OUT}=10μF		54		dB
		I_{OUT}=10mA, f=10kHz, C_{OUT}=10μF		36		dB
		I_{OUT}=10mA, f=100kHz, C_{OUT}=10μF		43		dB
Enable and Soft-startup						
V_{EN_H}	Enable high threshold			1.47		V
V_{EN_L}	Enable low threshold			1.27		V
V_{EN_Hys}	Enable threshold hysteresis			200		mV
I_{EN_0V}	Enable pin pull-up current	EN=0V		0.27		μA
T_{SS}	Soft-start time			1.5		mS

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SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Good						
V_{PG_R}	PG rising threshold percentage	$V_{OUT}/V_{OUT(NOM)}$,when V_{OUT} rising(ESOP-8L package)		92%		
V_{PG_F}	PG falling threshold percentage	$V_{OUT}/V_{OUT(NOM)}$,when V_{OUT} falling(ESOP-8L package)		86%		
V_{PG_R}	PG rising threshold percentage	$V_{OUT}/V_{OUT(NOM)}$,when V_{OUT} rising(TO252-4L package)		89%		
V_{PG_F}	PG falling threshold percentage	$V_{OUT}/V_{OUT(NOM)}$,when V_{OUT} falling(TO252-4L package)		89%		
V_{PG_LOW}	PG output low voltage	PG sink 1mA		142		mV
R_{PG}	PG pull down resistor	$R_{PG}=V_{PG_LOW}/1mA$		142		Ω
I_{PG_LKG}	PG leakage current	PG=5V, V_{OUT} in regulation			0.2	uA
$Td_{_PGR}$	PG signal turn to high delay	From V_{OUT}>0.92x$V_{OUT(NOM)}$ to PG rising edge delay time(ESOP-8L package)		50		us
$Td_{_PGF}$	PG signal turn to low delay	From V_{OUT}<0.86x$V_{OUT(NOM)}$ to PG falling edge delay time(ESOP-8L package)		20		us
$Td_{_PGR}$	PG signal turn to high delay	From V_{OUT}>0.89x$V_{OUT(NOM)}$ to PG rising edge delay time(TO252-4L package)		300		us
$Td_{_PGF}$	PG signal turn to low delay	From V_{OUT}<0.89x$V_{OUT(NOM)}$ to PG falling edge delay time(TO252-4L package)		23		us
I_{PGDL}	PGDL charging current			16		uA
V_{PGDL_R}	PGDL rising threshold			1.77		V
V_{PGDL_F}	PGDL falling threshold			0.387		V
Thermal Protection						
T_{SD}	Thermal shutdown threshold(3)	T_J rising Hysteresis		175 12		°C °C

(1) The dropout voltage is defined as V_{IN}-V_{OUT}, when force V_{IN} is 100mV below the value of V_{OUT} for $V_{IN}=V_{OUT(NOM)}$+1V.

(2) PSRR is derived from bench characterization, not production test.

(3) Thermal shutdown threshold is derived from bench characterization, not production test.

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TYPICAL CHARACTERISTICS

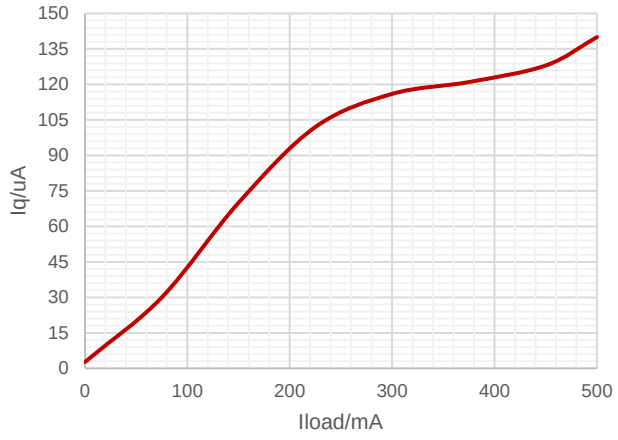


Figure 1. Quiescent Current vs Output Current

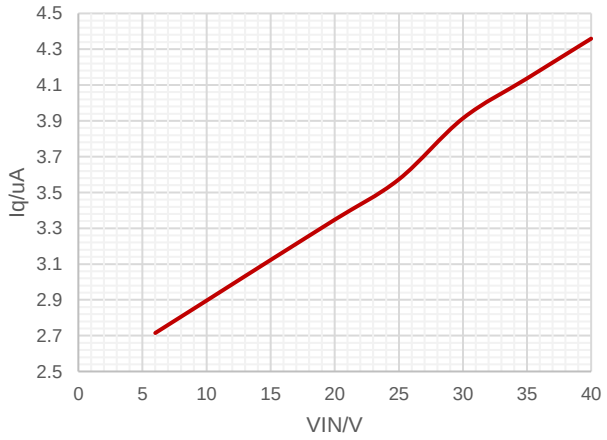


Figure 2. Quiescent Current vs Input Voltage, No load

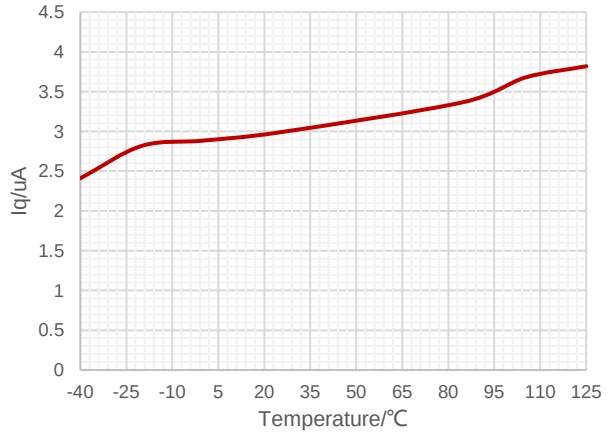


Figure 3. Quiescent Current vs Ambient Temperature

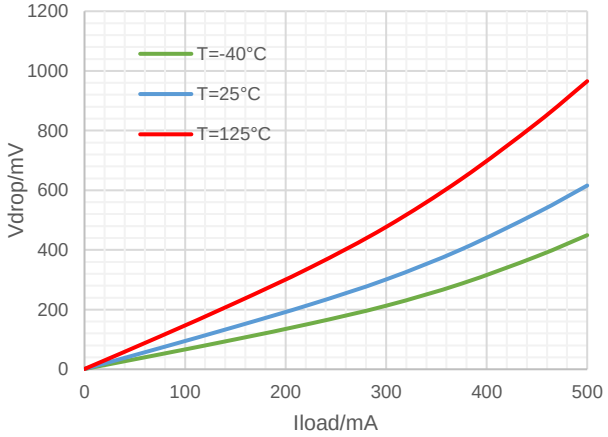


Figure 4. Dropout Voltage vs Output Current

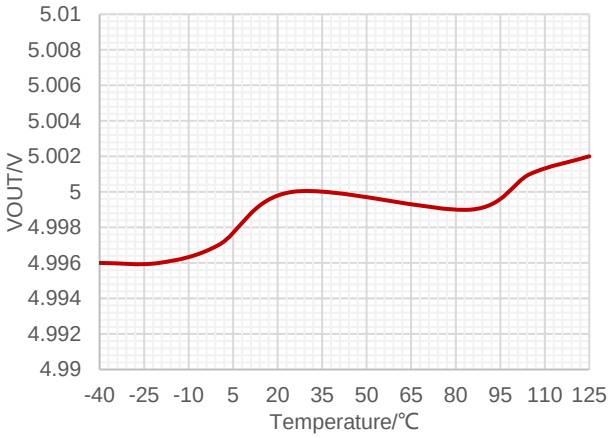


Figure 5. Output Voltage vs Ambient Temperature at VOUT=5V

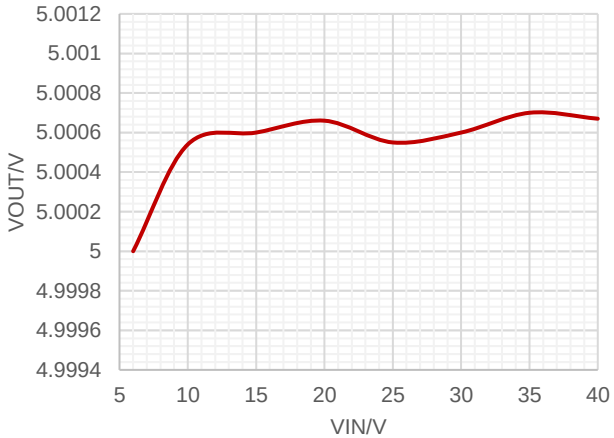


Figure 6. Output Voltage vs Input Voltage

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TYPICAL CHARACTERISTICS (continued)

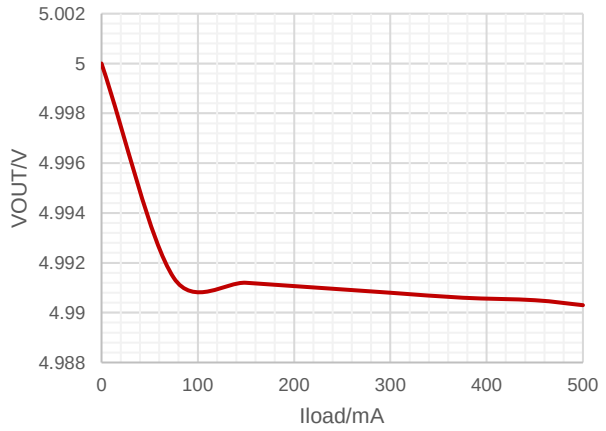


Figure 7. Output Voltage vs Output Current

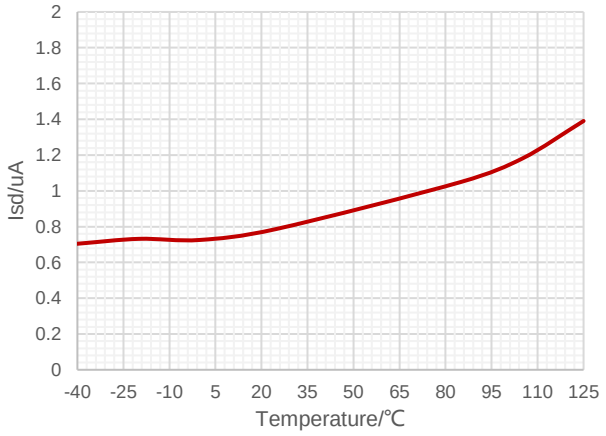


Figure 8. Shutdown Current vs Ambient Temperature

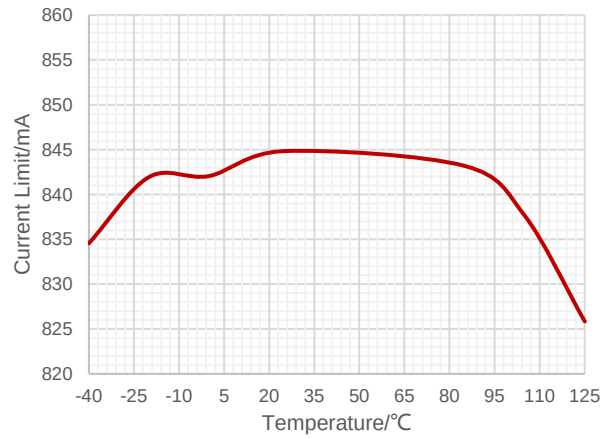


Figure 9. Output Current Limit vs Ambient Temperature at VIN<30V

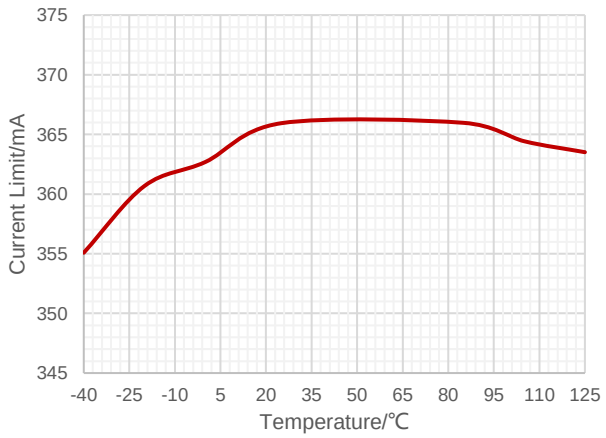


Figure 10. Output Current Limit vs Ambient Temperature at VIN≥30V

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TYPICAL CHARACTERISTICS (continued)

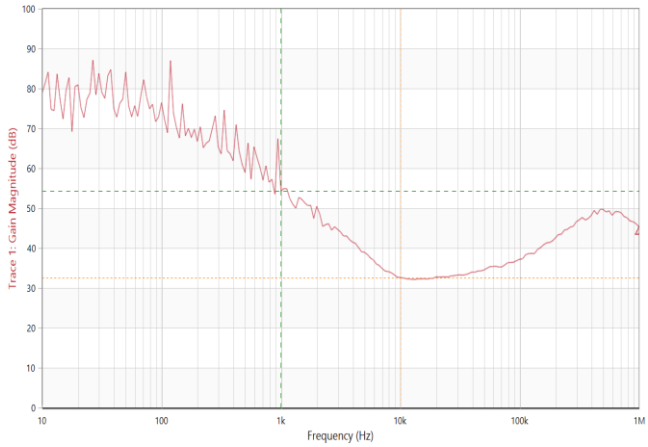


Figure 11. PSRR vs Frequency at Iout=10mA, C_{OUT}=4.7uF

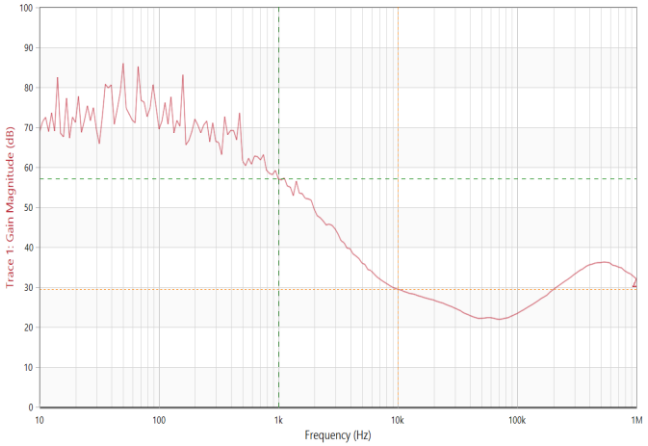


Figure 12. PSRR vs Frequency at Iout=100mA, C_{OUT}=4.7uF

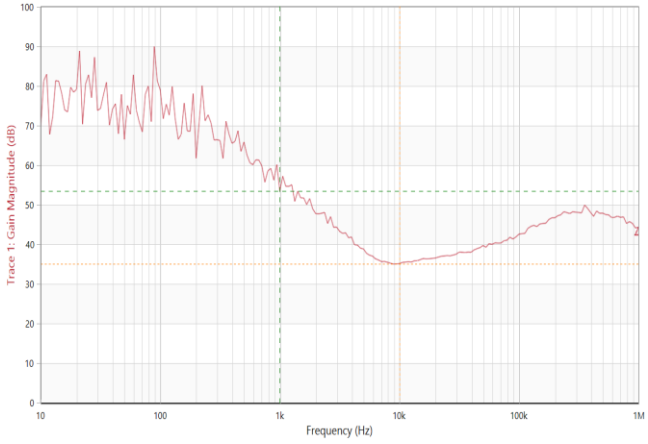


Figure 13. PSRR vs Frequency at Iout=10mA, C_{OUT}=10uF

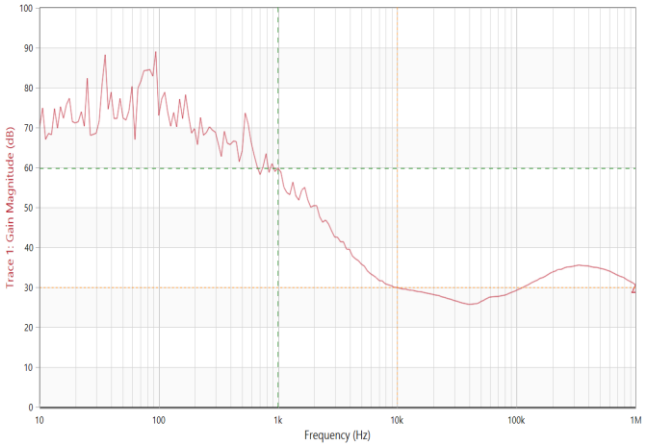


Figure 14. PSRR vs Frequency at Iout=100mA, C_{OUT}=10uF

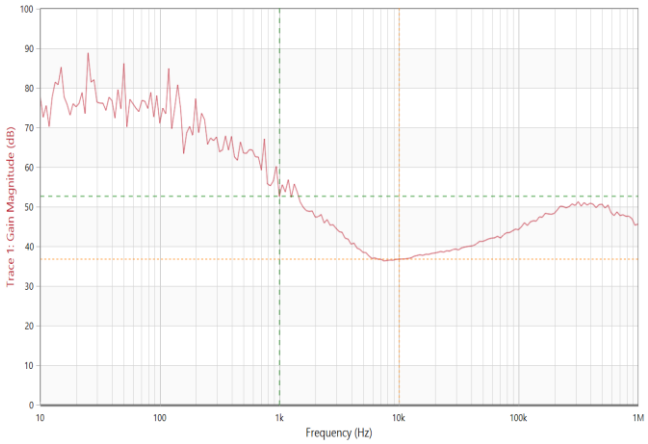


Figure 15. PSRR vs Frequency at Iout=10mA, C_{OUT}=22uF

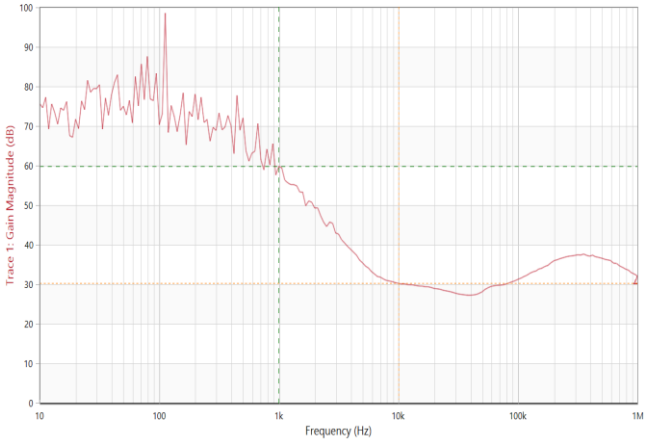


Figure 16. PSRR vs Frequency at Iout=100mA, C_{OUT}=22uF

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FUNCTIONAL BLOCK DIAGRAM

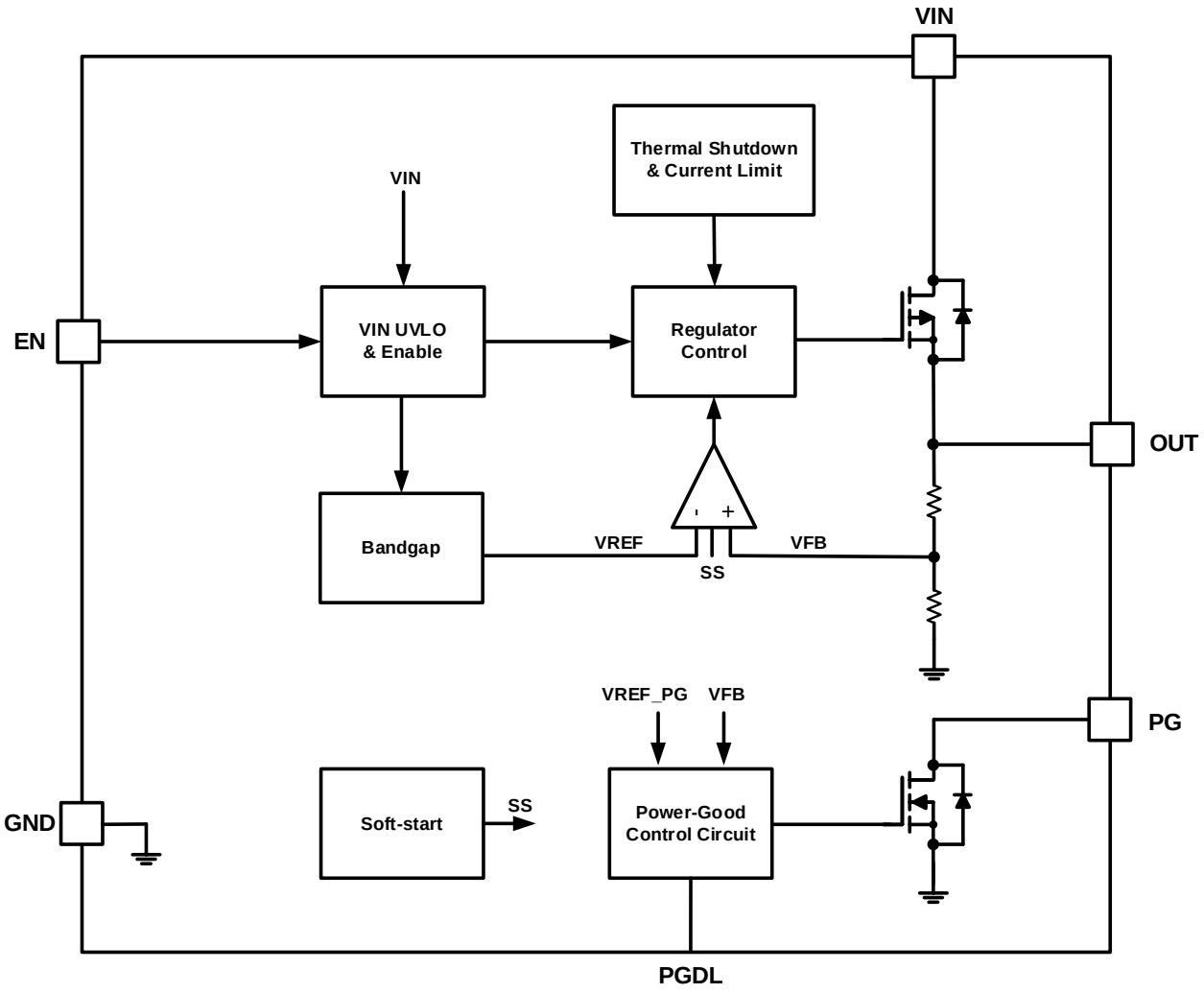


Figure 17. Fixed Output Version Functional Block Diagram

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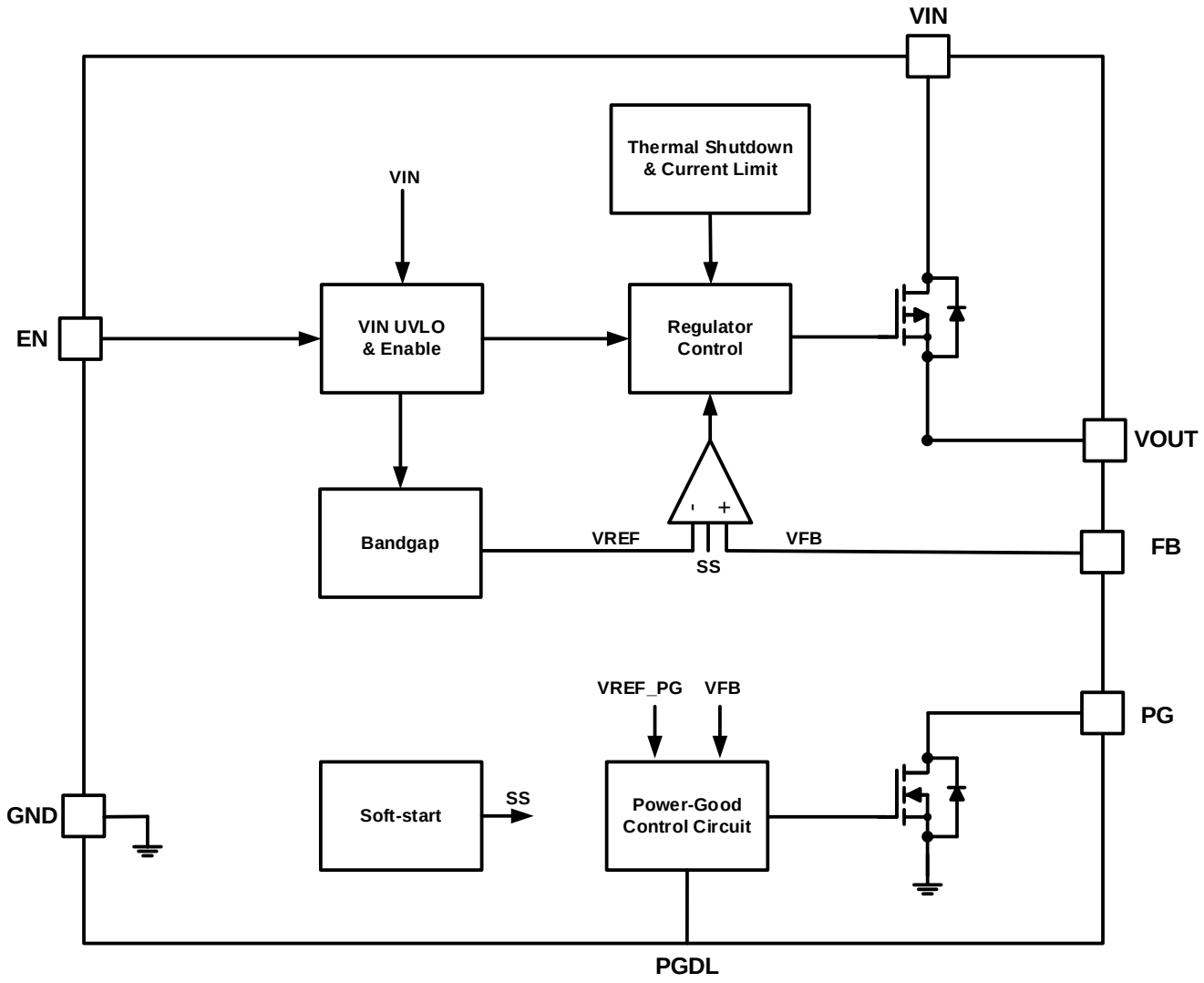


Figure 18. Adjustable Output Version Functional Block Diagram

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OPERATION

Overview

The SCT71405Q series products are 500mA wide input voltage range linear regulators with very low quiescent current. These voltage regulators operate from 3V to 40V DC input voltage with supporting 45V transient input voltage and consume 2.6μA quiescent current at no load.

The SCT71405Q series products is stable with 3.3uF~220uF output capacitors, and 10uF ceramic capacitor is recommended. An internal 1.5ms soft-start time avoids large inrush current and output voltage overshoot during startup.

The SCT71405Q series products also provide enable control, Power-Good feature and programmable Power-Good delay time which is very suitable for the applications needing sequence configuration. Other protection features include the VIN input under-voltage lockout, over current protection, output hard short protection and thermal shutdown protection.

The SCT71405Q series products are available in fixed voltage versions of 3.3V and 5V with 1% output voltage accuracy at room temp and 2% output voltage accuracy over operating conditions. The series products are available in ESOP-8L and TO252-4L packages.

The SCT71405Q series products also provide adjustable output version which can adjust the output voltage from 1.25V to 25V. If you need a new output voltage version or a new package option, please feel free to contact SCT sales.

Enable and Under Voltage Lockout Threshold

The SCT71405Q series products is enabled when the VIN pin voltage rises above 2.49V and the EN pin voltage exceeds the enable threshold V_{EN_H}. The device is disabled when the VIN pin voltage falls below 2.49V or when the EN pin voltage is below V_{EN_L}. Internal pull up current source to EN pin allows the device enable when EN pin floats.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) from VIN to GND shown in Figure 18. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$VIN_{rise} = V_{EN_H} * \frac{R1 + R2}{R2} \quad (1)$$

$$VIN_{hys} = (V_{EN_H} - V_{EN_L}) * \frac{R1 + R2}{R2} \quad (2)$$

Where

VIN_{rise}: Vin rise threshold to enable the device

VIN_{hys}: Vin hysteresis threshold

I_1=0.27uA and could be neglected in the calculation

V_{EN_H}=1.47V

V_{EN_L}=1.27V

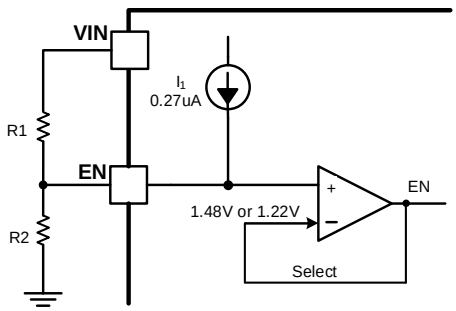


Figure 19. System UVLO by enable divide

Regulated Output Voltage

The SCT71405Q series are available in fixed voltage versions of 3.3V and 5V. When the input voltage is higher than $V_{OUT(NOM)}$+V_{DROP}, output pin is the regulated output based on the selected voltage version. When the input voltage falls below $V_{OUT(NOM)}$+V_{DROP}, output pin tracks the input voltage minus the dropout voltage based on the load current.When the input voltage drops below UVLO threshold, the output keeps shut off.

The SCT71405Q series products also provide adjustable output version which can adjust the output voltage from 1.25V to 25V. Please feel free to contact SCT sales, if you need a new output voltage version or a new package

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option.

Over Current Limit and Foldback Current Limit

The SCT71405Q series products has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is 700mA when VIN<30V, but SCT71405Q supplies a fold-back current limit 430mA when VIN>30V.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the regulator begins to heat up because of the increase in power dissipation. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition persists, the device cycles between current limit and thermal shutdown.

With the over current VIN_HIGH Control feature, the SCT71405Q series products would be more robust and safer when over current faults and shorting events occur. But it also requires the maximum loading current should be smaller than Isc during startup. The characteristic is shown in the following figure.

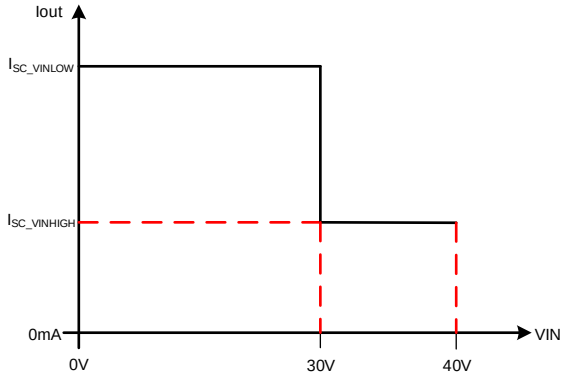


Figure 20. Current Limit with Foldback Feature

Internal Soft-Start

The SCT71405Q series products integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 0.6V reference voltage in 1.5ms. If the EN pin is pulled below 1.27V, LDO will be shut off and the internal soft-start resets. The soft-start also resets during shutdown due to thermal overloading.

Below figure shows the startup waveform at small output capacitor and large output capacitor. When output capacitor is small, for example 10uF, the slope of VOUT is limited by soft-start. When output capacitor is large, for example 100uF, the slope of VOUT is limited by current limit (I_{SC_VINLOW}) at VIN<30V, and the slope of VOUT is limited by current limit ($I_{SC_VINHIGH}$), when VIN> 30V.

In SCT71405Q series products, typical Tss is 1.5ms, and typical I_{SC_VINLOW} is 700mA and typical $I_{SC_VINHIGH}$ is 430mA, could use the following formula for initial startup time calculation.

$$\text{Tstart} = \max\left\{\frac{C_{OUT}\times V_{OUT}}{(I_{sc}-I_{load})}, T_{SS}\right\} \quad (3)$$

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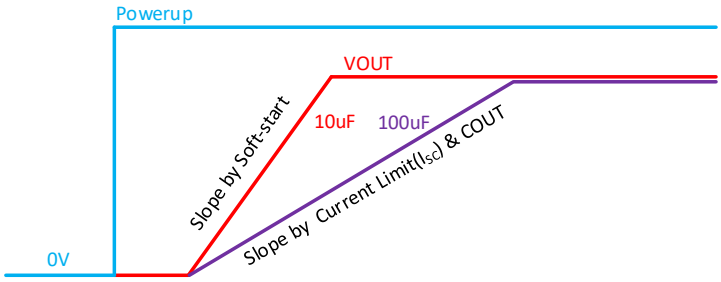


Figure 21. Soft-start Waveform vs Output Capacitor

Power-Good and Power-Good Delay

The power-good (PG) pin is an open-drain output and can be connected to any 5V or lower rail through an external pull-up resistor. The PG output is high-impedance when VOUT is greater than the PG trip threshold (he following text takes ESOP-8L package as an example, V_{PG_R}=92% x $V_{OUT(NOM)}$). If VOUT drops below V_{PG_F}=86% x $V_{OUT(NOM)}$, the open-drain output turns on and pulls the PG output low. If output voltage monitoring is not needed, the PG pin can be left floating or connected to GND.

The power-good delay time ($Td_{_PGR}$) is defined as the time period from when V_{OUT} exceeds the PG trip threshold voltage (V_{PG_R}) to when the PG output is high. This power-good delay time is set by an internal time, which is 220us typical. The power-good deglitch time ($Td_{_PGF}$) is defined as the time period from when V_{OUT} fall below the PG trip threshold voltage (V_{PG_F}) to when the PG output is low. This power-good deglitch time is set by an internal time, which is 6.6us typical. This delay time can be programmed by adding a capacitor on PGDL. To select a capacitor for PGDL, use the equation 4:

$$C_{PGDL} = \frac{t_{PGDL} * I_{PGDL}}{V_{PGDL}} \quad (4)$$

where:

- t_{PGDL} is the desired delay time for PG rising.
- I_{PGDL} is the PGDL charging current.
- V_{PGDL_R}=1.77V.

To ensure proper operation of the power-good feature, maintain $V_{IN} \geqslant$ 3V (V_{IN_MIN}). It allows connections of PG pin to circuit with the same or different power supply voltage to the LDO's VOUT level. Below are the connections examples.

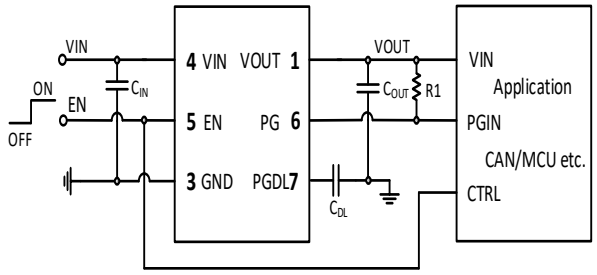


Figure 22. PG Connected to LDO's Ouput

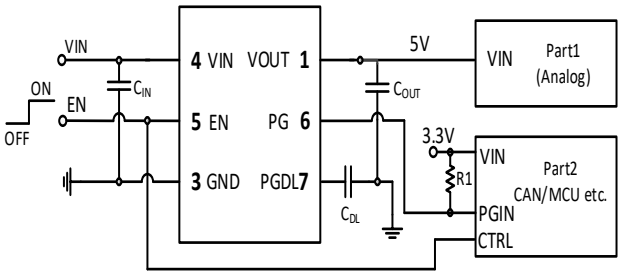


Figure 23. PG Connected to the other Power Supply

Below figure shows the startup and shutdown situation when slow power up and power down.

At the point 0, the input voltage starts to rise from 0 to 6 V, LDO is in shutdown (because VIN is below its UVLO

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threshold) and output voltage is 0V.

At the point 1, the VIN voltage reaches UVLO threshold level and LDO starts charging of output capacitor. VOUT rising speed is defined by internal soft-start function.

At the point 2, the VOUT voltage reaches almost the VIN voltage as it rises faster and LDO gets into dropout region. The difference between VIN and VOUT is the dropout voltage.

At the point 3, the VOUT reaches PG threshold (V_{PG_R}=92% x $V_{OUT(NOM)}$) and from this point LDO counts the power good delay time ($Td_{_PGR}$). After this delay, the PG pin rises to high level showing that VOUT is ok.

At the point 4, the VOUT reaches its nominal value (5.0V) as the VIN starts to be higher than ($V_{OUT(NOM)}$ + V_{DROP}) and LDO gets into regulation region.

At the point 5, as the VIN voltage slow power down and LDO returns to dropout region again.

At the point 6, the VOUT drops below PG threshold (V_{PG_F}=86% x $V_{OUT(NOM)}$) and LDO starts counting the power good deglitch time ($Td_{_PGF}$), which filters fast VOUT undershoots (caused for example by line/load transient responses). After this delay, the PG output is shorted to 0 V level to highlight “power fail” state.

At the point 7, the VIN voltage is lower than input voltage UVLO threshold minus UVLO hysteresis level and LDO goes into the shutdown state.

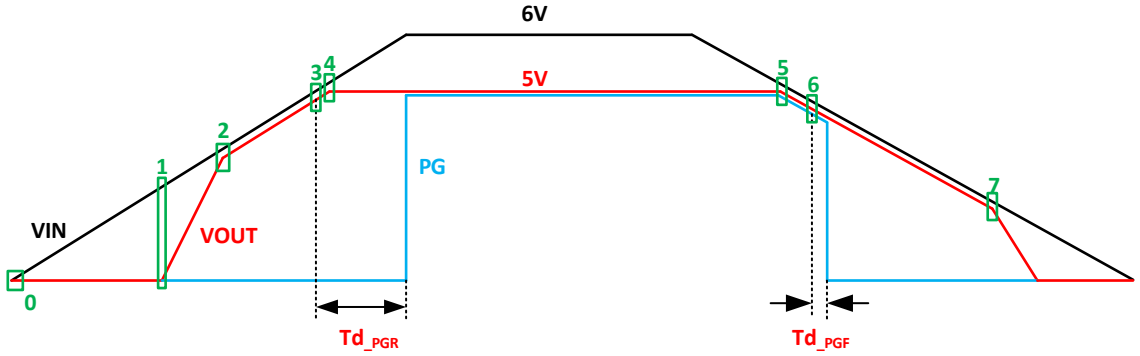


Figure 24. Startup and Shutdown Example —SCT71405Q Series

Thermal Shutdown

This device incorporates a thermal shutdown (T_{SD}) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the T_{SD} trip point. The junction temperature exceeding the T_{SD} trip point causes the output to turn off. When the junction temperature falls below the T_{SD} trip point minus thermal shutdown hysteresis, the output turns on again.

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APPLICATION INFORMATION

Typical application 1:

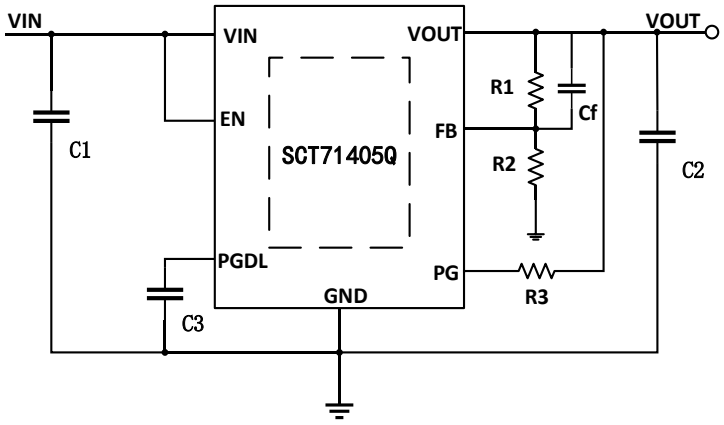


Figure 25. SCT71405Q Typical Application Schematic

Design Parameters

Design Parameters	Example Value
Input Voltage	12V Normal, 3V~40V
Output Voltage	5V Normal,1.25V~25V
Maximum Output Current	500mA
Output Capacitor Range (C_2)	3.3uF~220uF , recommends 10uF
Input Capacitor Range (C_1)	>2.2uF , recommends 10uF
Pull-up resistor of power-good (R3)	10kΩ~100kΩ

Typical application 2:

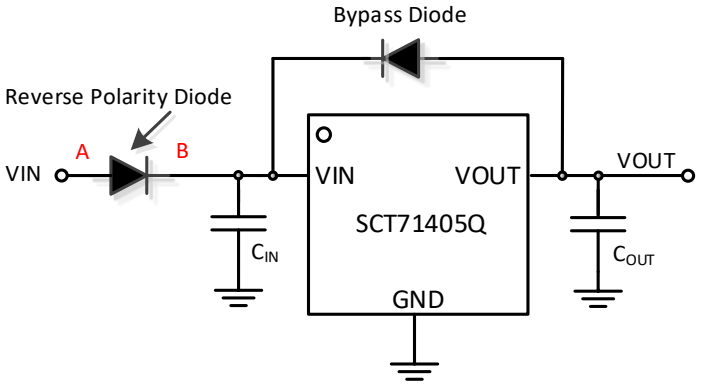


Figure 26. SCT71405Q Typical Application Schematic with Reverse Polarity Diode

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Design Parameters

Design Parameters	Example Value
Input Voltage	12V Normal, 3V~40V
Output Voltage	5V Normal, 1.25V~25V
Maximum Output Current	500mA
Output Capacitor Range (C_{OUT})	3.3uF~220uF , recommends 10uF
Input Capacitor Range (C_{IN})	>2.2uF , recommends 10uF

In some applications, the VIN and the VOUT potential might be reversed, possibly resulting in circuit internal damage or damage to the elements. For example, the accumulated charge in the output pin capacitor flowing backward from the VOUT to the VIN when the VIN shorts to the GND. In order to minimize the damage in such case, use a capacitor with a capacitance less than 220μF. Also by inserting a reverse polarity diode in series to the VIN, it can prevent reverse current from reverse battery connection or the case, when the point A is short-circuited GND. If there may be any possible case point B is short-circuited to GND, we also recommend using a bypass diode between the VIN and the VOUT.

Typical application 3:

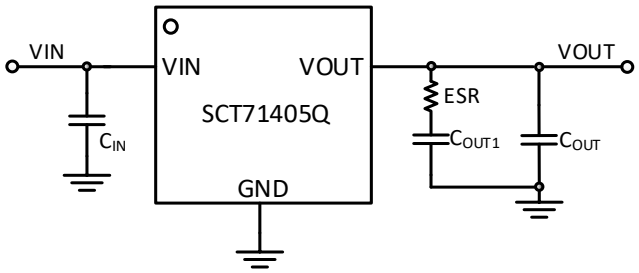


Figure 27. SCT71405Q Typical Application Schematic with Large Output Capacitor

Design Parameters

Design Parameters	Example Value
Input Voltage	12V Normal, 3V~40V
Output Voltage	5V Normal, 1.25V~25V
Maximum Output Current	500mA
Output Capacitor Range (C_{OUT1} and ESR)	3.3uF~220uF with ESR=0.5Ω~5Ω
Output Capacitor Range (C_{OUT2})	recommends 10uF with low ESR
Input Capacitor Range (C_{IN})	>2.2uF , recommends 10uF

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Output Voltage

For adjustable output version the output voltage is set by an external resistor divider R1 and R2 in typical application schematic. Recommended R2 resistance is 100KΩ. Use equation 5 to calculate R1.

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_2 \quad (5)$$

where:

- V_{REF} is the feedback reference voltage, typical 1.25V

Table 1: Compensation Values for Typical Output Voltage/Capacitor Combinations

Vout/V	COUT/uF	Cf/pF	R1/KΩ	R2/KΩ	COUT1/uF (optional)	ESR/Ω
1.8	33	68	48.7	100	220	1
2.5	33	33	105	100	220	1
3.3	15	22	174	100	220	1
5	15	10	309	100	220	1
12	15	3.3	887	100	220	1

Input Capacitor and Output Capacitor

SCT recommends adding a 2.2μF or greater capacitor with a 0.1μF bypass capacitor in parallel at VIN pin to keep the input voltage stable. Aluminum electrolytic capacitor or other capacitor with high capacitance is suggested for the system power with large voltage spike. The voltage rating of the capacitors must be greater than the maximum input voltage

To ensure loop stability, the SCT71405Q series products requires an output capacitor with a minimum effective capacitance value of 3.3μF. And the series products could support output capacitor range from 3.3uF to 220uF and with an ESR range between 0.001Ω and 5Ω. SCT recommends selecting a X5R- or X7R-type 4.7uF~10uF ceramic capacitor with low ESR over temperature range to improve the load transient response.

When using large output capacitor with higher ESR resistor, for example 100uF output electrolytic capacitor with 1Ω ESR resistor in the application, SCT recommends adding extra 10uF low ESR output capacitor parallel connection with the large electrolytic capacitor, this will eliminate the undershoot/overshoot voltage caused by the large ESR resistor and get better load transient performance.

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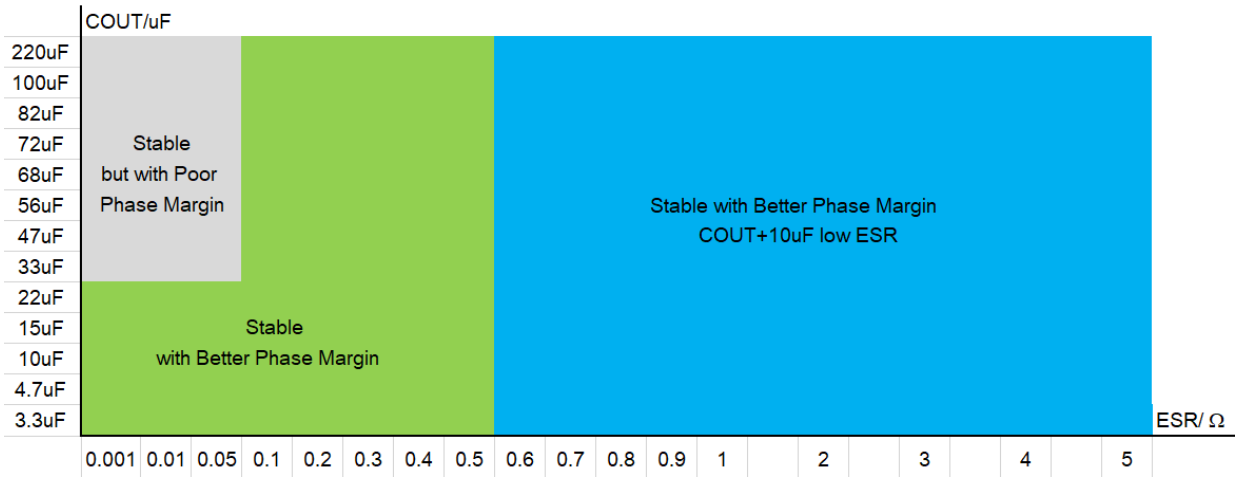


Figure 28. SCT71405Q Stability VS Output Capacitor

Power Dissipation and Thermal Performance

Power dissipation caused by voltage drop across the LDO and by the output current flowing through the device needs to be dissipated out from the chip. The maximum junction temperature is dependent on power dissipation, package, the PCB layout, number of used Cu layers, Cu layer thickness and the ambient temperature.

During normal operation, LDO junction temperature should not exceed 150°C, or else it may result in deterioration of the properties of the chip. Using below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using Equation 6. Because I_{GND} « I_{OUT}, the term V_{IN} x I_{GND} in Equation 6 could be ignored.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (6)$$

The junction temperature can be estimated using Equation 7. $R_{\theta JA_EVM}$ is the junction-to-ambient thermal resistance based on customer's PCB. Verify the application and allow sufficient margins in the thermal design by the following method is used to calculate the junction temperature T_J.

$$T_J = T_A + P_D \times R_{\theta JA_EVM} \quad (7)$$

$R_{\theta JA_EVM}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature/flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

For the SCT71405Q series products, the maximum allowable power dissipation of different packages was listed in the following table, and the test results are based on our EVM board, larger power dissipation will trigger thermal shutdown protection. As a result, we could calculate the $R_{\theta JA_EVM}$ of different packages. The following table is just for your reference based on our EVM test, please leave enough margin when you design thermal performance.

The PCB information of our EVM: 4-layer, both the inner and outer layers are 1oz Cu, 50mm x 30mm size.

Thermal Performance of Different Packages Based on EVM Test

Package(4-layer)	Max Allowable PD (W) (Not Trigger TSD,VOUT=5V)	Max Allowable PD (W) (TJ≤125℃)	$R_{\theta JA_EVM}$ (℃/W)
ESOP-8L	4.517	3.011	33.21
Package(4-layer)	**Max Allowable PD (W) (Not Trigger TSD,VOUT=5V)**	**Max Allowable PD (W) (TJ≤125℃)**	**$R_{\theta JA_EVM}$ (℃/W)**
TO252-4L	6.193	4.129	24.22

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THERMAL CHARACTERISTICS

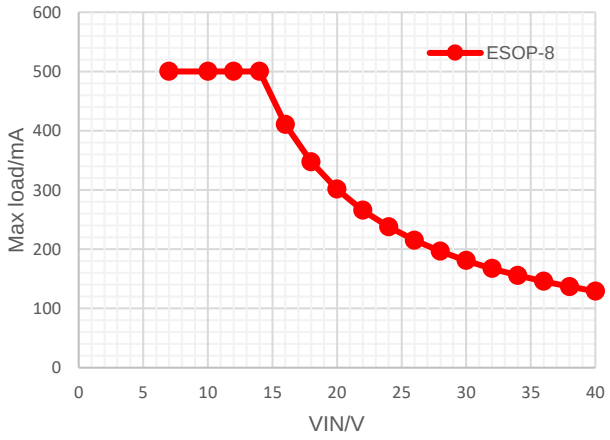


Figure 29. Maximum Output Current vs Input Voltage, VOUT=5V of ESOP-8L ,T_J ≤ TSD_R(4-layer EVM)

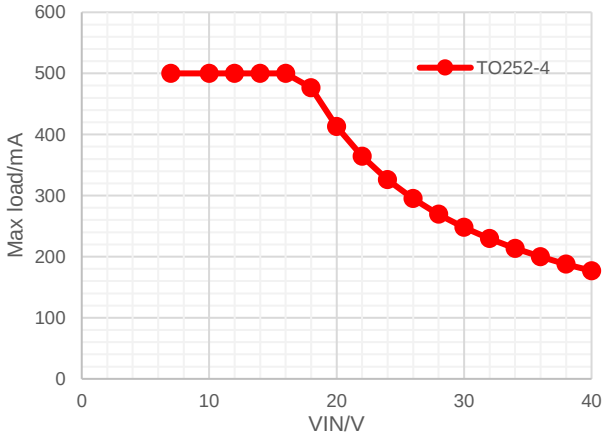


Figure 30. Maximum Output Current vs Input Voltage, VOUT=5V of TO252-4L ,TJ ≤ TSD_R(4-layer EVM)

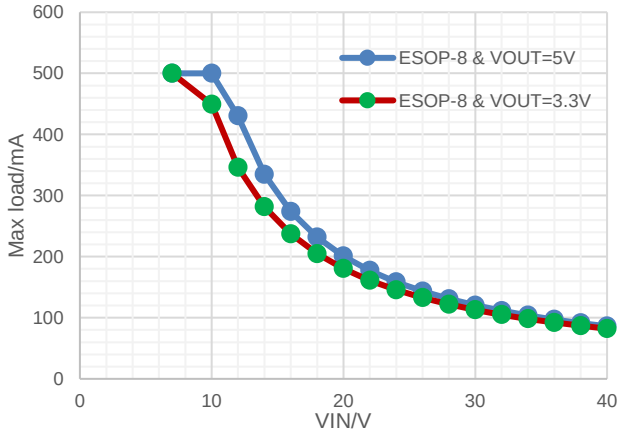


Figure 31. Maximum Output Current vs Input Voltage, ESOP-8L,TJ ≤ 125℃(4-layer EVM)

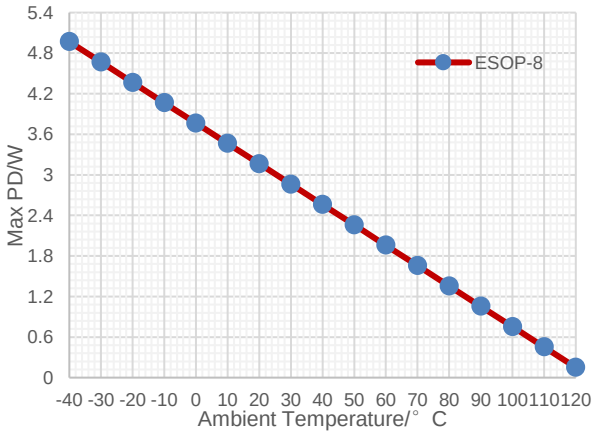


Figure 32. Maximum Allowed Power Dissipation vs Ambient Temperature, ESOP-8L,TJ ≤ 125℃(4-layer EVM)

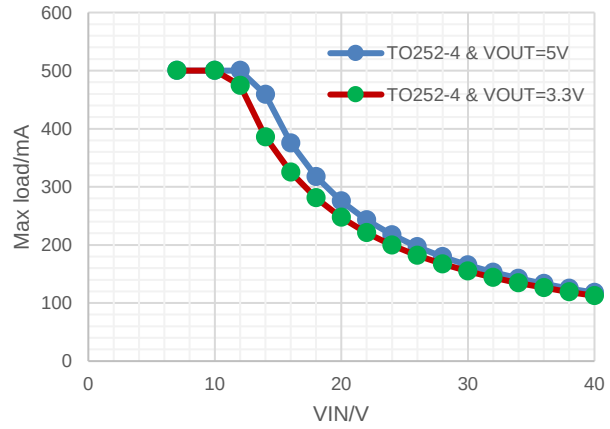


Figure 33. Maximum Output Current vs Input Voltage, TO252-4L,TJ ≤ 125℃(4-layer EVM)

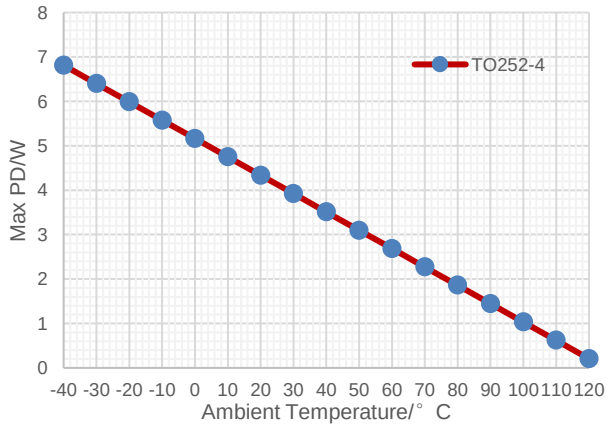


Figure 34. Maximum Allowed Power Dissipation vs Ambient Temperature, TO252-4L,TJ ≤ 125℃(4-layer EVM)

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Application Waveforms

Vin=Vout +1V, unless otherwise noted

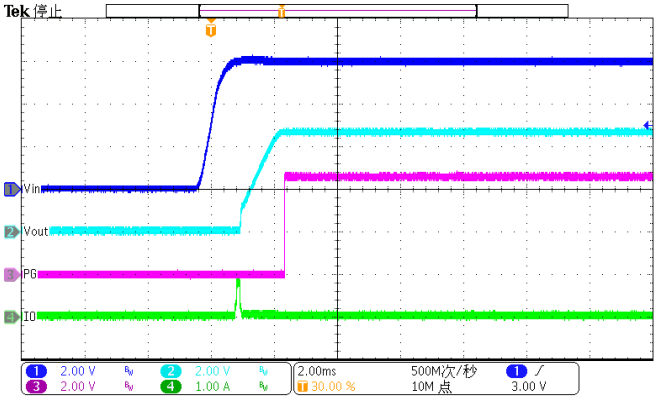


Figure 35. Power up (Iload=10mA)

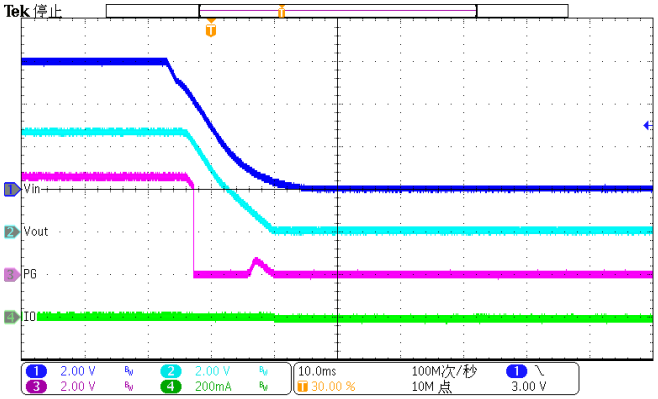


Figure 36. Power down (Iload=10mA)

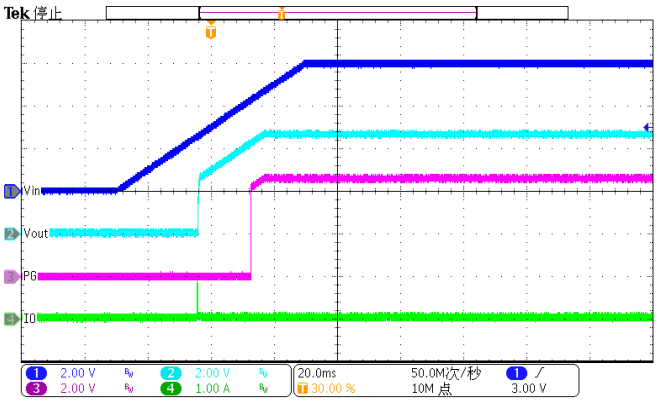


Figure 37. Slow Power up (Iload=10mA)

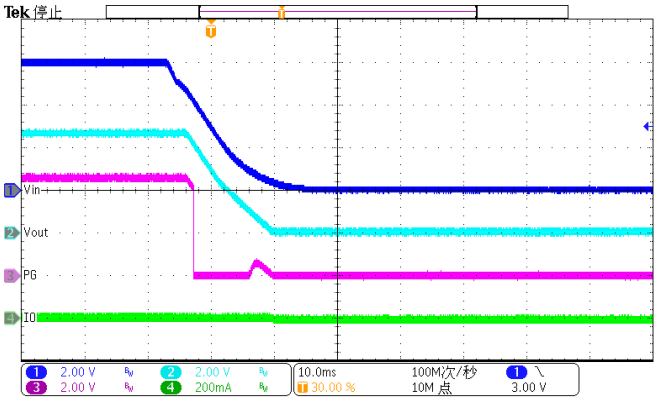


Figure 38. Slow Power down (Iload=10mA)

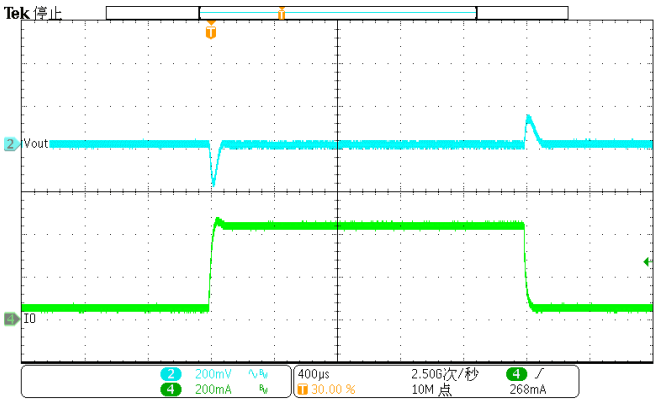


Figure 39. DC-DC Load Transient

(50mA-450mA),VOUT=5V

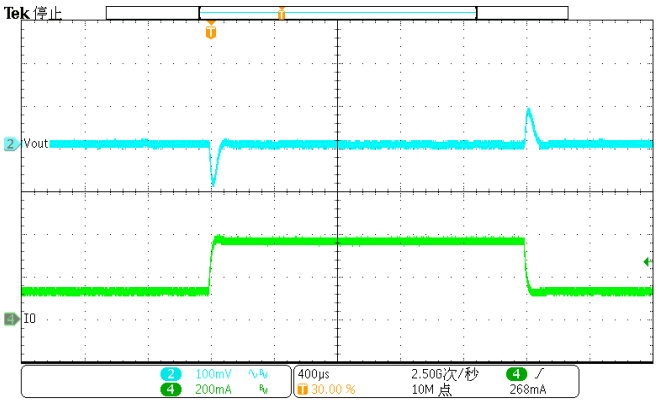


Figure 40. DC-DC Load Transient

(130mA-370mA),V_{OUT}=5V

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Application Waveforms(Continued)

Vin=Vout +1V, unless otherwise noted

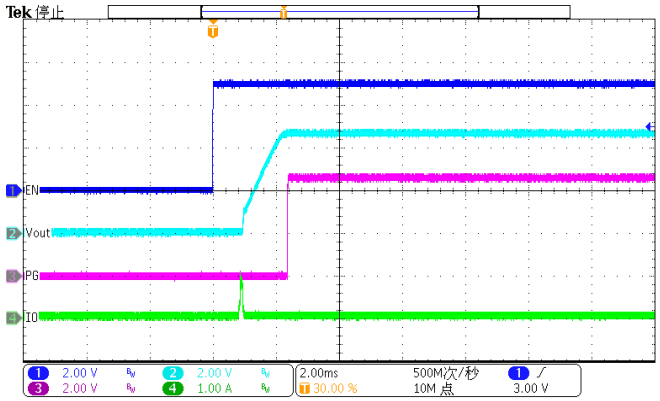


Figure 41. Enable (Iload=10mA)

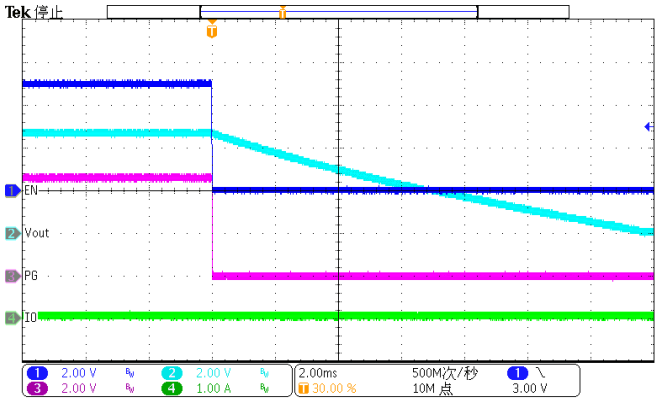


Figure 42. Disable (Iload=10mA)

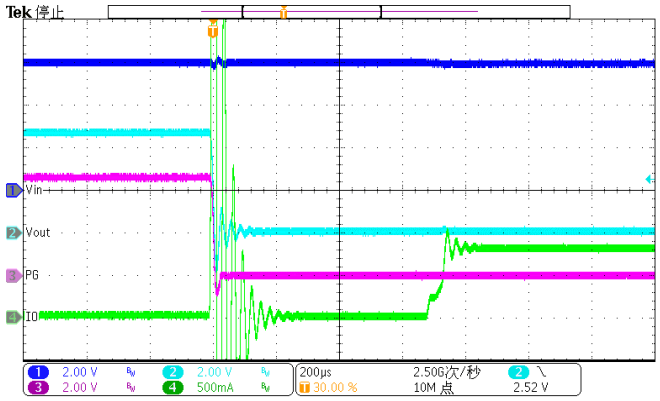


Figure 43. Enter Over Current Protection (Iload=1A)

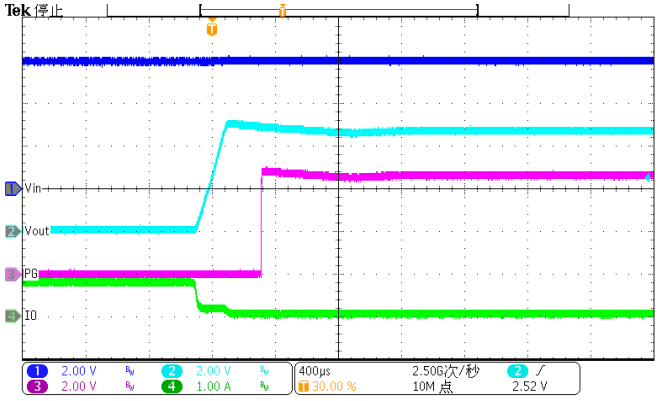


Figure 44. Exit Over Current Protection (Iload=1A)

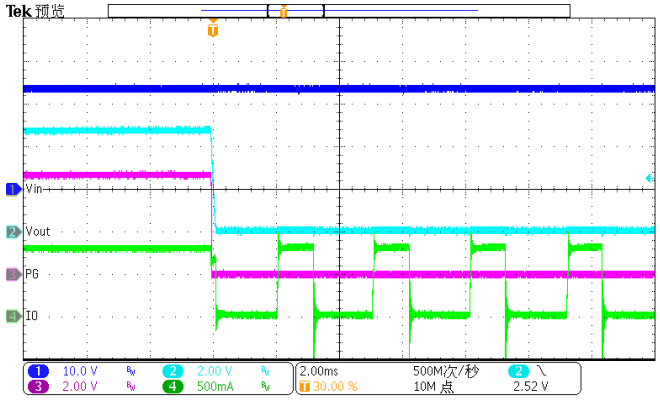


Figure 45. Enter Over Temperature Protection(Vin=24V)

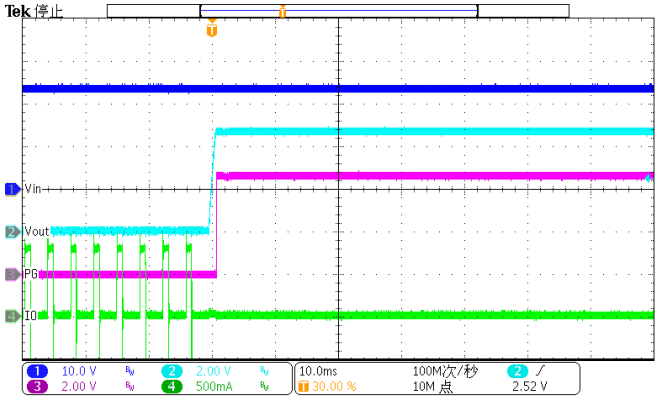


Figure 46. Exit Over Temperature Protection(Vin=24V)

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Layout Guideline

Proper PCB layout is a critical for SCT71405Q's stability, transient performance and good regulation characteristics. For better results, follow these guidelines as below:

1. Both input capacitors and output capacitors must be placed as close to the device pins as possible.
2. It is recommended to bypass the input pin to ground with a 0.1μF bypass capacitor. The loop area formed by the bypass capacitor connection, V_{IN} pin and the GND pin of the system must be as small as possible.
3. It is recommended to use wide trace lengths or thick copper weight to minimize I×R drop and heat dissipation.
4. To improve the thermal performance of the device, and maximize the current output at high ambient temperature, SCT recommends spreading the copper under the thermal pad as far as possible and placing enough thermal vias on the copper under the thermal pad.
5. If using large electrolytic capacitor with high ESR resistor, SCT recommends adding a 10uF low ESR capacitor parallel connection with the large electrolytic capacitor.

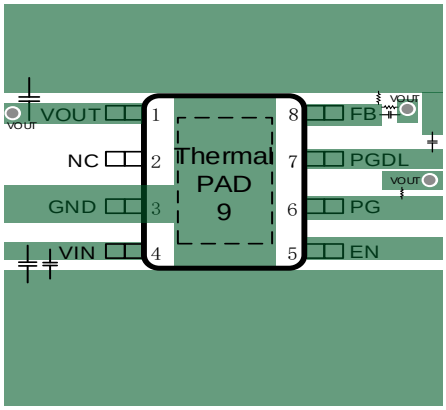


Figure 47. PCB Layout Example

SCT71405A00QSTER

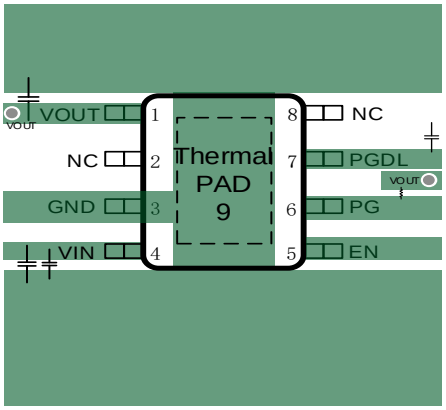


Figure 48. PCB Layout Example

SCT71405FxxBQSTER

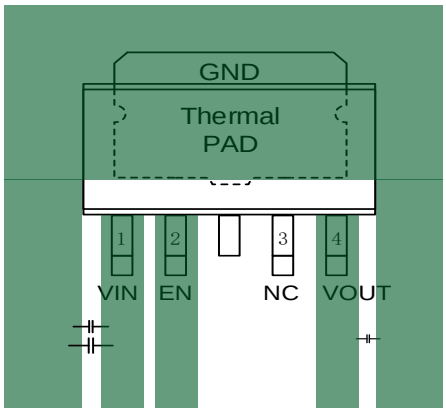


Figure 49. PCB Layout Example

SCT71405FxxQOWCR

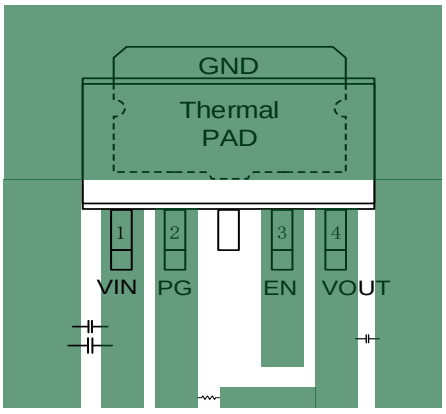


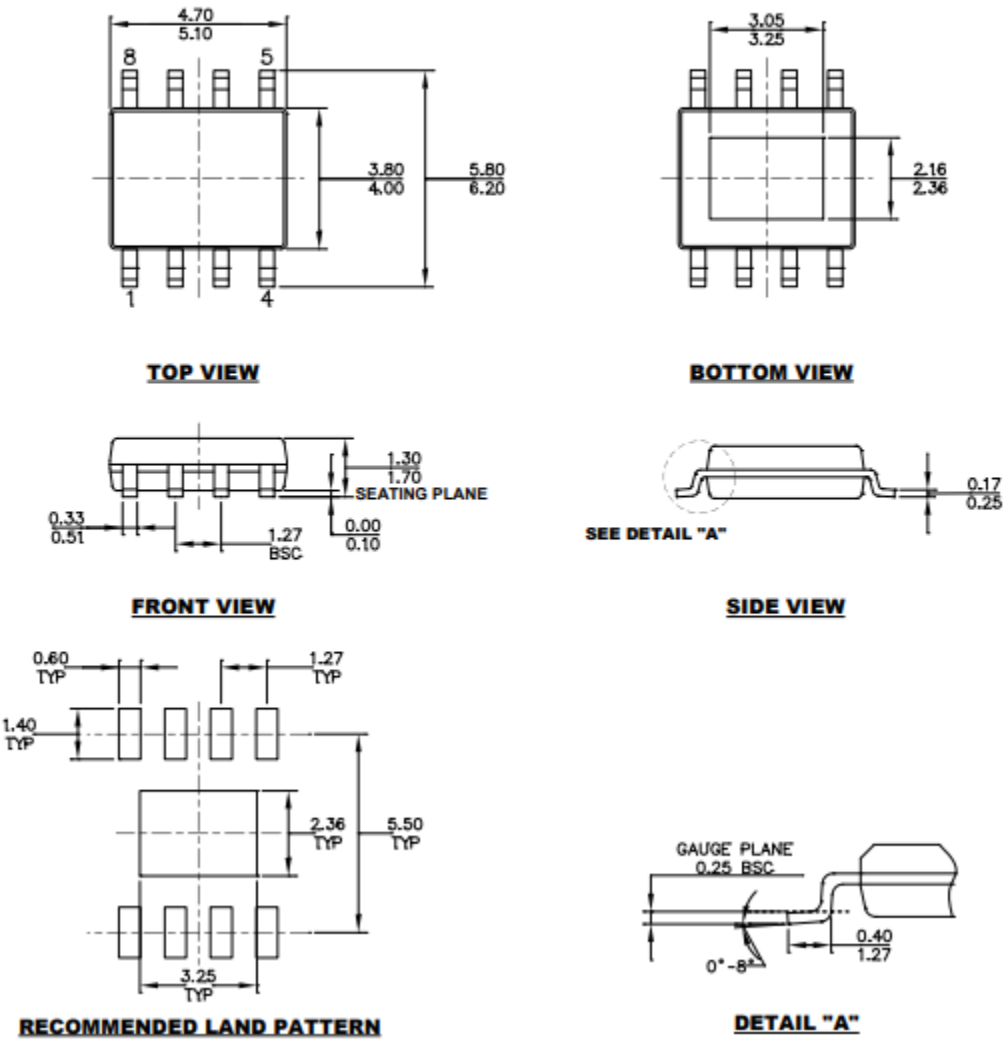
Figure 50. PCB Layout Example

SCT71405FxxAQOWCR

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PACKAGE INFORMATION

PACKAGE OUTLINE DRAWING FOR 8L SOP-EP
POD-0022 Revision 1.0



ESOP-8L Package Outline Dimensions

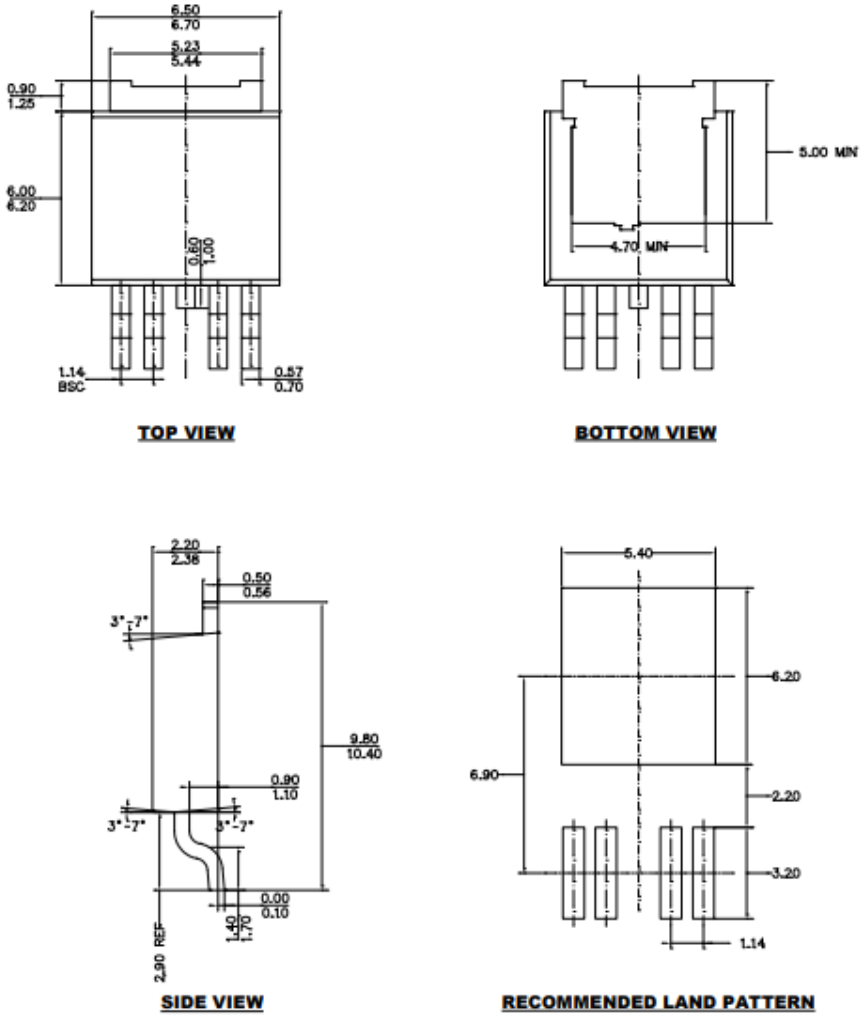
NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

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PACKAGE INFORMATION

PACKAGE OUTLINE DRAWING FOR TO252-4L
POD-0040 Revision 0.0



NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) DRAWING CONFORMS TO JEDEC TO-252.
5) DRAWING IS NOT TO SCALE.

TO252-4L Package Outline Dimensions

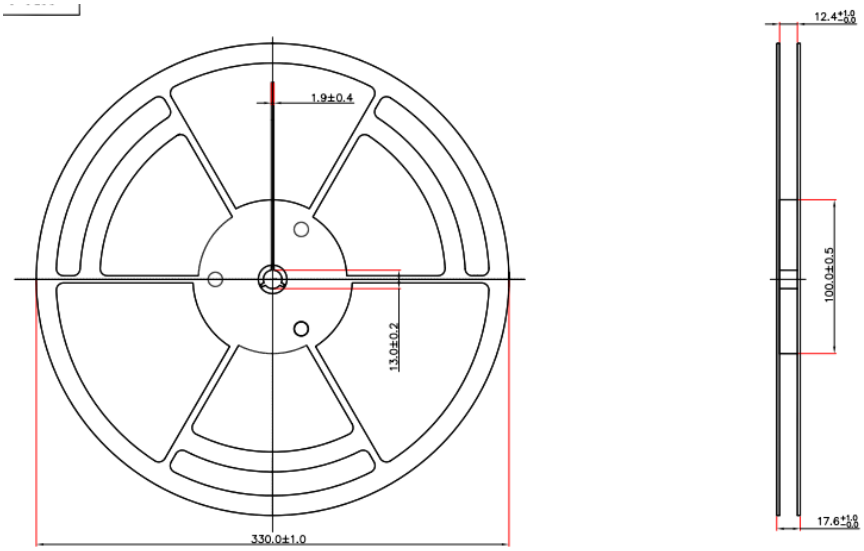
NOTE:

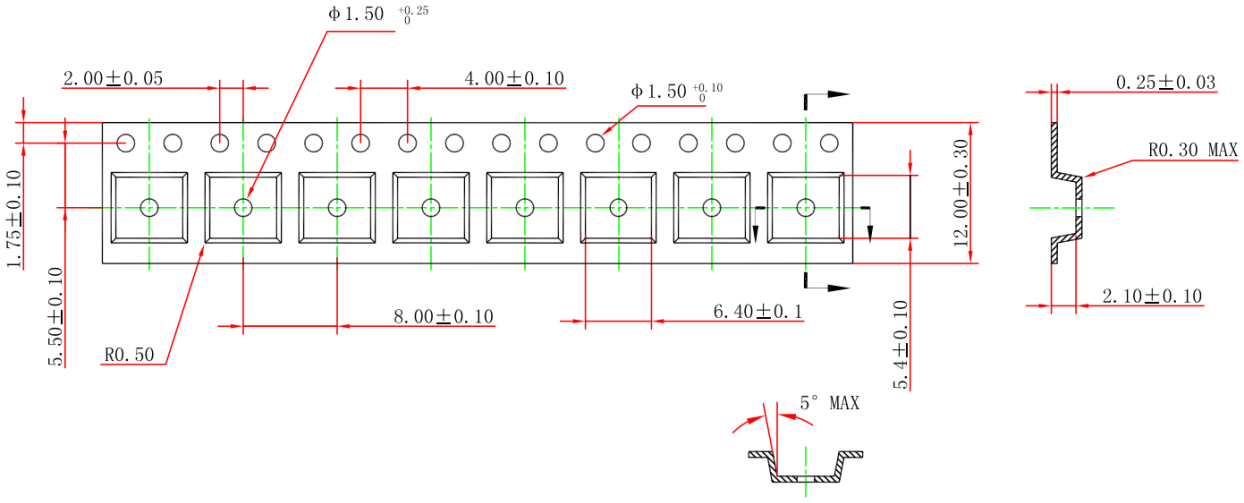
7. Drawing proposed to be made a JEDEC package outline MO-220 variation.
8. Drawing not to scale.
9. All linear dimensions are in millimeters.
10. Thermal pad shall be soldered on the board.
11. Dimensions of exposed pad on bottom of package do not include mold flash.

Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

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TAPE AND REEL INFORMATION

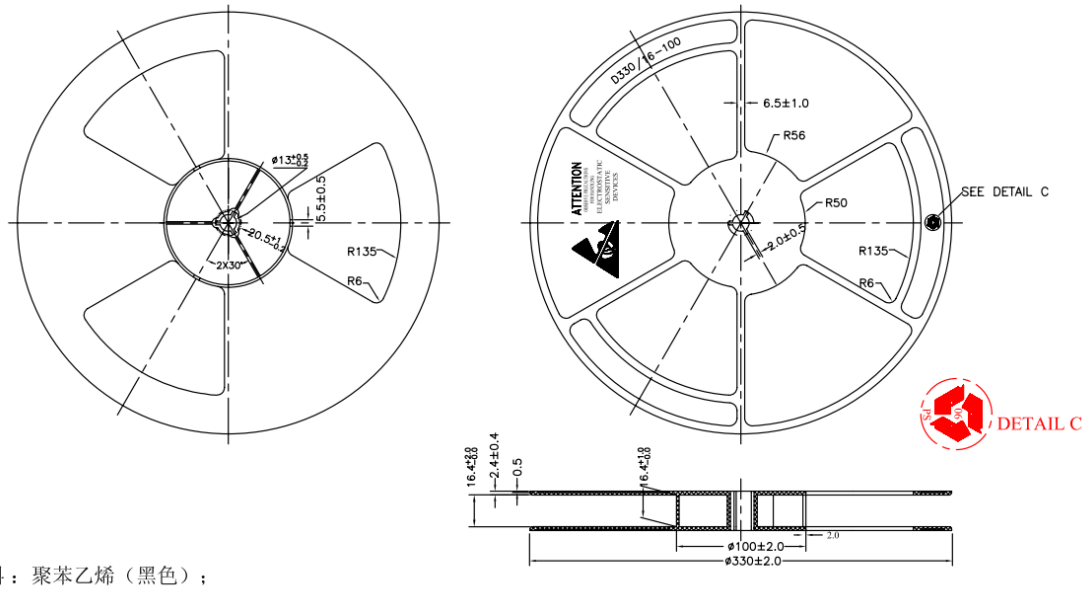




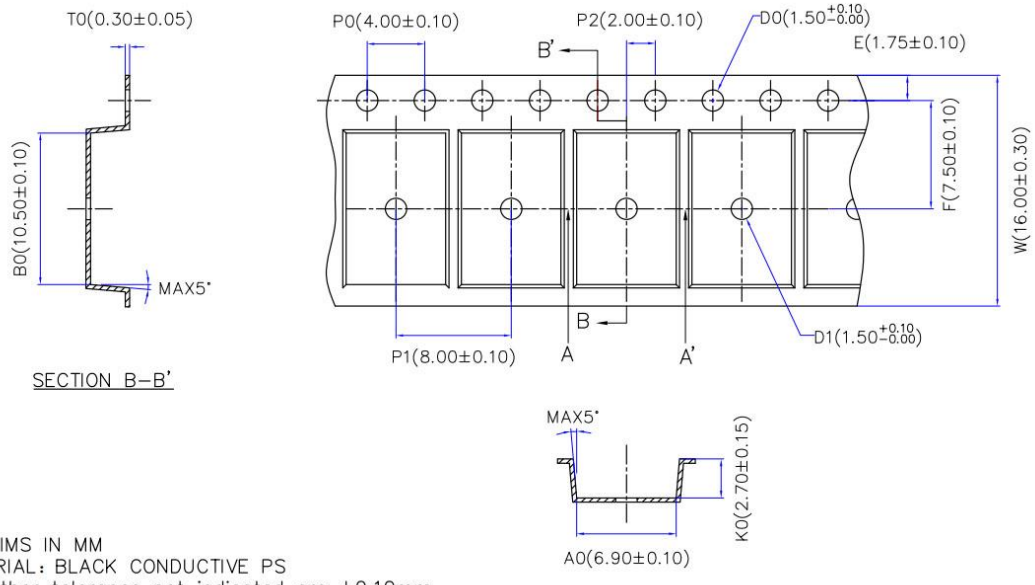
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TAPE AND REEL INFORMATION



注意：
1. 材料：聚苯乙烯（黑色）；
2. 平整度：最大允许3 毫米；
3. 所有尺寸为毫米；
4. 表面电阻： 10^5 TO 10^{11}OHMS/SQ.
5. 所有未注公差：±0.25。



NOTES:
1. ALL DIMS IN MM
2. MATERIAL: BLACK CONDUCTIVE PS
3. The other tolerance not indicated are ±0.10mm
4. 10 sprocket hole pitch cumulative tolerance ±0.20mm
5. Carrier camber is within 1mm in 250mm
6. There must not be foreign body adhesion and the state of the surface must be excellent
7. Surface resistance 1X10E5≤Rs<1X10E9 OHMS
8. Friction Voltage<100V
9. 17" PLASTIC–Reel

TO252

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