3V-17V Vin 6A Synchronous Step Down Convertor

FEATURES

- Input Voltage Range: 3V-17V
- Output Voltage Range: 0.6V-10V
- Up to 6A Continuous Output Current
- 100μA Quiescent Current
- 0.6V ±1% Feedback Reference Voltage
- Integrated 42mΩ High-Side and 23mΩ Low-Side Power MOSFETs
- 550kHz Switching Frequency
- Fixed 1.5ms Soft-start Time
- PFM Operation at Light Load (SCT2263)
- FCCM Operation at Light Load (SCT2264)
- Cycle-by-cycle Current Limit
- Input Under-voltage Lockout
- Output Under-voltage Protection
- Over Temperature Protection
- Available in a TSOT23-6L Package

APPLICATIONS

- High-End DTV
- Set-top Box, xDSL Modem, Personal Video Recorders
- Server, Cloud-Computing, Storage
- Telecom & Networking, Small-cell Base Stations, Point-of-Load (POL), IPCs, Factory Automation, PLC, Test Measurement

DESCRIPTION

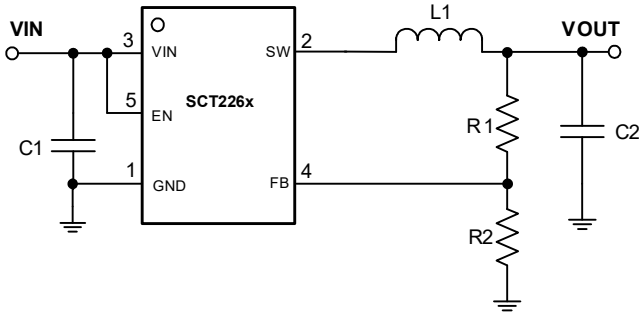
The SCT226x is a fully integrated high efficiency synchronous step-down DCDC converter capable of delivering 6A current. The devices operate over a wide input voltage range from 3V to 17V and fully integrate high-side power MOSFETs and synchronous MOSFETs with low Rdson to minimize the conduction loss.

The SCT226x adopts Constant On-Time (COT) control architecture to achieve fast load transient responses for step-down applications. With 550kHz fixed switching frequency, low output voltage ripple, small external inductor are achieved.

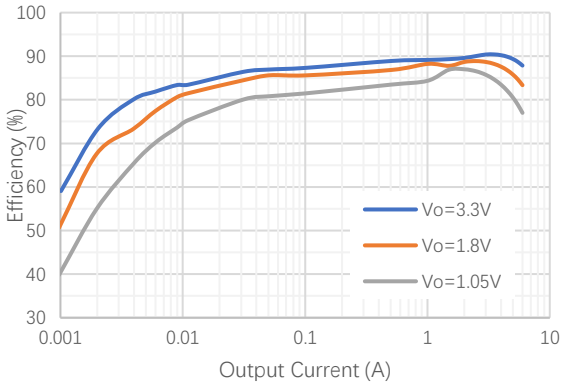
The SCT2263 operates in PFM mode, which maintains high efficiency during light load operation. The SCT2264 operates in FCCM mode, which achieves smaller output voltage ripple compared with PFM at light load. It includes full protection features, such as over current protection, output under-voltage protection, input under-voltage lockout, and thermal shutdown.

The SCT226x requires a minimal number of external components and is available in a space-saving TSOT23-6L package.

TYPICAL APPLICATION



3V-17V, Synchronous Buck Converter



Efficiency, Vin=12V, PFM mode

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Released to market.

DEVICE ORDER INFORMATION

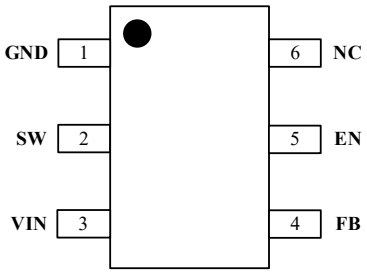
ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL
SCT2263TVBR	Tape & Reel	5000	2263	6	TSOT23-6L	3
SCT2264TVBR	Tape & Reel	5000	2264	6	TSOT23-6L	3

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted (1)

DESCRIPTION	MIN	MAX	UNIT
VIN, EN	-0.3	18	V
FB	-0.3	6	V
SW	-1	VIN+0.3	V
SW(<10ns)	-2.5	VIN+1	V
Operating junction temperature T_J(2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

PIN CONFIGURATION



Top View: TSOT23-6L

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
GND	1	Power ground. Must be soldered directly to the ground plane.
SW	2	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
VIN	3	Power supply input. VIN supplies the power to the IC, as well as the step-down converter switches. Drive VIN with a 3V to 17V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
FB	4	Buck converter output feedback sensing voltage. Connect a resistor divider from VOUT to FB to set up output voltage. The device regulates FB to the internal reference of 0.6V typical.
EN	5	Enable logic input. EN pin default pulls down to GND with 2MΩ resistor, Pulling the pin high enables the device. The device has precision enable thresholds 1.2V rising/1V falling for programmable UVLO threshold and hysteresis.
NC	6	NC pin.

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RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3	17	V
V_{OUT}	Output voltage range	0.6	10	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)	-2	+2	kV
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins (1)	-1	+1	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	TSOT23-6L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance (1)	80.9	°C/W
$R_{\theta JCtop}$	Junction to case thermal resistance (1)	61.6	
Ψ_{JT}	Junction-to-top characterization parameter (1)	5.1	
Ψ_{JB}	Junction-to-board characterization parameter (1)	15.5	
$R_{\theta JB}$	Junction-to-board thermal resistance (1)	16.1	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT226x is mounted and external environmental factors. The PCB board is a heat sink that is soldered to the leads of the SCT226x. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

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ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		3		17	V
V_{IN_UVLO}	Input UVLO	V_{IN} rising	2.74	2.9	2.98	V
	Hysteresis			200		mV
I_{SD}	Shutdown current	EN=0V		1.5	7	uA
I_Q	Quiescent current from VIN	no load, no switching, PFM mode		100	150	uA
		no load, no switching, FCCM mode		300	400	uA
		Vo=1.8V, L=1uH, no load and switching(1), PFM mode		124		uA
Reference						
V_{FB}	Reference voltage of FB	Tj=25°C	0.594	0.6	0.606	V
		Tj=-40°C~125°C	0.591	0.6	0.609	V
I_{FB}	FB pin leakage current				100	nA
Power MOSFETs						
R_{HS}	High-side switch on resistance			42	65	mΩ
R_{LS}	Low-side switch on resistance			23	35	mΩ
Switching Frequency						
F_{SW}	Switching frequency		450	550	650	kHz
t_{ON_MIN}	Minimum on-time			90		ns
t_{OFF_MIN}	Minimum off-time			150		ns
Enable and Soft-start						
V_{ENH}	High-level threshold voltage		1.13	1.2	1.27	V
V_{ENL}	Low- level threshold voltage		0.93	1	1.07	V
R_{EN}	EN Pull down resistance			2		MΩ
T_{SS}	Soft-start time		0.7	1.5	2.8	ms
Protection						
$ILIM_{LS}$	Low-side valley current limit		6	7.5	9.5	A
$I_{_LSZC}$	Low-side zero cross current threshold	PFM mode		150		mA
$ILIM_{_LSROC}$	LS reverse current limit	FCCM mode	-1.5	-4	-6	A
T_{HICCUP}	Hiccup waiting time			23		ms
V_{UVP_F}	UVP threshold % of V_{FB}	V_{FB} falling		60		%
T_{SD}	Thermal shutdown threshold			165		°C
	Hysteresis			20		°C

Notes:
1) Guaranteed by sample characterization. Not tested in production.

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TYPICAL CHARACTERISTICS

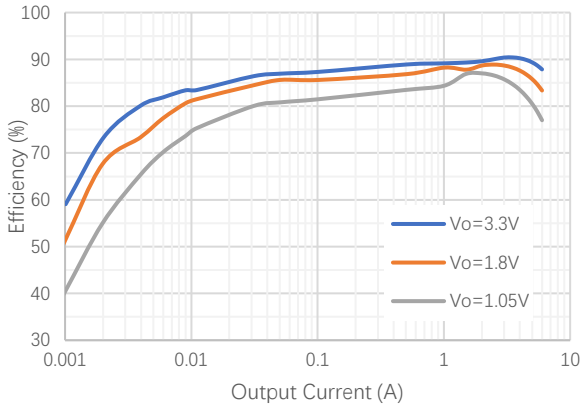


Figure 1. Efficiency vs Load Current, Vin=12V, L=1uH, PFM mode

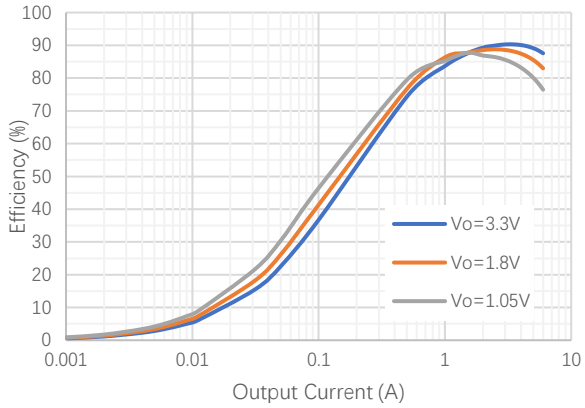


Figure 2. Efficiency vs Load Current, Vin=12V, L=1uH, FCCM mode

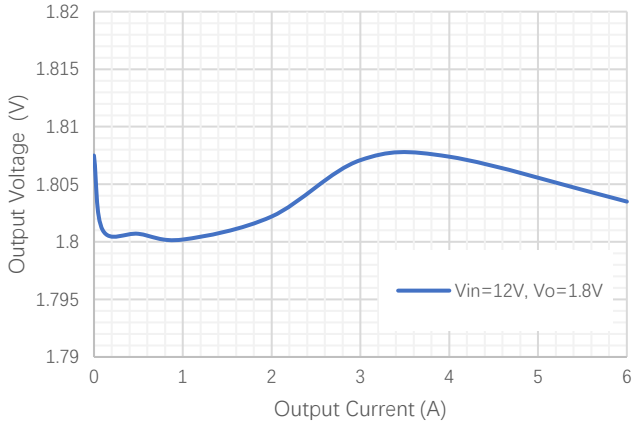


Figure 3. Load Regulation, PFM mode

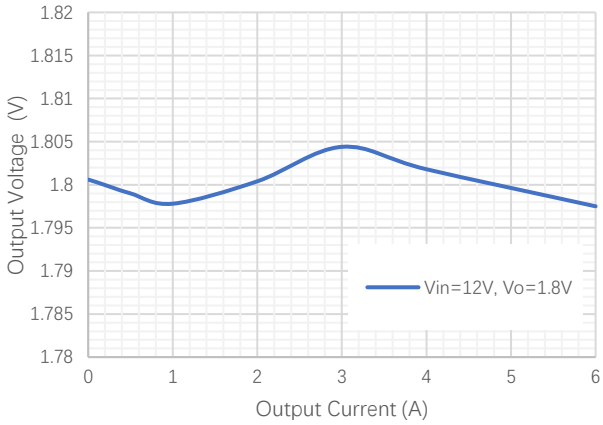


Figure 4. Load Regulation, FCCM mode

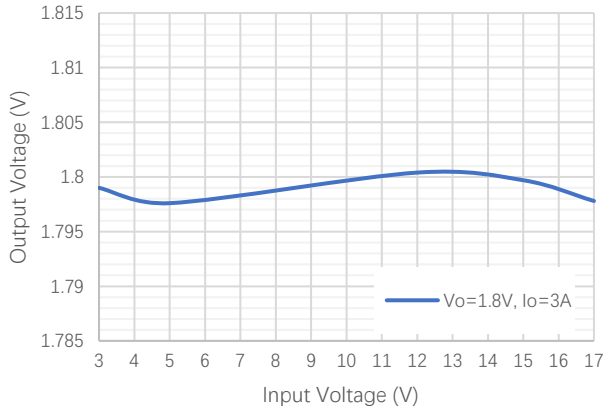


Figure 5. Line Regulation, PFM mode

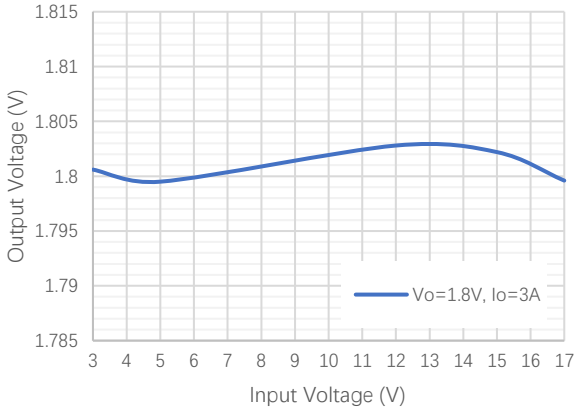


Figure 6. Line Regulation, FCCM mode

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TYPICAL CHARACTERISTICS (*Continued*)

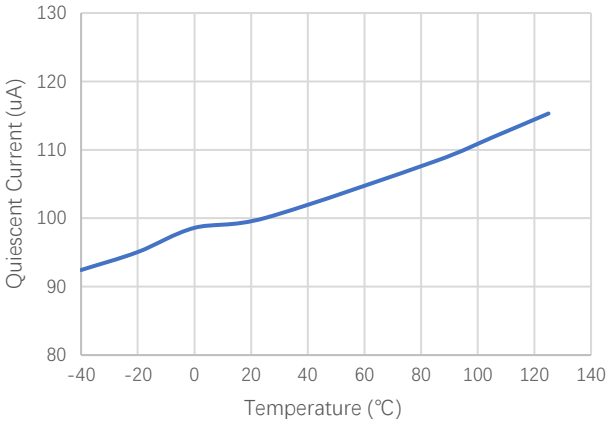


Figure 7. Quiescent Current vs Temperature, PFM mode

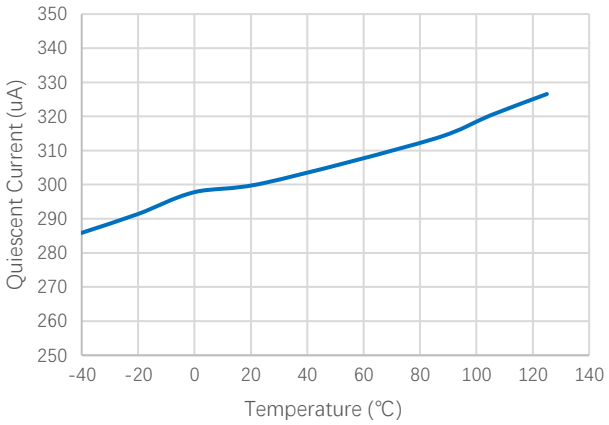


Figure 8. Quiescent Current vs Temperature, FCCM mode

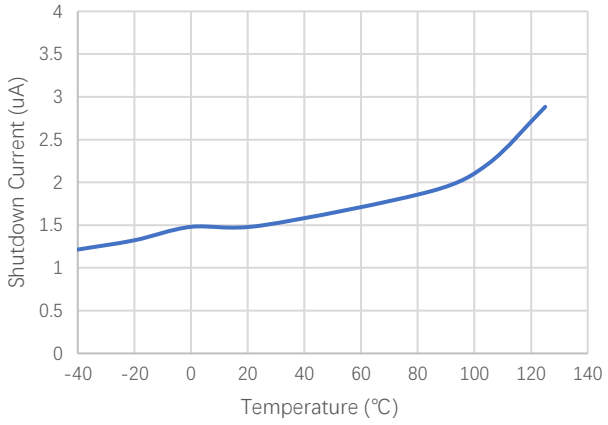


Figure 9. Shutdown Current vs Temperature

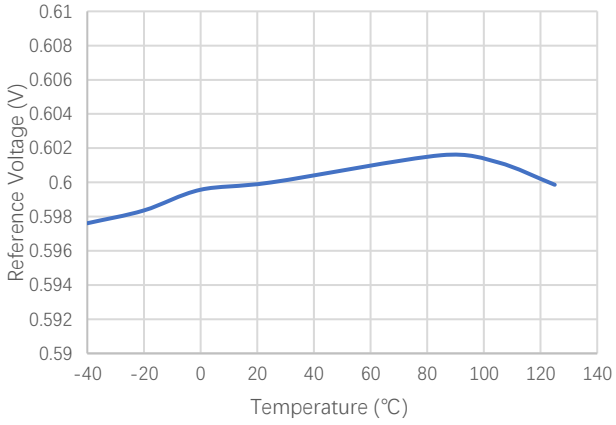


Figure 10. V_{FB} vs Temperature

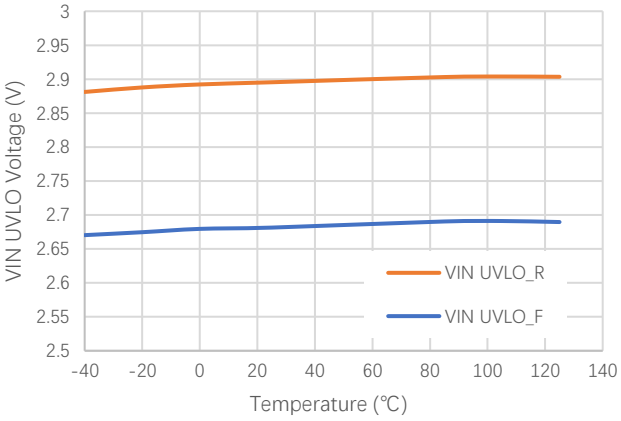


Figure 11.VIN UVLO vs Temperature

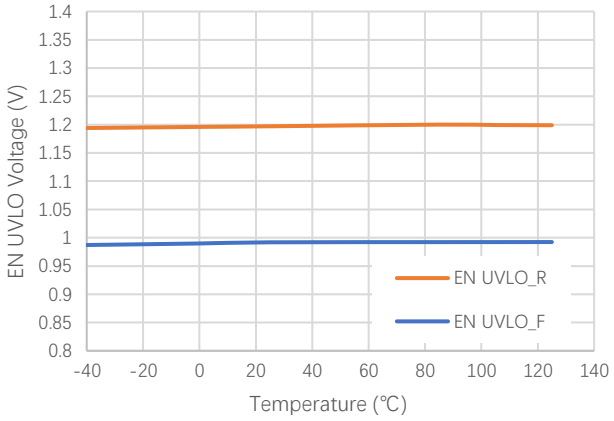


Figure 12. EN UVLO vs Temperature

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FUNCTIONAL BLOCK DIAGRAM

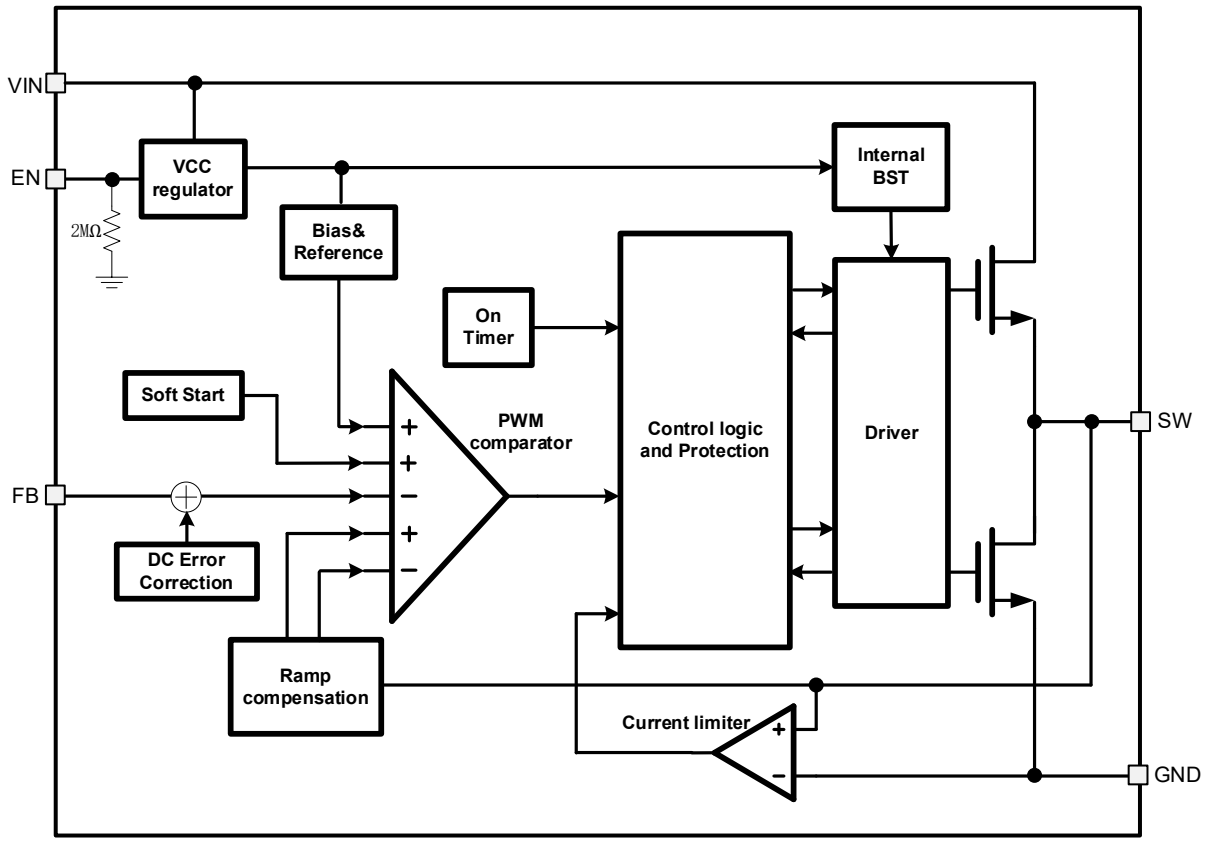


Figure 13. Functional Block Diagram

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OPERATION

Overview

The SCT226x device is a 3V-17V input, 6A output, synchronous step-down converter with built-in 42mΩ Rdson high-side and 23mΩ Rdson low-side power MOSFETs. It implements Constant on-time (COT) control to provide fast transient response and easy loop stabilization.

The SCT226x switching frequency is fixed at 550kHz. It features an internal 1.5ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The device features two different operation modes at light loading: Pulse Frequency Modulation (PFM) mode and Forced Continuous Conduction Mode (FCCM). The quiescent current is typically 100uA under no load and PFM mode condition to achieve high efficiency at light load.

The SCT226x has a default input start-up voltage of 2.9V with 200mV hysteresis. The EN function features a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to accurately meet higher UVLO system requirements.

The SCT226x full protection features include the input under-voltage lockout, over current protection with cycle-by-cycle current limiting and hiccup mode, output hard short protection and thermal shutdown protection.

Constant on-time (COT) Mode Control

The SCT226x employs constant on-time (COT) Mode control providing fast transient with pseudo fixed switching frequency. At the beginning of each cycle, the high-side MOSFET is turned on for a fixed one shot time period. The one shot time is calculated by the converter's input voltage (VIN) and the output voltage (VOUT) on a cycle-by-cycle basis to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. SCT226x turns off high-side MOSFET after the fixed on time and turns on the low-side MOSFET. SCT226x turns off the low-side MOSFET once the output voltage dropped below the output regulation, the one-shot timer then reset and the high-side MOSFET is turned on again. The on-time is inversely proportional to the input voltage and proportional to the output voltage. It can be calculated using the following Equation (1):

$$T_{ON} = \frac{V_{OUT}}{V_{IN} * f_s} \quad (1)$$

Where:

- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.
- fs is the switching frequency.

After an ON-time period, the regulator goes into the OFF-time period. The OFF-time period length depends on V_{FB} in most cases. It will end when the FB voltage decreases below 0.6V, at which point the ON-time period is triggered. If the OFF-time period is less than the minimum OFF time, the minimum OFF time will be applied, which is around 150ns typical.

Pulse Frequency Modulation (PFM) Mode

The SCT2263 works in Pulse Frequency Modulation (PFM) mode to improve the power efficiency in light load. The regulator automatically reduces the switching frequency and extends Toff while no Ton changing during the light load condition to get high efficiency and low output ripple. As the output current decreases from heavy load condition, the inductor current decreases as well, eventually nearing zero current, this is the boundary between CCM and DCM. The low side MOSFET is turned off when the inductor current reaches zero level. The load is provided only by output capacitors, when FB voltage is lower than 0.6V, the next ON cycle begins. The on-time is the minimum on time that benefits for decreasing VOUT ripple at light load condition. When the output current increases from light to heavy load the switching frequency increases to keep output voltage. The transition point to light load operation can be calculated using the following Equation (2):

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$$I_{LOAD} = \frac{V_{IN} - V_{OUT}}{2L} * T_{ON} \quad (2)$$

Where:

- T_{ON} is on-time.

Forced Continuous Conduction Mode (FCCM)

The SCT2264 forces the device operating at Forced Continuous Conduction Mode (FCCM) with pseudo-fixed switching frequency regardless loading current. Operating in FCCM mode can achieve smaller output voltage ripple compared with PFM at light load. When the load current approaches zero, the low-side MOSFET current crosses zero and sinks current from output to maintain the constant output. Hence power efficiency in light load is much lower than heavy load.

Enable and Start Up

EN is a digital control pin that can turn the regulator on and off. When applying a voltage higher than the EN high threshold (typical 1.2V/rise), the SCT226x enables all functions and the device starts the soft-start phase. The SCT226x has built-in 1.5ms soft-start time to prevent the output overshoot and inrush current. When EN pin is pulled low, the internal SS net will be discharged to ground. Buck operation is disabled when EN voltage falls below its lower threshold (typical 1V/fall). There is an internal 2MΩ resistor connected from the EN pin to ground.

Output Voltage

The SCT226x regulates the internal reference voltage at 0.6V. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$R_{FB_TOP} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_{FB_BOT} \quad (3)$$

Where:

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Under Voltage Lockout UVLO

The SCT226x Under Voltage Lock Out (UVLO) default startup threshold is typical 2.9V with VIN rising and shutdown threshold is 2.7V with VIN falling.

Over Current Protection (OCP) and Hiccup Mode

In each switching cycle, the inductor current is sensed by monitoring the low-side MOSFET during the OFF period. When the voltage between SW pin and GND pin is higher than the over current threshold voltage, the OCP will be triggered and the controller keeps the OFF state. A new switching cycle will begin only when the measured voltage is lower than limit voltage. If output loading continues to increase, output will drop below the UVP, Then the device waiting time and restart normally after 23ms. If overload or hard short condition still exists during soft-start and makes FB voltage lower than V_{UVP}, the device enters into turning-off mode again. When overload or hard short condition is removed, the device automatically recovers and enters normal regulating operation.

Thermal Shutdown

Once the junction temperature in the SCT226x exceeds 165°C, the thermal sensing circuit stops converter switching

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and restarts with the junction temperature falling below 145°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation conditions.

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APPLICATION INFORMATION

Typical Application

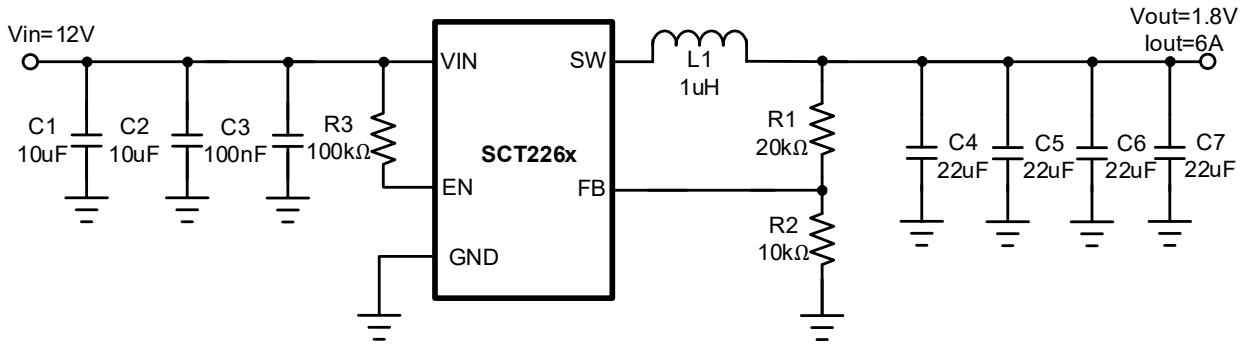


Figure 14. SCT226x Design Example, 1.8V Output

Design Parameters

Design Parameters	Example Value
Input Voltage	12V Normal 3V to 17V
Output Voltage	1.8V
Maximum Output Current	6A
Switching Frequency	550kHz
Output voltage ripple (peak to peak)	15mV
Transient Response 0A to 6A load step	ΔVout=130mV

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Application Waveforms

V_{IN}=12V, V_{OUT}=1.8V, unless otherwise noted

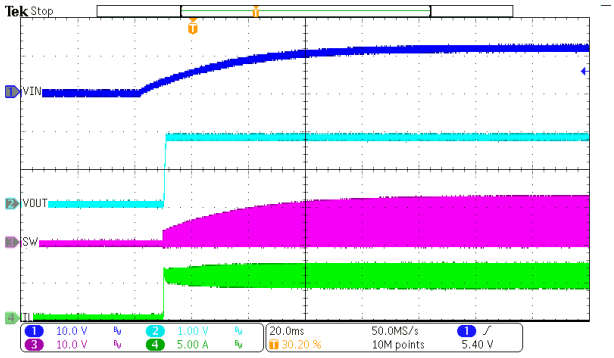


Figure 15. Power up (I_{LOAD}=6A)

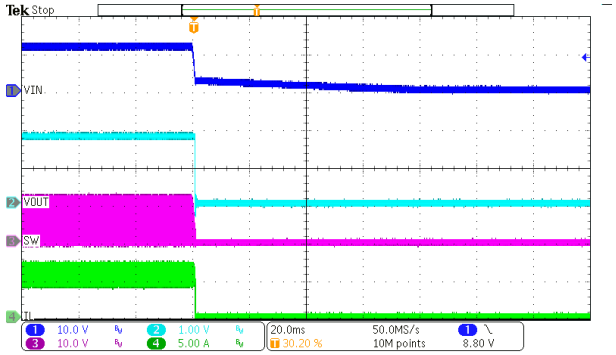


Figure 16. Power down (I_{LOAD}=6A)

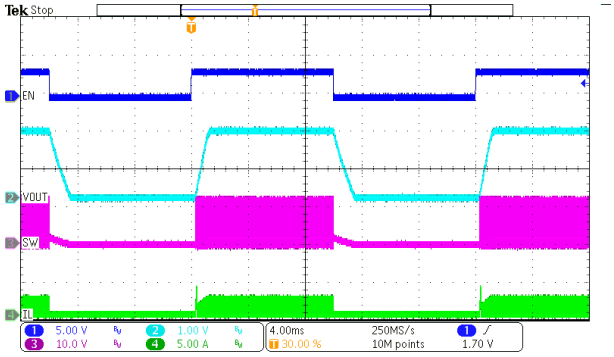


Figure 17. EN toggle (I_{LOAD}=0.1A)

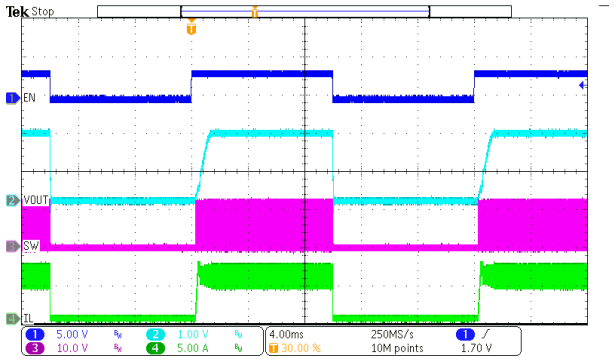


Figure 18. EN toggle (I_{LOAD}=6A)

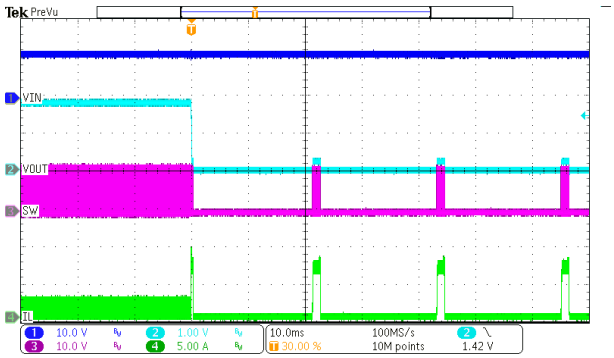


Figure 19. Over Current Protection (1A to hard short)

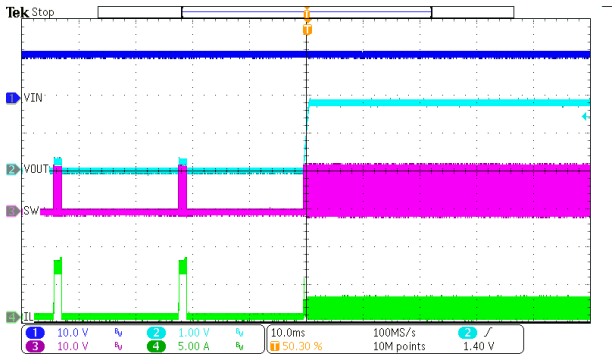


Figure 20. Over Current Release (hard short to 1A)

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Application Waveforms *(Continued)*
V_{IN}=12V, V_{OUT}=1.8V, unless otherwise noted

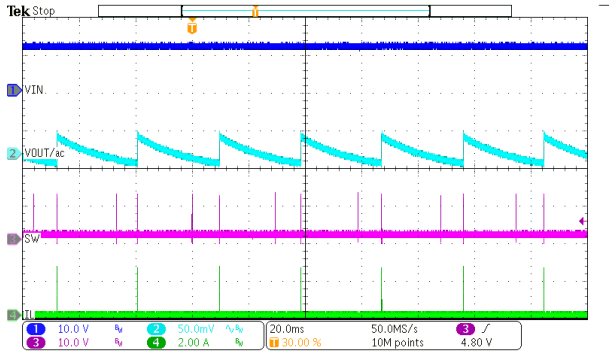


Figure 21. Output Ripple (I_{LOAD}=0A), PFM mode

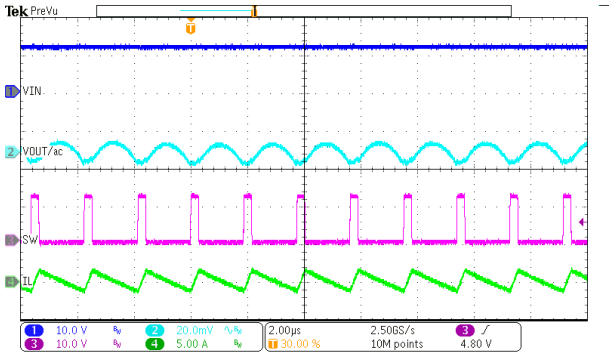


Figure 22. Output Ripple (I_{LOAD}=0A), FCCM mode

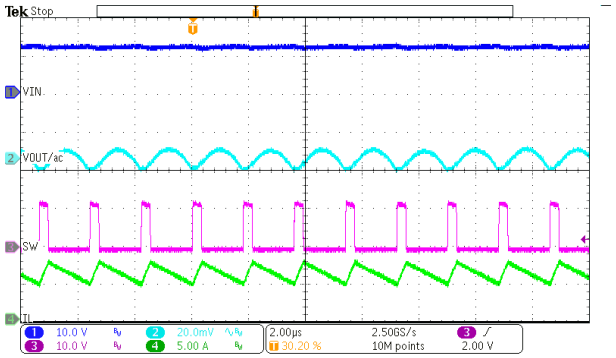


Figure 23. Output Ripple (I_{LOAD}=6A)

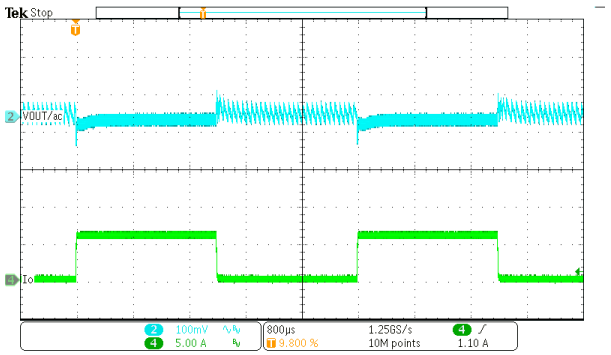


Figure 24. Load Transient (0A-6A, 1.6A/us)

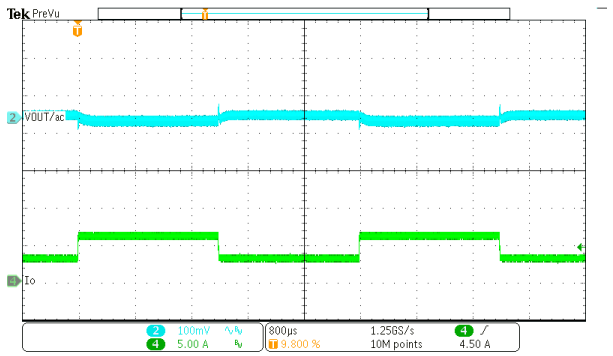


Figure 25. Load Transient (3A-6A, 1.6A/us)

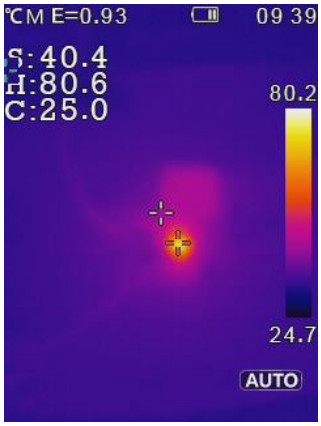


Figure 26. Thermal, V_{IN}=12V, V_{OUT}=1.8V, I_{LOAD}=6A

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Output Voltage

The output voltage is set by an external resistor divider R1 and R2 in typical application schematic. Recommended R2 resistance is 10kΩ to reduce VOUT leakage current. Use Equation 4 to calculate R1.

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_2 \quad (4)$$

where:

- V_{REF} is the feedback reference voltage, typical 0.6V.

Table 1. R_1, R_2 Value for Common Output Voltage (Room Temperature)

V_{OUT}	R_1	R_2
1.05V	7.5kΩ	10kΩ
1.8V	20kΩ	10kΩ
3.3V	45kΩ	10kΩ
5V	73.5kΩ	10kΩ

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance (DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 10%~40% of the maximum output current.

The peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 5.

$$I_{LPP} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{V_{IN} * L * f_{SW}} \quad (5)$$

where:

- I_{LPP} is the inductor peak-to-peak current.
- L is the inductance of inductor.
- f_{SW} is the switching frequency.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

Since the inductor-current ripple increases with the input voltage, the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 6 to calculate the inductance value.

$$L_{MIN} = \frac{V_{OUT}}{f_{SW} * LIR * I_{OUT(max)}} * (1 - \frac{V_{OUT}}{V_{IN(max)}}) \quad (6)$$

Where:

- L_{MIN} is the minimum inductance required.
- f_{sw} is the switching frequency.
- V_{OUT} is the output voltage.
- $V_{IN(max)}$ is the maximum input voltage.
- $I_{OUT(max)}$ is the maximum DC load current.
- LIR is coefficient of I_{LPP} to I_{OUT}.

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in Equation 7 and Equation 8.

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$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2} \quad (7)$$

$$I_{LRMS} = \sqrt{(I_{OUT})^2 + \frac{1}{12} * (I_{LPP})^2} \quad (8)$$

Where:

- I_{LPEAK} is the inductor peak current.
- I_{OUT} is the DC load current.
- I_{LPP} is the inductor peak-to-peak current.
- I_{LRMS} is the inductor RMS current.

In overloading or load transient conditions, the inductor peak current can increase. The most conservative approach is to choose an inductor with a saturation current rating greater than I_{LPEAK}. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the SCT226x can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a lower maximum output current.

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g. 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 9.

$$I_{CINRMS} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})} \quad (9)$$

The worst case condition occurs at V_{IN}=2*V_{OUT}, where:

$$I_{CINRMS} = 0.5 * I_{OUT} \quad (10)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 11 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} * C_{IN}} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

For this example, two 10μF, X7R ceramic capacitors rated for 25V in parallel are used. And a 0.1μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

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The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 12.

$$\Delta V_{OUT} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{8 * {f_{SW}}^2 * L * C_{OUT} * V_{IN}} \quad (12)$$

Where:

- ΔV_{OUT} is the output voltage ripple.
- f_{SW} is the switching frequency.
- L is the inductance of inductor.
- C_{OUT} is the output capacitance.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, four 22μF ceramic output capacitors work for most applications. Do not add a feedback capacitor across R1, because it will cause load regulation to become poor.

Table 2. Component with Typical Output Voltage BOM list

Vout (V)	L (uH)	R1 (kΩ)	R2 (kΩ)	Cout (uF)
1.05	0.68	7.5	10	4*22
1.8	1	20	10	4*22
3.3	1.5	45	10	4*22
5	2.2	73.5	10	4*22

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Layout Guideline

Proper PCB layout is critical to SCT226x's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The rule of thumb is to make ground trace lowest impedance and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing overheat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impedance of grounding.
4. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias directly under the IC. The center thermal pad should always be soldered to the board for mechanical strength and reliability, using multiple thermal vias underneath the thermal pad. Improper soldering thermal pad to ground plate on PCB will cause SW higher ringing and overshoot besides downgrading thermal performance. It is recommended 8mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss through the vias is of concern, plugging or tenting can be used to achieve a repeatable process.
5. Output inductor should be placed close to the SW pin. The area of the PCB conductor should be minimized to prevent excessive capacitive coupling.

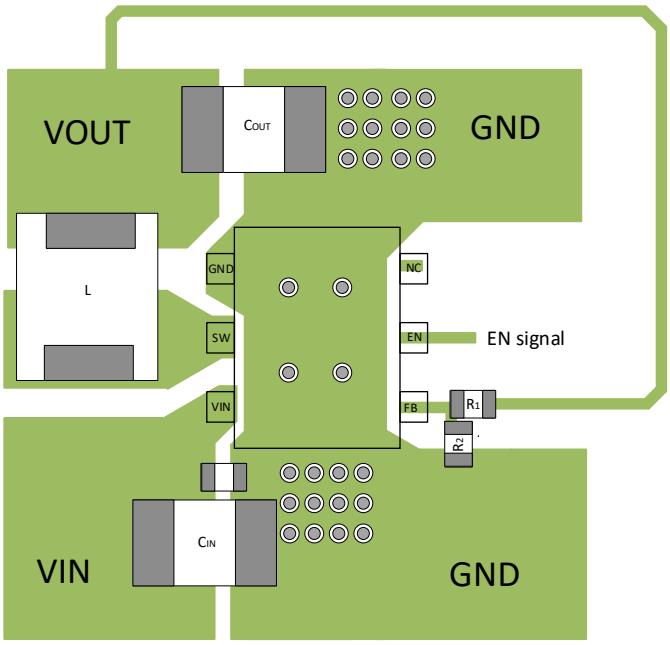
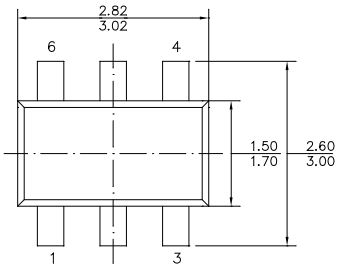


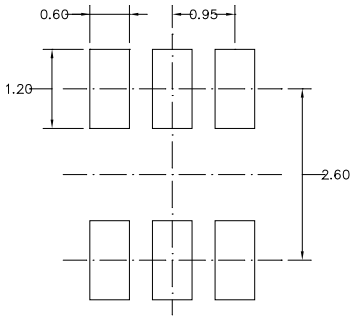
Figure 27. PCB Layout Example

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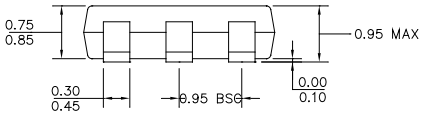
PACKAGE INFORMATION



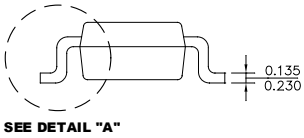
TOP VIEW



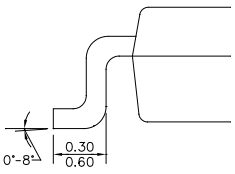
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



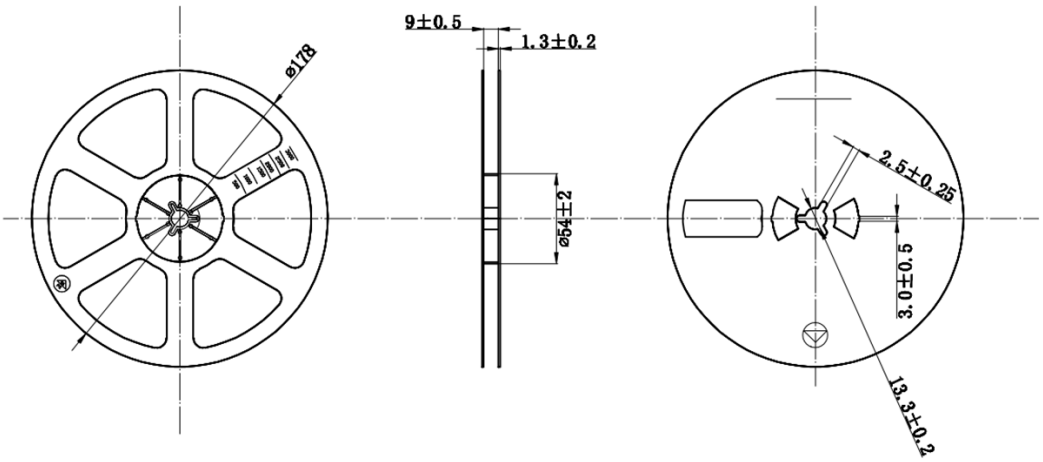
DETAIL "A"

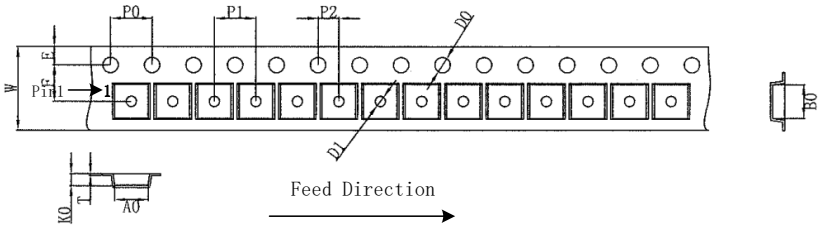
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

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TAPE AND REEL INFORMATION





ITEM	W	Ao	Bo	Ko	E	F	D1	D_n	P_n	P_1	P_2	T
MIN	7.90	3.12	3.10	1.05	1.65	3.45	-	-	3.90	3.90	1.95	0.15
NOM	8.00	3.22	3.20	1.15	1.75	3.50	1.00	1.50	4.00	4.00	2.00	0.20
MAX	8.10	3.32	3.30	1.25	1.85	3.55	1.10	1.60	4.10	4.10	2.05	0.25

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