ASIL-D Safety Power Management IC for Safety Applications

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
- Wide Input Voltage Range:
  - 3.0V-40V with pre-boost regulator
  - 6.0V-40V without pre-boost regulator
- Asynchronous Pre-Boost Controller VO_BST:
  - Fixed Output Voltage of 7.5V
  - Maximum Duty Cycle up to 95%
  - Fixed 500kHz Switching Frequency
- Synchronous Pre-Buck1 Converter VO_BUCK1:
  - Fixed Output Voltage of 5.8V/5.5V/5V/4V/3.3V
  - Up to 4A Continuous Output Current
  - Integrated 120mΩ High-Side and 90mΩ Low-Side Power MOSFETs
  - Selectable 400kHz or 2.2MHz Switching Frequency
- Synchronous Post-Buck2 Converter VO_BUCK2:
  - Output Voltage Range from 0.6V to 1.87V
  - +/- 1.5% Output Voltage Accuracy
  - Up to 4A Continuous Output Current
  - Integrated 75mΩ High-Side and 40mΩ Low-Side Power MOSFETs
  - Fixed 2.2MHz Switching Frequency
- LDO1 VO_UC for µC Supply:
  - Selectable 5V/3.3V/1.8V Output Voltage
  - +/- 2% Output Voltage Accuracy
  - Up to 800mA Continuous Output Current
- LDO2 VO_COM for Communication Supply:
  - Selectable 5V/3.3V/1.8V Output Voltage
  - +/- 2% Output Voltage Accuracy
  - Up to 600mA Continuous Output Current
- Dual Tracker LDO3,4 VO_TRK1, VO_TRK2:
  - +/- 1% Accuracy under 5V Output Voltage or +/- 10mV Accuracy under tracking mode
  - Selectable 5V/3.3V/1.8V or VREF tracking mode Output Voltage
  - Up to 200mA Continuous Output Current
- LDO5 VO_VREF for Voltage Reference:
  - Selectable 5V/3.3V/1.8V Output Voltage
  - +/- 1% Output Voltage Accuracy
  - Up to 200mA Continuous Output Current
- LDO6 VO_STB for Standby Supply:
  - Selectable 3.3V or 5V Output Voltage
  - +/- 4% Output Voltage Accuracy
  - Up to 20mA Continuous Output Current
- Integrated Frequency Dither for EMI Mitigation
- Safe State Outputs SS1, SS2
- Reset Output RESETB for System Management
- Interrupt Output INTB
- Independent External Voltage Monitor
- Error Signal Input Monitoring
- Configurable Functional and Window Watchdog
- Support Extended External Regulator for Core Supply
- Integrated Protection Features:
  - Hiccup Over Current Protection
  - Output Over-Voltage/Under-Voltage Protection
  - Input Voltage Over-Voltage Protection
  - Thermal Shutdown Protection
- Functional Safety Features:
  - Compliance with ISO26262 Development
  - Hardware Integrity up to Support ASIL-D System
  - ASIL-D Device Certification
  - BIST
- Up to 10MHz SPI Interface with Parity Bit Checking
- Available in QFN-48 (7mm*7mm)

DESCRIPTION

The SCT61490S device is a power management IC with multi-channel output. The device is designed to support safety microcontroller in automotive applications.

The SCT61490S integrates a pre-boost controller to support wide input voltage from 3V to 40V. The device has multiple switch mode regulators and low dropout (LDO) voltage regulators to supply microcontroller, sensors, peripheral ICs and communication interfaces. Each channel output is continuously monitored, any over-voltage/under-voltage fault will be detected and the device will react depending on severity. All output voltages are pre-programmed, which saves external feedback divider and minimizes system solution. The device also integrates window watchdog mode and functional watchdog mode. The dedicated WDI pin allows trigger pulse generated by MCU. Programmable

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watchdog window is suitable for a wide variety of applications.

The SCT61490S device has protection features such as thermal shutdown, short-circuit protection and input over-voltage protection. Sleep mode is available to reduce current consumption.

With advanced safety mechanism and abundant safety outputs, the device supports a wide range of applications up to ASIL-D level.

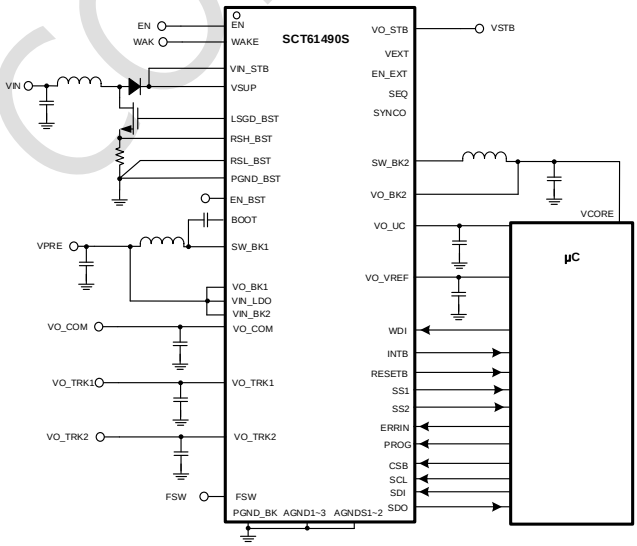
The device is available in a QFN-48(7mm*7mm) Package.

APPLICATIONS

- OBC
- Battery Management System
- Safety MCU
- ADAS
- Zone Control

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TYPICAL APPLICATION



SCT61490S Radar PMIC Typical Application Circuit

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version

Revision 0.9: Customer Sample

DEVICE ORDER INFORMATION

PART NUMBER	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL
SCT61490S-xxxxQFFR(1)	Tape & Reel	3000	1490S	48	QFN7x7-48L	3

1) For Tape & Reel, Add Suffix R (e.g. SCT61490S-xxxxQFFR)
"xxxx" is the specific suffix code for different configuration, contact SCT for details

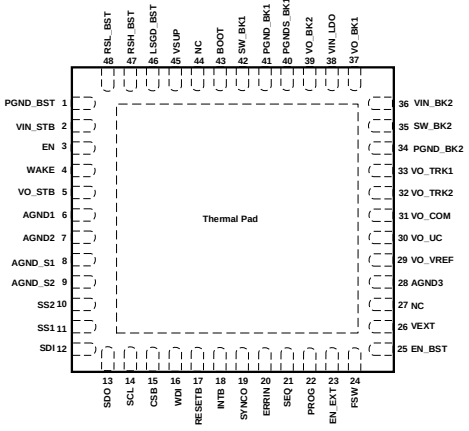
ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VSUP, EN, WAKE, VIN_STB, SS1, SS2, VO_TRK1, VO_TRK2, LSGD_BST, RSH_BST	-0.3	42	V
SW_BK1	-0.3 (-1V trans 30ns)	42	V
VO_BK1, VIN_LDO	-0.3	7	V
Others	-0.3	6	V
Junction temperature(2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 175°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN CONFIGURATION



Top View: 48-Lead QFN 7mmx7mm

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PIN FUNCTIONS

NAME	NO.	DESCRIPTION
PGND_BST	1	Boost driver ground. Connect this pin to ground at the low side of Boost external current sense resistor to decouple the driver noise from the sensitive ground. If Boost is not used, connect this pin to ground directly.
VIN_STB	2	Standby LDO voltage input. Connect this input to supply (battery) voltage with reverse protection diode and capacitor between pin and ground. An EMC filter is recommended.
EN	3	Enable Input. A positive edge signal at this pin will wake the device. Connect to ground if not used.
WAKE	4	Wake Input. A high level signal of defined length at this pin will wake the device. In case of not used, connect to ground.
VO_STB	5	Output standby LDO. Connect a capacitor as close as possible to pin.
AGND1	6	Analogue ground, pin 1. Connect this pin directly (low ohmic and low inductive) to ground.
AGND2	7	Analogue ground, pin 2. Connect this pin directly (low ohmic and low inductive) to ground.
AGND_S1	8	Analogue ground, safety, pin 1. Connect this pin directly (low ohmic and low inductive) to ground. In case a safety switch is used, connect directly to the source of the NMOS used.
AGND_S2	9	Analogue ground, safety, pin 2. Connect this pin directly (low ohmic and low inductive) to ground. In case a safety switch is used, connect directly to the source of the NMOS used.
SS2	10	Safe state output signal 2, sets the application into a safe state. Signal is delayed against SS1, delay can be adjusted via SPI command.
SS1	11	Safe state output signal 1, sets the application into a safe state.
SDI	12	Serial peripheral interface, signal data input. SPI signalling port, connect to SPI port “data output” of microprocessor to receive commands during SPI communication.
SDO	13	Serial peripheral interface, signal data output. SPI signalling port, connect to SPI port “data input” of microprocessor to send status information during SPI communication. If not used, leave open.
SCL	14	Serial peripheral signal clock. SPI signalling port, connect to SPI port “clock” of microprocessor to clock the device for SPI communication.
CSB	15	Serial peripheral interface, signal chip select. SPI signalling port, connect to SPI port “chip select” of microprocessor to address the device for SPI communication. If not used, leave open.
WDI	16	Watchdog input, trigger signal. Input for trigger signal, connect the “trigger signal output” of the microprocessor to this pin. In case of not used, leave open (internal pull-down).
RESETB	17	Reset output. Open drain structure with internal pull-up current source. A low signal at this pin indicates a reset event.
INTB	18	Interrupt signal. Push-pull-stage. A low pulse at this pin indicates an interrupt, the microprocessor shall read out the SPI status registers. Connect to a non maskable interrupt port (NMI) of the microprocessor core supply voltage.
SYNCO	19	Synchronization output signal. Connect this output to the optional external switch mode post regulator synchronization input. The signal delivers the buck regulator switching frequency either in phase or shifted by 180° (selectable via SPI command). The switch mode post regulator shall synchronize to the rising edge. If not used, leave open.

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PIN FUNCTIONS (continued)

NAME	NO.	DESCRIPTION
ERRIN	20	Error signal input. Input for error signal from microprocessor safety managing unit (SMU, internal failure detection of the microprocessor). Connect the “error signal output” of the microprocessor to this pin.
SEQ	21	Sequencer output to enable external post regulator for core supply. Connect this pin to the enable input of the external post regulator. If not used, leave open.
PROG	22	Microcontroller programming support pin. Pull down this pin to ground for operation. Optionally, this pin can be used for microcontroller debugging and programming purposes.
EN_EXT	23	Configuration pin for external post regulator for core supply. Connect this pin to ground if the option external post regulator is not used. If the option external post regulator is used, leave open.
FSW	24	Frequency adjustment pin. Connect pin to ground for low frequency range or leave open for high frequency range.
EN_BST	25	Configuration pin for boost converter. Connect this pin to ground if the option boost pre regulator is not used. If the option boost pre regulator is used, leave open.
VEXT	26	Input for optional external post regulator output voltage (core supply). Connect an external resistor divider to adjust the over and under voltage thresholds of reset output signal RESETB. If the option external post regulator is not used, leave open.
NC	27	Internally not connected: This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
AGND3	28	Analogue ground, pin 3. Connect this pin directly (low ohmic and low inductive) to ground.
VO_VREF	29	Output voltage reference. Connect a capacitor as close as possible to pin.
VO_UC	30	Output LDO_uC supply (microprocessor supply). Connect a capacitor as close as possible to pin.
VO_COM	31	Output LDO_communication supply. Connect a capacitor as close as possible to pin.
VO_TRK2	32	Output tracker 2. Connect a capacitor as close as possible to pin.
VO_TRK1	33	Output tracker 1. Connect a capacitor as close as possible to pin.
PGND_BK2	34	Post-Buck2 power ground. Connect this pin straight (low ohmic and low inductive) to ground and post· regulator output capacitor minus.
SW_BK2	35	Switching node of Post-Buck2. Connect a power inductor to this pin.
VIN_BK2	36	Pre-Buck1 redundant feedback input plus input for LV step down post regulator: Connect the capacitor of the step down pre regulator output filter with low ohmic and low inductive connection straight to this pin. Always connect in parallel with pin VO_BK1.
VO_BK1	37	Pre-Buck1 feedback input. Connect the capacitor of the buck pre regulator output filter with low ohmic and low inductive connection straight to this pin. Always connect in parallel with pin VIN_LDO.
VIN_LDO	38	Input for linear post regulators and trackers. Connect the capacitor of the buck pre regulator output filter with low ohmic and low inductive connection straight to this pin. Always connect in parallel with pin VO_BK1.
VO_BK2	39	Post-Buck2 feedback input. Connect the capacitor of the LV step down post regulator output filter with low ohmic and low inductive connection straight to this pin.

PIN FUNCTIONS (continued)

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NAME	NO.	DESCRIPTION
PGNDS_BK1	40	Pre-Buck1 power ground. Connect this pin straight (low ohmic and low inductive) to ground and pre regulator output capacitor minus. Always connect in parallel with pin PGND1.
PGND_BK1	41	Pre-Buck1 power ground. Connect this pin straight (low ohmic and low inductive) to ground and pre regulator output capacitor minus. Always connect in parallel with pin PGND1S.
SW_BK1	42	Pre-Buck1 switching node. Connect this pin straight (low ohmic and low inductive) to the pre regulator output filter.
BOOT	43	Power supply bias for high-side power MOSFET gate driver of Pre-Buck1. Connect a 0.1μF capacitor from BOOT pin to SW_BK1 pin. Bootstrap capacitor is charged when low-side power MOSFET is on or SW_BK1 voltage is low.
NC	44	Internally not connected: This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
VSUP	45	Power supply voltage Pre-Buck1 regulator input. Connect this input to the output of the boost pre regulator. If boost pre regulator option is not used, connect to supply (battery) voltage with reverse protection diode and capacitor between pin and ground. An EMC filter is recommended.
LSGD_BST	46	Driver output for external boost regulator power stage, connect to gate. Gate of low side switch of boost pre regulator: Connect to the gate of an external N-channel mosfet, line to be straight and as short as possible. If boost pre regulator option is not used, leave open.
RSH_BST	47	Sense resistor for external boost regulator power stage, high side. Connect this pin to the high side of an external current sense resistor to determine the maximum current threshold through the external N-channel mosfet. If boost pre regulator option is not used, connect to ground.
RSL_BST	48	Sense resistor for external boost regulator power stage, low side. Connect this pin to the low side of an external current sense resistor to determine the maximum current threshold through the external N-channel mosfet. If boost pre regulator option is not used, connect to ground.
Thermal Pad		Connect to ground.

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RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{BAT}	Operating Voltage Range with active Pre-Boost	3.0	40	V
T_J	Operating Junction Temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per AEC-Q100-002	-2	2	kV
	Charged Device Model(CDM), per AEC-Q100-011	-1	1	kV

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	QFN-48	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	25.06	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.49	
Ψ_{JB}	Junction-to-board characterization parameter(1)	9.1	
$R_{\theta JC\ (top)}$	Junction to case (top) thermal resistance(1)	19.5	
$R_{\theta JB}$	Junction to board thermal resistance(1)	9.53	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT61490S is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT61490S. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

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ELECTRICAL CHARACTERISTICS

V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{SUP}	Operating input voltage at VSUP pin		6		40	V
V_{SUP_UVLO}	Input UVLO	V_{SUP} rising	4.35	4.6	4.85	V
$V_{SUP_UVLO_HYS}$	Hysteresis			1.6		V
V_{SUP_OVP}	Input OVP	V_{SUP} rising	42	44	46	V
$V_{SUP_OVP_HYS}$	Hysteresis		1	2	3	V
$V_{START,STG,BUCK_RISING}$	Step down regulator short to ground activation rising threshold at pin VSUP	V_{SUP} increasing	5.5	5.7	5.9	V
$V_{START,STG,BUCK_HYS}$	Step down regulator short to ground activation threshold Hysteresis at pin VSUP			150		mV
I_Q(1)	Quiescent current from VSUP	In INIT/NORMAL/WAKE state, Boost is off, f_{OSC_BUCK1}=2.2MHz, FCCM(2)		16		mA
		In INIT/NORMAL/WAKE state, Boost is off, f_{OSC_BUCK1}=400kHz, FCCM(2)		8		mA
		In INIT/NORMAL/WAKE state, Boost is off, PFM(2)		3		mA
		In STANDBY state, Standby LDO is off, TJ=25°C		55	65	µA
		In STANDBY state, Standby LDO is off, TJ=-40~150°C			150	µA
		In STANDBY state, Standby LDO is on		70	100	µA
		In SLEEP state		150	350	µA
		In FAILSAFE state			1200	µA
Enable Signal Input EN						
V_{EN_H}	Enable high threshold	V_{EN} ramping up		1.6	2	V
V_{EN_L}	Enable low threshold	V_{EN} ramping down	0.8	1.2		V
V_{EN_HYS}	Enable hysteresis			400		mV
$T_{EN_DEGLITCH}$	Enable high deglitch time		20			µs
I_{EN_HIGH}	Enable high input current	V_{EN} = 16V		8	15	µA
I_{EN_LOW}	Enable low input current	V_{EN} = 0.5V		0.1	2	µA
Wake Signal Input WAKE						
V_{WAKE_H}	Wake high threshold	V_{WAKE} ramping up		1.6	2	V
V_{WAKE_L}	Wake low threshold	V_{WAKE} ramping down	0.8	1.2		V
V_{WAKE_HYS}	Wake hysteresis			400		mV
$T_{WAKE_DEGLITCH}$	Wake high deglitch time		40			µs

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ELECTRICAL CHARACTERISTICS (continued)

V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
I_{WAKE_HIGH}	Wake high input current	V_{WAKE} = 5V		8	15	μA
I_{WAKE_LOW}	Wake low input current	V_{WAKE} = 0.5V		0.1	2	μA
Pre-Boost Controller						
V_{PRE_BOOST}	Boost output voltage		7	7.5	8	V
V_{RSEN_THR}	Threshold external sense resistor for OC		190	210	230	mV
I_{RSL}	Low side sense input current		-40	-30	-20	μA
I_{RSH}	High side sense input current		-1	-0.5	-0.1	μA
V_{BOOST_OFF}	BOOST shutdown threshold voltage		7.8	8.3	8.8	V
$V_{BOOST_OFF_HYS}$	BOOST shutdown threshold voltage hysteresis		80	150	250	mV
I_{GATE_SRC}(2)	Gate driver peak sourcing current		60	130	195	mA
I_{GATE_SNK}(2)	Gate driver peak sinking current		55	100	160	mA
t_{GATE_RISE}	Gate driver output rise time	10% to 90%; C_{GATE} = 470 pF	12		160	ns
t_{GATE_FALL}	Gate driver output fall time	90% to 10%; C_{GATE} = 470 pF	12		160	ns
V_{BGATE}	Gate driver output voltage	V_{SUP} >6V	4.5	4.75	5.5	V
D_{MAX_BOOST}	Maximum duty cycle		75	95		%
t_{BLANK}	Blanking time			240		ns
$f_{OSC,Boost}$	Boost Frequency		450	500	550	kHz
Pre-Buck1 Converter						
V_{O_BK1}	Pre-Buck1 output voltage	V_{SUP} ≥ 6.5V, V_{O_BK1}=5.8V	5.65	5.8	5.95	V
		V_{SUP} ≥ 6.5V, V_{O_BK1}=5.5V	5.35	5.5	5.65	V
R_{DSON_H1}	High-side MOSFET on-resistance	V_{SUP} ≥ 6V		120		mΩ
R_{DSON_L1}	Low-side MOSFET on-resistance	V_{SUP} ≥ 6V	40	75	150	mΩ
I_{LIM_HS1}	High-side power MOSFET peak over current limit		5.1	6	6.9	A
I_{LIM_LS1}	Low-side power MOSFET valley over current limit		4	4.7	5.4	A
I_{LIM_NOC1}	Reverse Current Limit		0.8	1	1.2	A
t_{RISE1}(2)	SW1 rise time		2	6	14	ns
t_{FALL1}(2)	SW1 fall time		2	9	18	ns
D_{MAX_BUCK1}	Maximum duty cycle				96	%
t_{ON_MIN1}(2)	Minimum high-side on time		60	80	100	ns
t_{SS_BK1}	Soft-start time	2.2MHz, V_{O_BK1} from 5% to 95%	300	400	600	μs

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ELECTRICAL CHARACTERISTICS (continued)

V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
		400kHz, V_{O_BK1} from 5% to 95%	0.7	2	3.5	ms
R_{DIS1}	Discharge resistance	Output disabled , 2.5V< V_{O_BK1}<7V		100		Ω
T_{OT_WRN}	Over Temperature Warning Threshold		130	140	150	°C
T_{OT_SD}	Over Temperature Shutdown Threshold		165	175	185	°C
T_{OT_HYS}	Over Temperature Sensor Hysteresis		-	10	-	°C
f_{OSC_BK1}	Pre-Buck1 switching frequency range	FSW pin connected to GND	360	400	440	kHz
		FSW pin open	2000	2200	2500	kHz
Post-Buck2 Converter						
V_{O_BK2}	Post-Buck2 output voltage range		0.6		1.87	V
$V_{O_BK2_ACC}$	Output Voltage Accuracy		-1.5		1.5	%
R_{DSON_H2}	High-side MOSFET on-resistance	V_{SUP} ≥ 6V	40	75	120	mΩ
R_{DSON_L2}	Low-side MOSFET on-resistance	V_{SUP} ≥ 6V	30	40	80	mΩ
I_{LIM_HS2}	High-side power MOSFET peak over current limit			5.5		A
I_{LIM_LS2}	Low-side power MOSFET valley over current limit			4.7		A
D_{MAX_BUCK2}	Maximum duty cycle				96	%
t_{ON_MIN1}(2)	Minimum high-side on time	I_{VO_BK2}≥0.5A			50	ns
t_{SS_BK2}	Soft-start time	2.2MHz, V_{O_BK2} from 5% to 95%	70	190	380	µs
		400kHz, V_{O_BK2} from 5% to 95%	300	512	700	µs
R_{DIS2}	Discharge resistance			50		Ω
T_{OT_WRN}	Over Temperature Warning Threshold		130	140	150	°C
T_{OT_SD}	Over Temperature Shutdown Threshold		165	175	185	°C
T_{OT_HYS}	Over Temperature Sensor Hysteresis		-	10	-	°C
f_{OSC_BK2}	Post-Buck2 switching frequency range		2000	2200	2500	kHz
LDO1 VUC						
V_{O_UC}	VUC output voltage	V_{VUC} = 5V,0mA ≤ I_{VUC} ≤ 800mA	4.9	5	5.1	V
		V_{VUC} = 3.3V,0mA ≤ I_{VUC} ≤ 800mA	3.23	3.3	3.37	V
I_{LIM_VUC}	Output current limit		850	1100	1300	mA

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ELECTRICAL CHARACTERISTICS (continued)

V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{DROP_VUC}	Dropout voltage	V_{VUC} = 5V, I_{VUC} = 600mA			400	mV
		V_{VUC} = 3.3V, I_{VUC} = 600mA			550	mV
		V_{VUC} = 5V, I_{VUC} = 800mA			700	mV
		V_{VUC} = 3.3V, I_{VUC} = 800mA			850	mV
ΔV_{VUC}	Load regulation	V_{VUC} = 5V, I_{VUC} = 100μA to 600mA			10	mV
		V_{VUC} = 3.3V, I_{VUC} = 100μA to 600mA			10	mV
		V_{VUC} = 5V, I_{VUC} = 100μA to 800mA			20	mV
		V_{VUC} = 3.3V, I_{VUC} = 100μA to 800mA			20	mV
$PSRR_{VUC}$	Power supply ripple rejection	V_{O_BK1} = 5.8V, $ESRC_{VUC}$≤100mΩ, C_{VUC}=10μF, I_{VUC} = 100mA, f = 1kHz to 1MHz	26			dB
C_{VUC}	Output capacitor		2.2		47	μF
$ESRC_{VUC}$	Output capacitor, ESR		0		200	mΩ
T_{OT_WRN}	Over Temperature Warning Threshold		130	140	150	°C
T_{OT_SD}	Over Temperature Shutdown Threshold		160	180	200	°C
T_{OT_HYS}	Over Temperature Sensor Hysteresis		-	10	-	°C
t_{SS_VUC}	Soft-start time	C_{O_UC}≤15μF; V_{O_UC} rising from 10% to 90%	130	200	270	μs
R_{DIS_VUC}	Discharge resistance	Output disabled, 1.8V<V_{O_UC}<6V		50		Ω
LDO2 VCOM						
V_{O_COM}	VCOM output voltage	0mA ≤ I_{VCOM} ≤ 600mA	4.9	5	5.1	V
			3.23	3.3	3.37	V
I_{LIM_VCOM}	Output current limit		650	850	1100	mA
V_{DROP_VCOM}	Dropout voltage	0 mA ⩽ I_{VCO} ⩽ 300 mA			220	mV
		0 mA ⩽ I_{VCO} ⩽ 600 mA			550	mV
ΔV_{VCOM}	Load regulation	I_{VUC} = 100μA to 300mA			10	mV
		I_{VUC} = 100μA to 600mA			10	mV
$PSRR_{VCOM}$	Power supply ripple rejection	V_{O_BK1} = 5.8V, $ESRC_{VCOM}$≤100mΩ, C_{VCOM}=10μF, I_{VCOM} = 100mA, f = 1kHz to 1MHz	26			dB
C_{VCOM}	Output capacitor		1		47	μF
$ESRC_{VCOM}$	Output capacitor, ESR		1		200	mΩ

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ELECTRICAL CHARACTERISTICS (continued)

V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
T_{OT_WRN}	Over Temperature Warning Threshold		130	140	150	°C
T_{OT_SD}	Over Temperature Shutdown Threshold		160	180	200	°C
T_{OT_HYS}	Over Temperature Sensor Hysteresis		-	10	-	°C
t_{SS_VCOM}	Soft-start time	C_{O_COM}≤15μF; V_{O_COM} rising from 10% to 90%	130	200	270	μs
R_{DIS_VCOM}	Discharge resistance	Output disabled, 1.8V<V_{O_COM}<6V		60		Ω
LDO5 VREF						
V_{O_VREF}	VREF output voltage	0mA ≤ I_{VREF} ≤ 200mA	4.95	5	5.05	V
I_{LIM_VREF}	Output current limit		250	300	350	mA
V_{DROP_VREF}	Dropout voltage	0 mA ⩽ I_{VREF} ⩽150mA			400	mV
		0 mA ⩽ I_{VREF} ⩽200mA			450	mV
ΔV_{VREF}	Load regulation	I_{VREF} = 100μA to 200mA		4.5	9	mV
$PSRR_{VREF}$	Power supply ripple rejection	V_{O_BK1} = 5.8V, $ESRC_{VREF}$≤100mΩ, C_{VREF}=10μF, I_{VREF} = 100mA, f = 1kHz to 1MHz	26			dB
C_{VREF}	Output capacitor		1		10	μF
$ESRC_{VREF}$	Output capacitor, ESR		0		200	mΩ
t_{SS_VREF}	Soft-start time	C_{O_VREF}≤15μF; V_{O_VREF} rising from 10% to 90%	130	200	270	μs
R_{DIS_VREF}	Discharge resistance	Output disabled, 1.8V<V_{O_VREF}<6V		60		Ω
Tracker LDO3,4 VTRK1, VTRK2						
ΔV_{O_TRKx}	Output voltage tracking accuracy to voltage reference	0mA ≤ I_{VTRKx} ≤ 150mA	-10		10	mV
		0mA ≤ I_{VTRKx} ≤ 200mA	-12		12	mV
	Output Accuracy in 5V Mode	0mA ≤ I_{VTRKx} ≤ 150mA	-1		1	%
		0mA ≤ I_{VTRKx} ≤ 200mA	-1		1	%
I_{LIM_VTRKx}	Output current limit		250	350	450	mA
V_{DROP_VTRKx}	Dropout voltage	0 mA ⩽ I_{VTRKx}⩽ 200 mA			400	mV
ΔV_{VTRKx}	Load regulation	I_{VQTx}= 100μA to 200mA		4.5	9	mV
$PSRR_{VTRKx}$	Power supply ripple rejection	V_{O_BK1} = 5.8V, $ESRC_{VTRKx}$≤100mΩ, C_{VTRKx}=10μF, I_{VTRKx} = 100mA, f = 1kHz to 1MHz	26			dB
C_{VTRKx}	Output capacitor		1		10	μF
t_{SS_VTRKx}	Soft-start time	C_{O_TRKx}≤15μF; V_{O_TRKx} rising from 10% to 90%	130	200	270	μs
R_{DIS_VTRKx}	Discharge resistance	Output disabled, 1.8V<V_{O_TRKx}<6V		10		kΩ

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ELECTRICAL CHARACTERISTICS (continued)

V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Standby LDO6 VSTB						
V_{O_STB}	VSTB output voltage	V_{VSTB} = 5V,0mA ≤ I_{VSTB} ≤ 20mA	4.9	5	5.1	V
		V_{VSTB} = 3.3V,0mA ≤ I_{VSTB} ≤ 20mA	3.2	3.3	3.4	V
I_{LIM_VSTB}	Output current limit		45	60	75	mA
V_{DROP_VSTB}	Dropout voltage	V_{VSTB} = 5V, I_{VSTB}= 100μA to 20mA			500	mV
ΔV_{VSTB_LOAD}	Load regulation	V_{VSTB} = 5V, I_{VSTB}= 100μA to 20mA			20	mV
		V_{VSTB} = 3.3V, I_{VSTB}= 100μA to 20mA			20	mV
ΔV_{VSTB_LINE}	Line regulation	V_{VSTB} = 5V		0.1	0.5	mV/V
		V_{VSTB} = 3.3V		0.1	0.5	mV/V
$PSRR_{VSTB}$	Power supply ripple rejection	$ESRC_{VSTB}$≤100mΩ, C_{VSTB} =10μF, I_{VSTB} = 100mA, f = 100kHz	40			dB
C_{VSTB}	Output capacitor		0.47		10	μF
$ESRC_{VSTB}$	Output capacitor, ESR		0		200	mΩ
t_{SS_VSTB}	Soft-start time	C_{O_VSTB}≤2.2μF; V_{O_VSTB} rising from 10% to 90%	130	200	270	μs
R_{DIS_VSTB}	Discharge resistance	Output disabled, 1.8V<V_{O_VSTB}<6V		50		Ω
External Regulator						
V_{SEQ_H}	SEQ high level	V_{VUC} = 5.0 V, I_{EN_EXT} = -9 mA	4			V
		V_{VUC} ≥ 4.7 V, I_{EN_EXT} = -0.5 mA	4.6			V
		V_{VUC} = 3.3 V, I_{EN_EXT} = -7 mA	2.3			V
		V_{VUC} ≥ 3.1 V, I_{EN_EXT} = -0.5 mA	3			V
V_{ENC_L}	SEQ low level	V_{VUC} = 5V, I_{EN_EXT} = 7 mA			0.7	V
		V_{VUC} = 3.3 V, I_{EN_EXT} = 5.5 mA			0.7	V
I_{VRXTI}	Core voltage monitoring input pull-up current	VEXT = 0.8V		100	130	nA
V_{SYN_HI}	SYNC output high level	V_{VUC} = 5V, I_{SYNC} = -9mA	4			V
		V_{VUC} ≥ 4.7V, I_{SYNC} = -0.5mA	4.6			V
		V_{VUC} = 3.3V, I_{SYNC} = -7mA	2.3			V
		V_{VUC} ≥ 3.1V, I_{SYNC} = -0.5mA	3			V
V_{SYN_LO}	SYNC output low level	V_{VUC} = 5V, I_{SYNC} = 7mA			0.7	V

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ELECTRICAL CHARACTERISTICS (continued)

V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{SYN_LO}	SYNC output low level	V_{VUC} = 3.3V, I_{SYNC} = 5.5mA			0.7	V
D_{SYNC}	SYNC output duty cycle			50		%
RESETB Timing						
t_{CYCLE}	Reset cycle time		9.4	10	10.65	μs
t_{RD}	Reset delay time,	Default option		1000		t_{CYCLE}
		Adjustable Range	20		1500	t_{CYCLE}
t_{RR}	Reset reaction time		14		26	μs
t_{RR_STB}	Reset reaction time of standby LDO		14		40	μs
t_{STG}	Short to ground detection time	LDO	2.7	3	3.3	ms
		Pre-Buck1, 2.2MHz switching frequency	2.7	3	3.3	ms
		Pre-Buck1, 400kHz switching frequency	5.4	6	6.6	ms
t_{SHUT}	System shutdown time		9		20	ms
RESETB OV/UV Threshold for Standby LDO VSTB						
$V_{OV_THR_VSTB}$	Over voltage reset threshold	5V output	105	107	109	%
		3.3V output	105	107	109	%
$V_{OV_HYS_VSTB}$	Over voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV
$V_{UV_THR_VSTB}$	Under voltage reset threshold	5V output, option 0	84	86	88	%
		5V output, option 1	88	90	92	%
		3.3V output, option 0	88	90	92	%
		3.3V output, option 1	90	92	94	%
$V_{UV_HYS_VSTB}$	Under voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV
RESETB OV/UV Threshold for LDO VUC						
$V_{OV_THR_VUC}$	Over voltage reset threshold	5V output	105	107	109	%
		3.3V output	105	107	109	%
$V_{OV_HYS_VUC}$	Over voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV
$V_{UV_THR_VUC}$	Under voltage reset threshold	5V output, option 0	84	86	88	%
		5V output, option 1	88	90	92	%
		3.3V output, option 0	88	90	92	%
		3.3V output, option 1	90	92	94	%
$V_{UV_HYS_VUC}$	Under voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV

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ELECTRICAL CHARACTERISTICS (continued)

V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
RESETB OV/UV Threshold for LDO VCOM						
$V_{OV_THR_VCOM}$	Over voltage reset threshold	5V output, option 0	108	110	112	%
		5V output, option 1	103	105	107	%
		3.3V output, option 0	105	107	109	%
		3.3V output, option 1	103	105	107	%
$V_{OV_HYS_VCOM}$	Over voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV
$V_{UV_THR_VCOM}$	Under voltage reset threshold	5V output, option 0	88	90	92	%
		5V output, option 1	93	95	97	%
		3.3V output, option 0	88	90	92	%
		3.3V output, option 1	90	92	94	%
$V_{UV_HYS_VCOM}$	Under voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV
RESETB OV/UV Threshold for LDO VREF						
$V_{OV_THR_VREF}$	Over voltage reset threshold	5V output, option 0	105	107	109	%
		5V output, option 1	102	104	106	%
		3.3V output, option 0	105	107	109	%
		3.3V output, option 1	104	106	108	%
$V_{OV_HYS_VREF}$	Over voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV
$V_{UV_THR_VREF}$	Under voltage reset threshold	5V output, option 0	84	86	88	%
		5V output, option 1	95	96	97	%
		3.3V output, option 0	88	90	92	%
		3.3V output, option 1	92	94	96	%
$V_{UV_HYS_VREF}$	Under voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV
RESETB OV/UV Threshold for Tracker VTRK1						
$V_{OV_THR_VTRK1}$	Over voltage reset threshold	5V output, option 0	108	110	112	%
		5V output, option 1	106	108	110	%
		3.3V output	105	107	109	%
$V_{OV_HYS_VTRK1}$	Over voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV

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ELECTRICAL CHARACTERISTICS (continued)

V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{UV_THR_VTRK1}$	Under voltage reset threshold	5V output, option 0	88	90	92	%
		5V output, option 1	90	92	94	%
		3.3V output, option 0	88	90	92	%
		3.3V output, option 1	90	92	94	%
$V_{UV_HYS_VTRK1}$	Under voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV
RESETB OV/UV Threshold for Tracker VTRK2						
$V_{OV_THR_VTRK2}$	Over voltage reset threshold	5V output, option 0	108	110	112	%
		5V output, option 1	106	108	110	%
		3.3V output	105	107	109	%
$V_{OV_HYS_VTRK2}$	Over voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV
$V_{UV_THR_VTRK2}$	Under voltage reset threshold	5V output, option 0	88	90	92	%
		5V output, option 1	90	92	94	%
		3.3V output, option 0	88	90	92	%
		3.3V output, option 1	90	92	94	%
$V_{UV_HYS_VTRK2}$	Under voltage reset hysteresis	5V output	30	50	70	mV
		3.3V output	20	33	50	mV
RESETB OV/UV Threshold for Pre-Buck1						
$V_{OV_THR_VBK1}$	Over voltage reset threshold		111	113	115	%
$V_{OV_HYS_VBK1}$	Over voltage reset hysteresis		40	60	90	mV
$V_{UV_THR_VBK1}$	Under voltage reset threshold		86	88	90	%
$V_{UV_HYS_VBK1}$	Under voltage reset hysteresis		40	60	90	mV
RESETB OV/UV Threshold for VEXT						
$V_{OV_THR_VEXT}$	Over voltage reset threshold	Option0	107.5	109	110.5	%
		Option1	106.5	108	109.5	%
$V_{OV_HYS_VEXT}$	Over voltage reset hysteresis		5	8	15	mV
$V_{UV_THR_VEXT}$	Under voltage reset threshold	Option0	89.5	91	92.5	%
		Option1	90.5	92	91.5	%
$V_{UV_HYS_VEXT}$	Under voltage reset hysteresis		5	8	15	mV
I_{RSTB_PULL}	RESETB output, pull-up current	$V_{RSTB} \leqslant$ 2.0 V	-175	-110	-15	μA

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ELECTRICAL CHARACTERISTICS (continued)

V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
RESETB Output						
$_{RSTB_L}$	RESETB output low level	V_{VUC} = 5V, I_{RSTB} = 7mA			0.7	V
		V_{VUC} = 5V, I_{RSTB} = 3.5mA			0.4	V
		V_{VUC} = 3.3V, I_{RSTB} = 5.5mA			0.7	V
		V_{VUC} = 3.3V, I_{RSTB} = 3mA			0.4	V
t_{RSTB_FALL}(2)	RESETB output fall time	C_{RSTB} = 50pF			25	ns
INTB Output						
V_{INTB_H}	Interrupt output high level	V_{VUC} = 5V, I_{INTB} = -9mA	4			V
		V_{VUC} = 3.3V, I_{INTB} = -7mA	2.3			V
V_{INTB_L}	Interrupt output low level	V_{VUC} = 5V, I_{INTB} = 7mA			0.7	V
		V_{VUC} = 3.3V, I_{INTB} = 5mA			0.7	V
t_{INTB_RISE}(2)	INTB output rise time	C_{INTB} = 50pF			25	ns
t_{INTB_FALL}(2)	INTB output fall time	C_{INTB} = 50pF			25	ns
State Machine						
t_{INIT}	INIT timer / Initialization time-out		550	600	650	ms
$t_{FAILSAFE}$	FAILSAFE time		18	20	22	ms
$t_{FAILSAFE_TSD}$	FAILSAFE time TSD	Thermal shutdown	0.9	1	1.1	s
t_{TR_DEL}	Transition delay timer accuracy		-20		20	%
I_{VUC_ATT}	VUC current monitoring for low power states	10mA monitor current	-60		60	%
		30mA monitor current	-40		40	%
		60mA monitor current	-35		35	%
		100mA monitor current	-30		30	%
t_{TRANS}	State transition time	Except transitions to SLEEP, to STANDBY or from STANDBY			100	µs
t_{TRANS_INIT}	State transition time to INIT	Except transitions from STANDBY, FAILSAFE and POWERDOWN			150	µs
		From STANDBY, FAILSAFE and interrupted transition to STANDBY			250	µs
t_{ST_PWD}	Internal start-up time from POWERDOWN	From first VS connection to INIT/ power sequence		0.4	2	ms
ERRIN Pin						
V_{ERR_H}	ERRIN valid high level	V_{VUC} = 5V	3.6			V
		V_{VUC} = 3.3V	2			V

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ELECTRICAL CHARACTERISTICS (continued)

V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{ERR_L}	ERRIN valid low level				0.8	V
V_{ERR_HYS}	ERRIN hysteresis	V_{VUC} = 5V		350		mV
		V_{VUC} = 3.3V		160		mV
I_{ERR_PULL}	ERRIN pull-down current			150	330	μA
C_{ERR}(2)	ERR input capacitance			4	15	pF
t_{ERR_VALID}	Valid ERRIN input signal frequency	Duty = 50%	10		45	kHz
$t_{ERR_INVALID}$	Invalid ERRIN input signal frequency	Duty = 50%, low frequency	0		5	kHz
		Duty = 50%, high frequency	96.2		500	kHz
t_{ERR_DET}	Invalid ERRIN input signal detection time	Low frequency	50.1		99.9	μs
		High frequency	5.2		11.1	μs
t_{ERR_REAC}	ERRIN reactivation time-out	After SLEEP	9	10	11	ms
		After re-enabling via SPI	50.1		110	μs
Safe State Indicator SSx						
V_{SSx_H}	SSx output high level	V_{VUC} = 5V, I_{SSx} ≥ -1mA	3.6	4.8	V_{VUC}	V
		V_{VUC} = 5V, I_{SSx} ≥ -5mA	3	4.3	V_{VUC}	V
		V_{VUC} = 3.3V, I_{SSx} ≥ -1mA	2.9	3.2	V_{VUC}	V
		V_{VUC} = 3.3V, I_{SSx} ≥ -5mA	2	2.8	V_{VUC}	V
R_{SSx}	SSx pull-down resistor		70	100	130	kΩ
V_{SSx_L}	SSx output low level				0.8	V
t_{SSx}	SSx internal reaction time			12	30	μs
t_{SSx_ACC}	SSx time base accuracy		-10		10	%
t_{REC}	Adjustable recovery delay time	Option0		0		ms
		Option1		1		ms
		Option2		2.5		ms
		Option3		5		ms
		Option4		10		ms
t_{SS_DLY}	Adjustable delay time between SS1 and SS2	Option0		0		ms
		Option1		10		ms
		Option2		50		ms
		Option3		100		ms
		Option4		250		ms
Watch Dog Interface						
t_{WD_PERIOD}	Watchdog period time	Option0	94	100	106	μs
		Option1	940	1000	1060	μs
t_{WD_OPEN}	Long open window time		564	600	639	ms

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ELECTRICAL CHARACTERISTICS (continued)

V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
t_{WD_SAMPLE}	Watchdog sampling time		188	200	213	μs
V_{WDI_HI}	Threshold for WDI pin	WDI voltage rising, V_{VUC} = 5V	3.6			V
		WDI voltage rising, V_{VUC} = 3.3V	2			V
V_{WDI_LOW}	Threshold for WDI pin				0.8	V
V_{WDI_HYS}	WDI Hysterisis	V_{VUC} = 5V		350		mV
		V_{VUC} = 3.3V		160		mV
I_{WDI_PULL}	WDI pull-down current			150	330	μA
R_{WDI}(2)	WDI input capacitance			4	15	pF
$t_{WDI_DEG_RISING}$	Deglitch time for WDI pin	WDI voltage rising		20		μs
t_{WD}	Watchdog timer accuracy		-8		8	%
Wake up Timer						
t_{WAKE_TR}	Wake up timer	Option0	9.5	10	10.5	μs
		Option1	9.5	10	10.5	ms
		Option2	0.95	1	1.05	s
C_{WAKE}	Counter			24		bit
SPI Interface (CSB, SCL, SDO, SDI)						
$V_{CSB,High}$	CSB Pin High Voltage Level	V_{VUC}=5V	3.6			V
		V_{VUC}=3.3V	2			V
$V_{CSB,Low}$	CSB Pin Low Voltage Level				0.8	V
$V_{CSB,\ Hys}$	CSB Pin Hysteresis	V_{VUC}=5V		350		mV
		V_{VUC}=3.3V		160		mV
$I_{CSB,\ PULL}$	CSB Pin Pull Up Current	V_{SCL}= V_{VUC}	-175	-120		μA
$V_{SCL,High}$	SCL Pin High Voltage Level	V_{VUC}=5V	3.6			V
		V_{VUC}=3.3V	2			V
$V_{SCL,Low}$	SCL Pin Low Voltage Level				0.8	V
$V_{SCL,\ Hys}$	SCL Pin Hysteresis	V_{VUC}=5V		350		mV
		V_{VUC}=3.3V		160		mV
$I_{SCL,\ PULL}$	SCL Pin Pull Up Current	V_{SCL}= V_{VUC}		150	330	μA
$V_{SDI,High}$	SDI Pin High Voltage Level	V_{VUC}=5V	3.6			V
		V_{VUC}=3.3V	2			V
$V_{SDI,Low}$	SDI Pin Low Voltage Level				0.8	V
$V_{SDI,\ Hys}$	SDI Pin Hysteresis	V_{VUC}=5V		350		mV
		V_{VUC}=3.3V		160		mV
$I_{SDI,\ PULL}$	SDI Pin Pull Up Current	V_{SCL}= V_{VUC}		150	330	μA

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ELECTRICAL CHARACTERISTICS (continued)

V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{SDO,High}$	SDO Pin High Voltage Level	V_{VUC}=5V, I_{SDO}=-9mA	4			V
		V_{VUC}=3.3V, I_{SDO}=-7mA	2.3			V
$V_{SDO,Low}$	SDO Pin Low Voltage Level	I_{SDO}=-7mA			0.7	V
$V_{SDO,High}$	SDO Pin Voltage Rise Time	C_{SDO}=50pF			25	ns
$t_{SDO, fall}$	SDO pin Voltage Fall Time	C_{SDO}=50pF			25	ns
$I_{SDO, Leakge}$	SDO Pin Leakage Current	Tri-state	-1		1	μA
SPI Timing						
F_{SPI_CLK}	CLK_SPI operating Frequency				10	MHz
		SLEEP state			1.5	MHz
D_{SPI}	CLK signal duty cycle		45	50	55	%
t_{SPI_CLK}	CLK_SPI operating Period		100			ns
$t_{SPI_CLK_H}$	CLK_SPI high time		45			ns
$t_{SPI_CLK_L}$	CLK_SPI low time		45			ns
$t_{SPI_CLK_R}$	CLK_SPI rise time	$t_{SPI_FACT} \le t_{SPI_CLK}$; 100 ns ≤ t_{SPI_FACT} ≤ 1 μs			0.1* t_{SPI_FACT}	ns
$t_{SPI_CLK_F}$	CLK_SPI fall time	$t_{SPI_FACT} \le t_{SPI_CLK}$; 100 ns ≤ t_{SPI_FACT} ≤ 1 μs			0.1* t_{SPI_FACT}	ns
t_{SPI_LEAD}	CLK_SPI lead time		100			ns
t_{SPI_LAG}	CLK_SPI lag time		50			ns
t_{CSB_R}	SPI Chip Select (CSB) Rise Time	$t_{SPI_FACT} \le t_{SPI_LAG}$; 50 ns ≤ t_{SPI_FACT} ≤ 500ns			0.2* t_{SPI_FACT}	ns
t_{CSB_F}	SPI Chip Select (CSB) Fall Time	$t_{SPI_FACT} \le t_{SPI_LAG}$; 100 ns ≤ t_{SPI_FACT} ≤1 μs			0.2* t_{SPI_FACT}	ns
t_{SDI_SET}	SPI Data Input (SDI) Setup		10			ns
t_{SDI_HOLD}	SPI Data Input (SDI) Hold Time		10			ns
t_{SDO_CLK}	SPI Data Output (SDO) Valid after CLK_SPI	C_{SDO} = 50 pF; $t_{SPI_FACT} \ge t_{SPI_clkf}$; 10 ns ≤ t_{SPI_FACT} ≤ 100 ns			0.1* t_{SPI_FACT}+36	ns
t_{SDI_SDO}	SPI Write Propagation Delay SDI to SDO				35	ns
t_{SDO_ACC}	SPI Data Output (SDO) Access	C_{SDO} = 50 pF			50	ns
t_{SDO_DIS}	SPI Data Output (SDO) Disable Time	C_{SDO} = 50 pF			100	ns

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ELECTRICAL CHARACTERISTICS (continued)

V_{SUP}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
t_{SEQ_DLY}	Sequential Transfer Delay		600			ns
		SLEEP state	2			µs
t_{SPI_DUR}	Frame duration (CSB low)				1.85	ms

(1) All quiescent current are measured under T_J ≤85°C and 10V≤ VIN≤ 28V, no load, selectable options off (external regulators, watchdog, timers).
(2) Guaranteed by sample characterization, not tested in production.

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TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{Buck1} = 5.8V, V_{Buck2} = 1.2V, V_{LDO1} ~ V_{LDO6}= 5V, L1 = 10μH, L2 = 1μH, T_A = 25°C, unless otherwise noted.

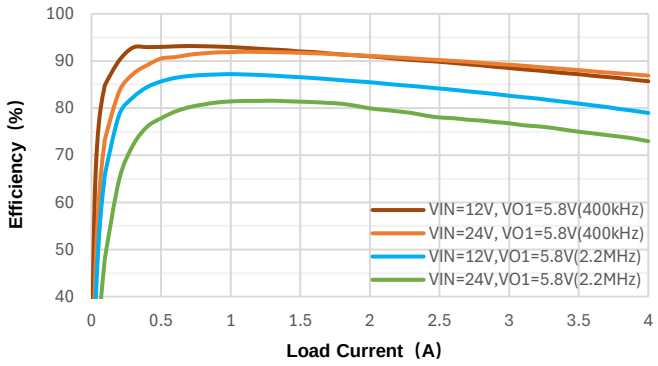


Figure 1. Buck1 Efficiency vs. Load Current

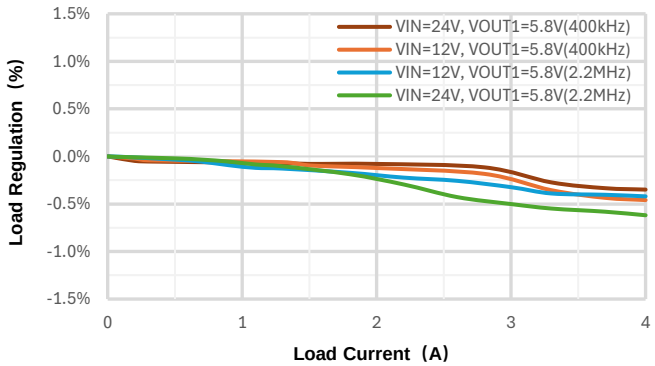


Figure 2. Buck1 Load Regulation

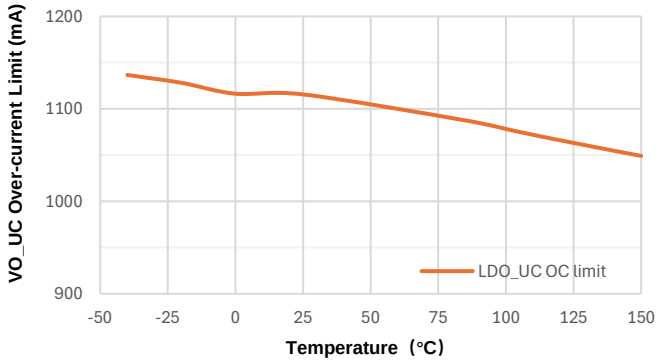


Figure 3. VO-UC Over-current Limit vs. Temperature

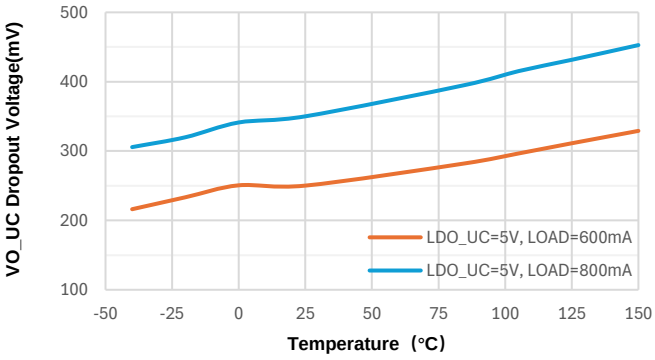


Figure 4. VO-UC Dropout Voltage vs. Temperature

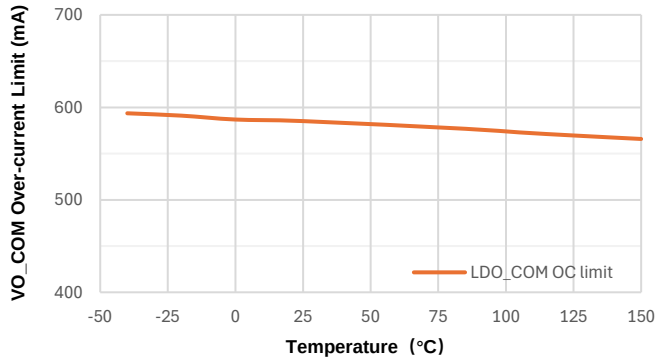


Figure 5. VO-COM Over-current Limit vs. Temperature

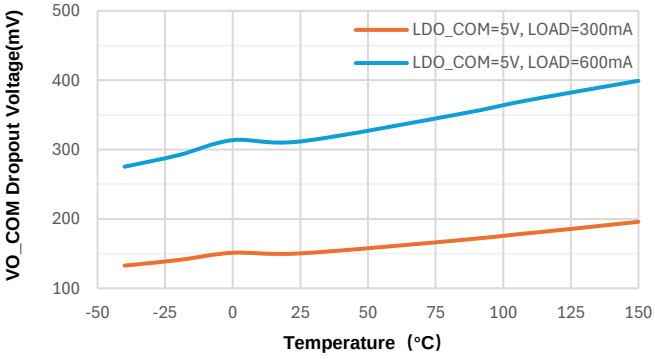


Figure 6. VO-COM Dropout Voltage vs. Temperature

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TYPICAL CHARACTERISTICS (continued)

V_{IN} = 12V, V_{Buck1} = 5.8V, V_{Buck2} = 1.2V, V_{LDO1} ~ V_{LDO6}= 5V, L1 = 10μH, L2 = 1μH, T_A = 25°C, unless otherwise noted.

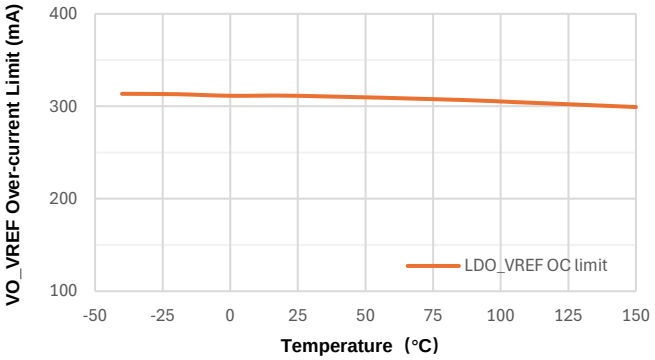


Figure 7. VO-VREF Over-current Limit vs. Temperature

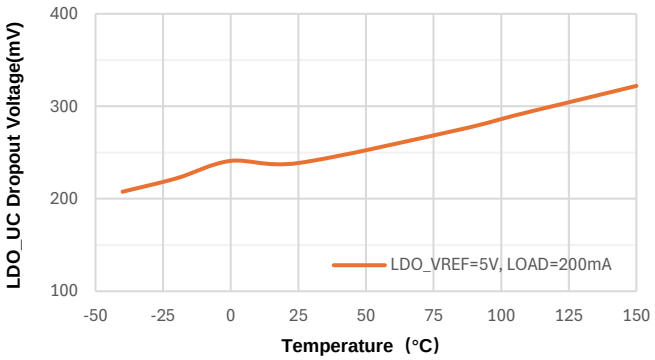


Figure 8. VO-VREF Dropout Voltage vs. Temperature

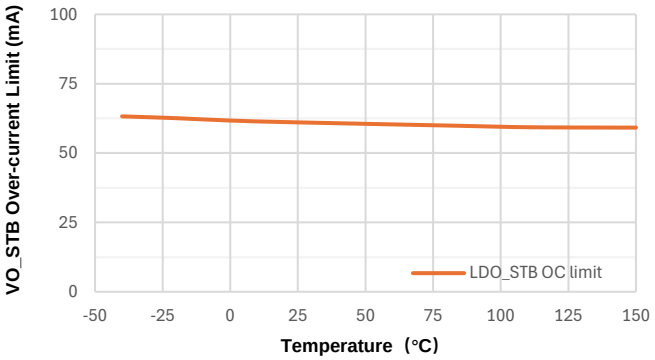


Figure 9. VO-STB Over-current Limit vs. Temperature

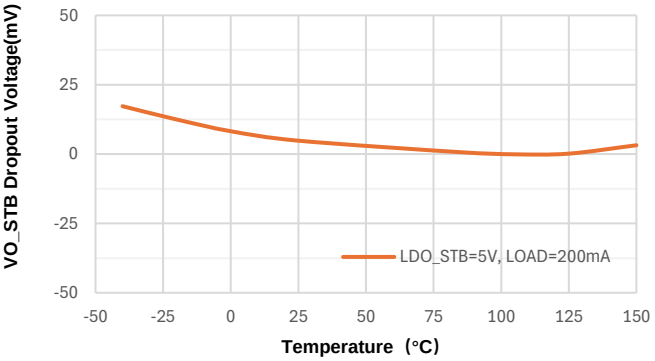


Figure 10. VO-STB Dropout Voltage vs. Temperature

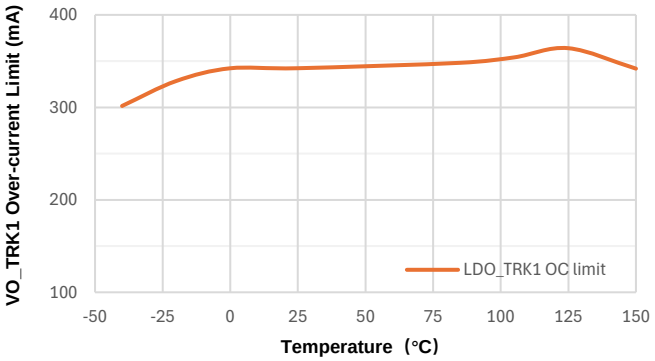


Figure 11. VO-TRK1 Over-current Limit vs. Temperature

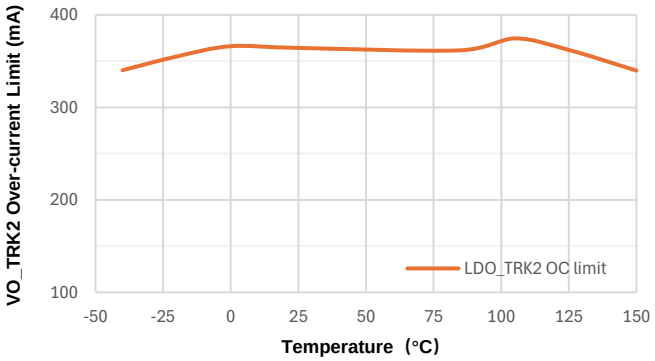


Figure 12. VO-TRK2 Dropout Voltage vs. Temperature

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FUNCTIONAL BLOCK DIAGRAM

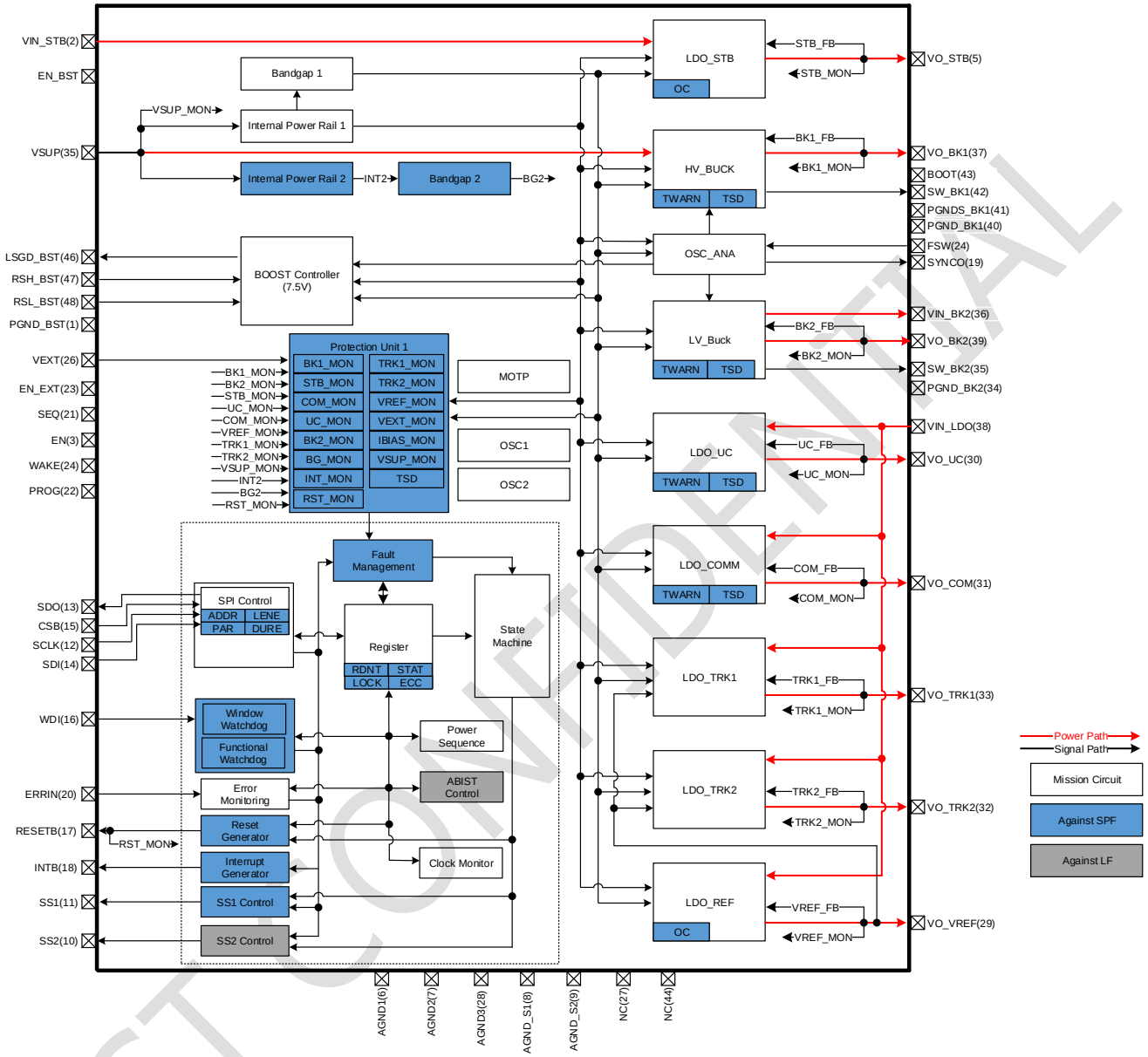


Figure 13. Functional Block Diagram

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OPERATION

1 Overview

The SCT61490S device is a power management IC with eight channels output. The device is designed to support safety microcontroller in automotive applications.

The SCT61490S integrates a pre-boost controller to support wide input voltage from 3V to 40V. The device has multiple switch mode regulators and low dropout (LDO) voltage regulators to supply microcontroller, sensors, peripheral ICs and communication interfaces. Each channel output is continuously monitored, any over-voltage/under-voltage fault will be detected and the device will enter safe state. All output voltages are pre-programmed, which saves external feedback divider and minimizes system solution

2 Wake-up Function

2.1 Introduction

The SCT61490S device is automatically turned on when connected to a battery (Power-On-Reset POR) and moves into INIT-state, where the device will be configured. After successful configuration, the device will be sent to NORMAL state via SPI command. From NORMAL or WAKE state, the device can be sent to a low power state (SLEEP or STANDBY) via SPI commands. The WAKE and EN signal are external triggers to leave the low power states (or the FAILSAFE state).

The SCT61490S provides the following wakeup sources:

• EN pin (edge sensitive input)

A positive going edge at pin EN with a rise time T_{EN_RISE} represents a valid Wake-up Signal

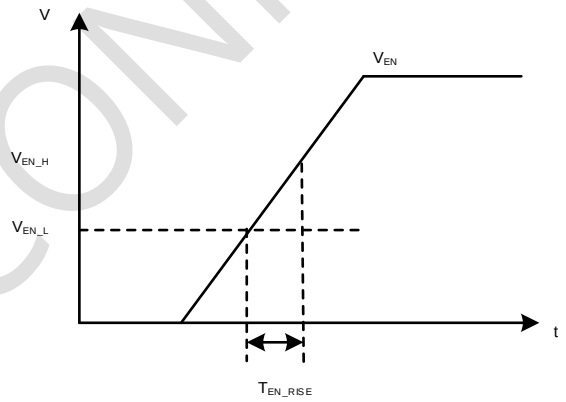


Figure 14. Valid enable signal

• WAKE pin (level sensitive input)

A signal, with a voltage higher than V_{WAKE_H} applied at pin WAKE for $T_{WAKE_DEGLITCH}$ represents a valid Wake-up signal.

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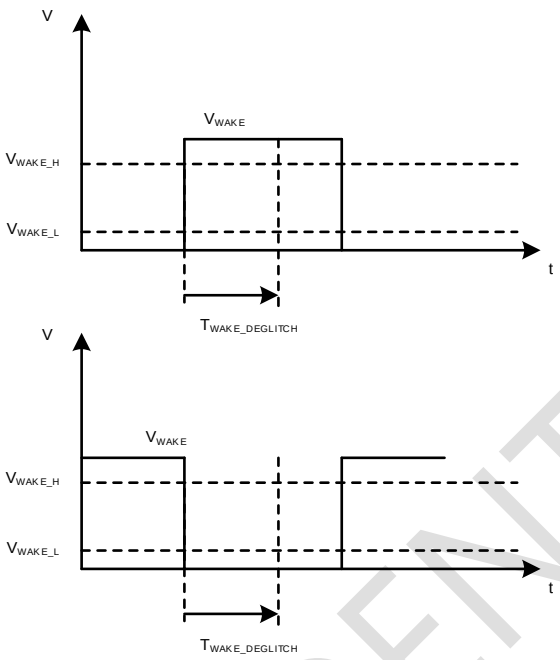


Figure 15. Valid wake signal

A valid Wake-up signal will bring the device from STANDBY to INIT state, from SLEEP to WAKE state or from FAILSAFE to INIT state.
A low signal V_{WAKE_L} at pin WAKE as well as a negative going edge at pin EN will have no impact on the state machine and will not initiate a transition between states.
In case a valid Wake-up signal is detected during the transition phase from NORMAL to SLEEP state, the device will initiate a transition to WAKE state and generate an interrupt.
In case a valid Wake-up signal is detected during the transition phase from NORMAL to STANDBY state, the device will initiate a transition to INIT state and a Reset (RESETB) will be generated.
Before sending a SPI transition command, pin EN doesn't have to be brought below V_{EN_L}. Even if pin EN is high (above V_{EN_H}), the SPI transition command will still send the device into SLEEP or STANDBY state.

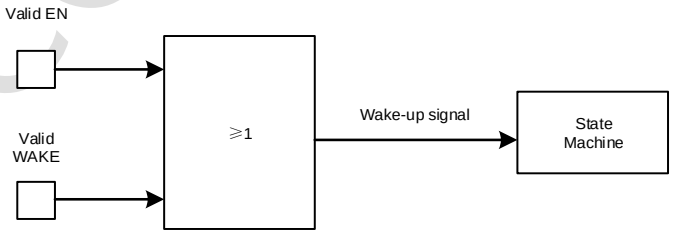


Figure 16. Principle of the enable function

2.2 Wake up Timer

The wake up timer is a function to wake up the SCT61490S.
The wake up timer value may be set by SPI in INIT, NORMAL and WAKE state. The value is stored in the 24 bit wide wake up timer register (**WKTIMCFG0**, **WKTIMCFG1**, **WKTIMCFG2**).
The wake up timer is implemented as a 24 bit counter and the time-base can be selected via SPI.
For the chosen time-base is 8 µs and a wake up time between 8 µs to 134 s can be configured via SPI.
For the chosen time-base is 1 ms and a wake up time between 1 ms to 4.6 hours can be configured via SPI.
For the chosen time-base is 8.192 ms and a wake up time between 8.192 ms to 1.6 days can be configured via

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SPI.
For the chosen time-base is 1 s and a wake up time between 1 s to 194 days can be configured via SPI.
When entering STANDBY or SLEEP state, the counter is loaded with the value of the wake up timer register and starts decrementing. At underflow, the timer will wake up the device from either SLEEP or STANDBY state. When leaving SLEEP state, an interrupt will be generated. The remaining timer counter will be stored if the device wake up before the timer is expired, MCU can read back via SPI to calculate the corresponding time elapsed.

3 Pre Regulators

3.1 Introduction

The pre regulator is mandatory to maintain a stabilized and constant intermediate circuit voltage to supply the following post regulators. It consists of two independent regulators: A HV boost converter with an external power stage in front to maintain a minimum input voltage to the following HV buck converter.
The boost converter can be deactivated (if not needed) by connecting pin EN_BOOST to ground. Leaving pin EN_BOOST open activates the boost regulator.
The buck regulator frequency can be preset by leaving pin FSW open for the high switching frequency range or connecting to GND for the low switching frequency range.
The HV buck converter is constantly on, providing a stabilized intermediate circuit voltage VO_BK1 to supply the following post regulators. The boost converter is connected directly to the input voltage V_{Bat}. It only operates during low input voltage condition (i.e. cold crank) when the input voltage drops below the threshold $V_{PRE_REG,boost,UV}$, to maintain an input voltage high enough for the following buck regulator. Low input voltage condition means, that the input voltage at pin VSUP is too low to provide an intermediate circuit voltage VO_BK1 within the specified limits. An internal comparator connected to the input voltage path detects the threshold when to turn on the boost converter. In case the input voltage is above the boost converter output voltage (threshold for switching on the boost converter), this regulator is deactivated by the internal comparator. An internal logic switches the boost converter on (and off again) whenever it is needed.

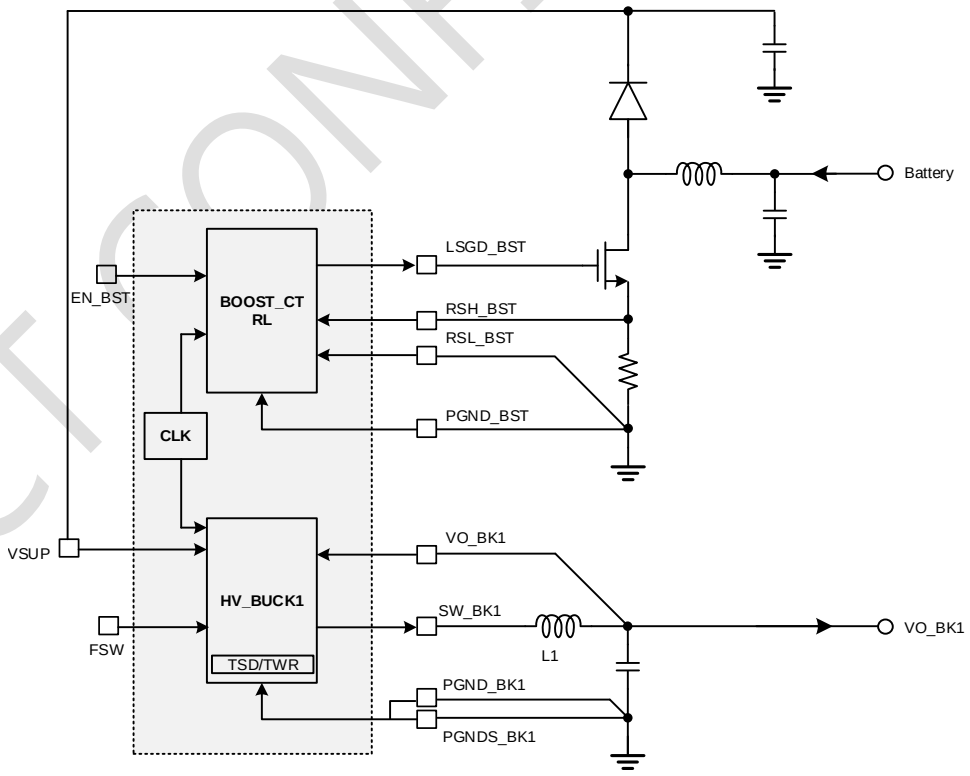


Figure 17. Principle of pre regulator stage

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3.2 HV Boost Regulator

The asynchronous boost pre regulator provides a higher output voltage than the input voltage when operating. This will be the case whenever the supply voltage should be too low to allow nominal values at the post regulator outputs. The boost pre regulator output voltage will be well below the nominal supply (battery) voltage to make sure, that it only operates during low input voltage conditions.
If the boost feature should not be necessary for the application, the external power elements (Mosfet, diode) can be skipped, the filter elements might be adjusted to the application requirements.

3.3 HV Buck Regulator

The synchronous buck pre regulator is continuously in operation providing a stable intermediate circuit voltage to supply the following post regulators. The internal power stage consists of synchronous N-channel (high side) and N-channel (low side) Mosfets. For startup a soft start function is implemented.
The regulation loop operates in peak current mode.
Under normal load conditions the regulator operates in Forced continuous conduction mode (FCCM). Under light load conditions it will operate in Pulse Frequency Modulation (PFM) to minimize the internal current consumption (only in SLEEP state, not in NORMAL, WAKE or INIT state).
The output filter of the buck regulator has to be sized to ensure a maximum output voltage ripple of 100 mV in order to be in line with the PSRR specified for the post regulators.

3.4 Frequency Setting

The frequency source supplies the boost pre regulator and the buck pre regulator with a constant frequency. The synchronous power switches of the buck pre regulator will switch directly with the frequency f_{OSC}.
The frequency range of the buck pre regulator can be set to the high switching frequency range by leaving pin FSW open or to the low switching frequency range by connecting the pin FSW to GND. The switching frequency will be set to the default value of the chosen frequency range. Optionally it can be fine tuned by SPI command (**BCK_FREQ_CHANGE**) or the spread-spectrum option can be activated (**BCK_FRE_SPREAD**).
The switching frequency range of the boost pre regulator is fixed at 500kHz and will be not impacted by FSW pin.
The switching frequency of the buck pre regulator is offered at pin SYNCO for the optional external switch mode post regulator for the µC core supply, if the EN_EXT pin is left open.
The synchronization function is not available in PFM mode.
The SCT61490S cannot be synchronized to an external frequency source.

4 Post Regulators

4.1 Introduction

The SCT61490S includes a number of linear low drop post regulators and offers the possibility to connect an external post regulator for the µC core supply if needed.
The bandgap 1 for regulator block provides the reference values for the error amplifiers of µC supply LDO, the communications supply LDO and the reference voltage source VO_VREF. The trackers get their reference value from the VO_VREF. The output voltage of trackers 1 and 2 is following the reference voltage source VO_VREF with a small drop.
An additional external post regulator can be added to deliver the core supply for the microprocessor. If this option is used the configuration pin EN_EXT must be left open. If the option is not used, pin EN_EXT must be connected to ground. The post regulator is to be connected external and uses its own reference voltage, the input is fed from the pre regulator output voltage VO_BK1. The post regulator is enabled by a high signal at pin SEQ and switched off with a low signal at pin SEQ. A synchronization signal (in phase or shifted by 180 degree with the buck pre regulator signal) is offered at pin SYNCO for usage of a switch mode post regulator. All output voltages of the post regulators are connected to the voltage monitoring function (please refer to chapter **Voltage Monitor**).
In case of an over voltage the related post regulator will be switched off, the shutdown signal is generated by the voltage monitoring function.

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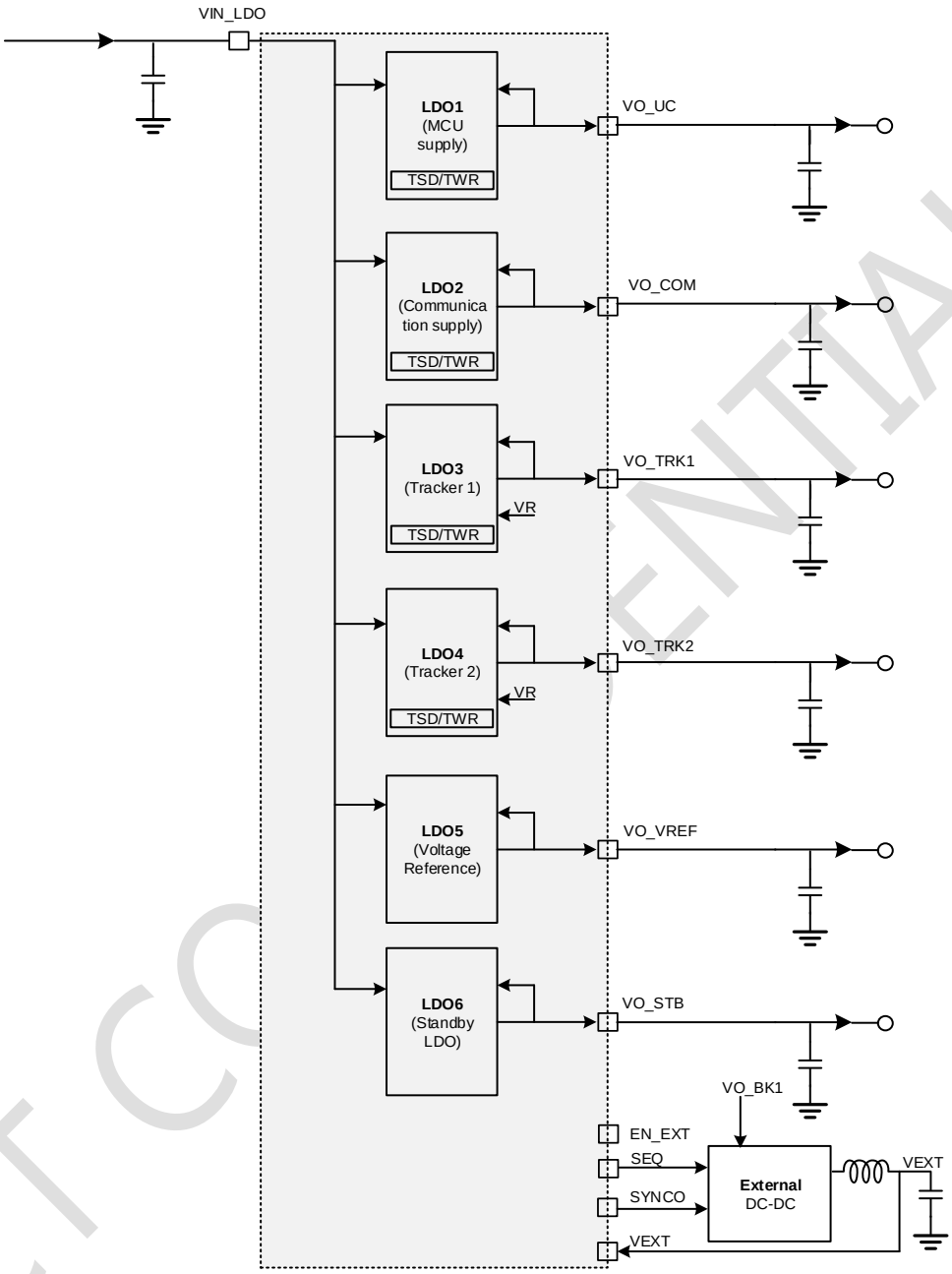


Figure 18. Principle of post regulators

4.2 µ-Processor Supply

The linear low drop regulator LDO_µC offers a precise 3.3 V or 5.0 V output voltage for microprocessor supply. The regulator is supplied from the intermediate circuit voltage VO_BK1 which provides a stabilized voltage. The output voltage VO_UC is controlled by the error amplifier. The actual value is compared to a reference voltage derived from band gap 1 for regulators. The stability of the control loop depends on the load current, the characteristics of the output capacitor and the chip temperature. To ensure a stable operation the output capacitor should be chosen according the specified requirements (capacitance value and electrical series resistance ESR). The input capacitor shown in figure below is the output filter capacitor of the step down pre regulator.

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Protection circuitry is installed to prevent the regulator and the application from damage:

• To protect the pass element of the LDO_µC from overstress the current limitation will limit the output current to the maximum specified limit. Current sensing is done via a current mirror, no sense resistor is used. In case the maximum current condition is reached, the current will be limited, thus the output voltage will decrease. The regulator is protected against short circuit to ground.

• The output voltage is monitored by the voltage monitoring. In case of over voltage at pin VO_UC, the LDO_µC will be switched off and the device will move into FAILSAFE state. The event will be stored in the SPI status register (**MONSF1**). In case of under voltage at pin VO_UC, the device will move into INIT state, pin RESETB will be pulled low and the event will be stored in an SPI status register (**MONSF2**). The regulator will not be switched off in case of output under voltage, which is shorter than the short to ground detection time t_{STG}. If the under voltage should be present for more than t_{STG}, the device will move into FAILSAFE state. This event will be stored in an SPI status register as well (**MONSF0**).

• There is a dedicated temperature sensor for this regulator. In case the power stage temperature exceeds the pre warning threshold, an interrupt will indicate this event and it will be stored in an SPI status register (**OTWRNSF**). If the power stage temperature exceeds the temperature shutdown threshold, the device will move into FAILSAFE state, the regulator will be switched off and the event will be stored in an SPI status register (**OTFAIL**). The off time due to temperature shut down will be at least one second.
If the device enters FAILSAFE state the RESETB is pulled low and all supplies are switched off.
If the device enters STANDBY state the LDO_µC is switched off
For further details please refer to **Chapter State Machine**.

4.3 Communication Supply

The linear low drop regulator LDO_COM offers a precise 5.0 V output voltage for communication supply. The regulator is supplied from the intermediate circuit voltage VO_BK1, which provides a stabilized voltage. The output voltage VO_COM is controlled by the error amplifier. The actual value is compared to a reference voltage derived from band gap 1 for regulators. The stability of the control loop depends on the load current, the characteristics of the output capacitor and the chip temperature. To ensure a stable operation the output capacitor should be chosen according the specified requirements (capacitance value and electrical series resistance ESR). The input capacitor shown in figure below is the output filter capacitor of the step down pre regulator.
Protection circuitry is installed to prevent the regulator and the application from damage:
• To protect the pass element of the LDO_COM from overstress the current limitation will limit the output current to the maximum specified limit. Current sensing is done via a current mirror, no sense resistor is used. In case the maximum current condition is reached, the current will be limited, thus the output voltage will decrease.
The regulator is protected against short circuit to ground.
• The output voltage is monitored by the voltage monitoring. In case of over voltage at pin VO_COM, the LDO_COM will be switched off, the event will be indicated by an interrupt and stored in an SPI status register (**MONSF1**). In case of under voltage at pin VO_COM, the event will be indicated by an interrupt and stored in an SPI status register (**MONSF2**). The regulator will not be switched off in case of output under voltage, which is shorter than the short to ground detection time t_{STG}. If the under voltage should be present for more than t_{STG}, the regulator will be switched off. This event will be stored in the SPI status register (**MONSF0**) and an interrupt will be generated.
• There is a dedicated temperature sensor for this regulator. In case the power stage temperature exceeds the pre warning threshold, an interrupt will indicate this event and it will be stored in an SPI status register (**OTWRNSF**). If the power stage temperature exceeds the temperature shutdown threshold, this event will be stored in an SPI status register (**OTFAIL**), the regulator will be switched off and an interrupt will be generated.
After a temperature shut down the LDO_COM can be re enabled via SPI command.
The regulator LDO_COM is switched off in STANDBY and FAILSAFE state. In INIT, SLEEP, NORMAL and WAKE state LDO_COM is ON or OFF depending on the SPI configuration.
For further details please refer to **Chapter State Machine**.

4.4 Voltage Reference

The linear low drop regulator LDO_VREF offers a highly precise 5.0 V output voltage as a voltage reference. The regulator is supplied from the intermediate circuit voltage VO_BK1, which provides a stabilized voltage. The output

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voltage VO_VREF is controlled by the error amplifier. The actual value is compared to a reference voltage derived from band gap 1 for regulators. The stability of the control loop depends on the load current, the characteristics of the output capacitor and the chip temperature. To ensure a stable operation the output capacitor should be chosen according the specified requirements (capacitance value and electrical series resistance ESR). The input capacitor shown in figure below is the output filter capacitor of the step down pre regulator.
Protection circuitry is installed to prevent the regulator and the application from damage:

• To protect the pass element of the LDO_VREF from overstress the current limitation will limit the output current to the maximum specified limit. Current sensing is done via a current mirror, no sense resistor is used. In case the maximum current condition is reached the current will be limited, thus the output voltage will decrease. The regulator is protected against short circuit to ground.

• The output voltage is monitored by the voltage monitoring. In case of over voltage at pin VO_VREF, the LDO_VREF will be switched off and the device will move into FAILSAFE state. The event will be stored in an SPI status register (**MONSF1**). In case of under voltage at pin VO_VREF, the event will be indicated by an interrupt and stored in an SPI status register (**MONSF2**). The regulator will not be switched off in case of output under voltage, which is shorter than the short to ground detection time t_{STG}. If the under voltage should be present for more than t_{STG}, the regulator will be switched off. This event will be stored in an SPI status register (**MONSF0**) and an interrupt will be generated.

• There is no dedicated temperature sensor for this regulator. The temperature is sensed on the chip by other temperature sensors located at LDO_µC and step down pre regulator. In case of the chip temperature will exceed the pre warning threshold, an interrupt will indicate this event and it will be stored in a SPI status register (**OTWRNSF**). If the chip temperature will exceed the temperature shutdown threshold, the regulator will be switched off. The temperature switch off time will be at least one second. An overload at LDO LDO_VREF (over current detected for more than 1ms) will be indicated by an interrupt and it will be stored in a SPI status register (**OTWRNSF**).
If the device enters FAILSAFE state the RESETB is pulled low and all supplies are switched off.
The regulator LDO_VREF is switched off in STANDBY and FAILSAFE state. In INIT, SLEEP, NORMAL and WAKE state LDO_VREF is ON or OFF depending on the SPI configuration.
For further details please refer to **Chapter State Machine**.

4.5 Tracker 1 & 2

The linear trackers 1 and 2 offer a sensor supply with a very high accuracy referred to voltage reference output (pin VO_VREF).
Both trackers are supplied by the intermediate circuit voltage VO_BK1, which provides a stabilized voltage. The output voltage VO_TRKx is controlled by the error amplifier. The actual value is compared to a reference voltage provided by the reference voltage VO_VREF. The tracker output voltages follow the VO_VREF output with a very small drop. The stability of the control loop depends on the load current, the characteristics of the output capacitor and the chip temperature. To ensure a stable operation the output capacitor for each tracker should be chosen according the specified requirements (capacitance value and electrical series resistance ESR). The input capacitor shown in figure below is the output filter capacitor of the step down pre regulator.
Protection circuitry is installed to prevent damage to both trackers and the application:

• To protect the pass element of a tracker from overstress the current limitation will limit the output current to the maximum specified limit. Current sensing is done via a current mirror, no sense resistor is used. In case the maximum current condition is reached, the current will be limited and in consequence the output voltage will decrease. A tracker is protected against short circuit to ground and short circuit to battery voltage.

• The output voltage is monitored by the voltage monitoring. In case of over voltage at pin VO_TRKx, the corresponding tracker will be switched off, the event will be stored in an SPI status register (MONSF1) and an interrupt will be generated. In case of under voltage at pin VO_TRKx, the event will be stored in an SPI status register (**MONSF2**) and an interrupt will be generated. The tracker will not be switched off in case of output under voltage, which is shorter than the short to ground detection time t_{STG}. If the under voltage should be present for more than t_{STG}, the tracker will be switched off. This event will be stored in an SPI status register (**MONSF0**) and an interrupt will be generated.

• The tracker is capable to withstand a short circuit either to ground or to battery voltage without receiving a damage. In case of a short circuit to battery voltage and if the battery voltage is above the tracker over voltage threshold, the

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tracker will be switched off, the event will be stored in the SPI status register (**MONSF1**).

• There is no dedicated temperature sensor for this regulator. The temperature is sensed on the chip by other temperature sensors located at LDO_µC and step down pre regulator. In case of the chip temperature will exceed the pre warning threshold, the event will be stored in an SPI status register (**OTWRNSF**) and an interrupt will be generated. If the chip temperature exceeds the temperature shutdown threshold, the tracker will be switched off. The temperature switch off time is at least one second.

Both trackers are switched off in STANDBY and FAILSAFE. In INIT, NORMAL, SLEEP and WAKE state each tracker is ON or OFF depending on the SPI configuration.

4.6 Integrated LV Buck Regulator

The internal synchronous buck offers a 0.6-1.87V (with 10mV step) and up to 4A current capabilitys for core voltage supply. The LV buck2 is supplied by the intermediate circuit voltage VO_BK1.

The switching frequency of LV buck2 is fixed at 2.2MHz. The FSS circuitry shifts the switching frequency range and triangular or pseudo modulation. To further improve the EMI performance, the LV buck2 and HV buck1 will operate with 180° phase-shifted clock. The regulation loop operates in constant one time (COT) mode. Under normal load conditions the regulator operates in Forced continuous conduction mode (FCCM). Under light load conditions it will operate in Pulse Frequency Modulation (PFM) to minimize the internal current consumption (only in SLEEP state, not in NORMAL, WAKE or INIT state).

The stability of the control loop depends on the load current, the characteristics of the output capacitor and the chip temperature. To ensure a stable operation the output capacitor for LV buck2 should be chosen at least 47µF and 100µF is recommended.

Protection circuitry is installed to prevent damage:

• To protect the pass element of a tracker from overstress the current limitation will limit the output current to the maximum specified limit. Current sensing is done via a current mirror, no sense resistor is used. In case the maximum current condition is reached, the current will be limited and in consequence the output voltage will decrease.

• The output voltage is monitored by the voltage monitoring. In case of over voltage at pin VO_BK2, the LV buck2 will be switched off, and the device will move into FAILSAFE state. The event will be stored in the SPI status register (**MONSF1**). In case of under voltage at pin VO_BK2, the device will move into INIT state, pin RESETB will be pulled low and the event will be stored in an SPI status register (**MONSF2**). The regulator will not be switched off in case of output under voltage, which is shorter than the short to ground detection time t_{STG}. If the under voltage should be present for more than t_{STG}, the device will move into FAILSAFE state. This event will be stored in an SPI status register as well (**MONSF0**).

• The buck2 is capable to withstand a short circuit to ground. The event will be stored in the SPI status register (**MONSF1**).

• There is a dedicated temperature sensor for this regulator. The temperature is sensed on the power MOSFET of the buck2. In case of the chip temperature will exceed the pre warning threshold, the event will be stored in an SPI status register (**OTWRNSF**) and an interrupt will be generated. If the chip temperature exceeds the temperature shutdown threshold, the tracker will be switched off. The temperature switch off time is at least one second.

LV buck2 are switched off in STANDBY and FAILSAFE. In INIT, NORMAL, SLEEP and WAKE state LV buck2 is ON or OFF depending on the SPI configuration.

4.7 External Post Regulator for Core Supply (optional)

An additional external post regulator may be added to the SCT61490S to provide the core supply voltage for the µC if needed.

In this case the configuration pin EN_EXT has to be left open to indicate that the external core voltage supply option is active. The configuration of the EN_EXT pin will only be read during the power sequencing at the point the core supply would be started.

The regulator is fed from the intermediate circuit voltage VO_BK1. The post regulator is enabled by a high signal at pin SEQ and switched off by a low signal at pin SEQ. The SEQ signal is controlled by the state machine. For example a detection of over voltage at pin VEXT will create a low signal at pin SEQ and shut down the post regulator

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to protect the µC core.
The device offers a synchronization signal of 50% duty cycle at pin SYNCO equal in phase (only with a very small delay) and frequency or shifted by 180 degree to the internal step down pre regulator (the selection is done via SPI command). It is highly recommended to synchronize the external switch mode post regulator to this signal to avoid interferences. The external post regulator will be enabled as soon as the pre regulator output voltage VO_BK1 is present and the VO_UC is above the lower reset threshold.
The output voltage of the post regulator will be monitored by the reset function of the device. To obtain a proper monitoring the output voltage of the post regulator has to be connected to the voltage monitoring input at pin VEXT via a resistor divider. The resistor divider should be dimensioned to adjust the post regulator output voltage to the internal reset reference voltage.
The synchronization signal at pin SYNCO can be switched on via SPI command, default configuration is off. Protection circuitry should be installed to prevent the external regulator and the application from damage:

• To protect the pass device(s) of the external post regulator from overstress a current limitation function should limit the output current to the maximum specified limit. Current sensing should be done via a current mirror, no sense resistor should be used. In case the maximum current should occur, it will be limited, thus the output voltage will decrease. The regulator should be protected against short circuit to ground.

• The output voltage is monitored by the voltage monitoring of the SCT61490S, no further reset function is required on the external post regulator. In case such a reset function should be present, it will not be used or supported by the reset function of the SCT61490S. In case of over voltage at pin VEXT the external post regulator will be switched off by pulling pin SEQ to low and the SCT61490S will move into FAILSAFE state. The event will be stored in an SPI status register (**MONSF1**). In case of under voltage at pin VEXT, the device will move into INIT state, pin RESETB will be pulled low and the event will be stored in an SPI status register (**MONSF2**). The external post regulator will not be switched off in case of output under voltage, which is shorter than the short to ground detection time t_{StG}. If the under voltage is present for more than t_{STG}, the device will move into FAILSAFE state. This event will be stored in an SPI status register as well (**MONSF0**).

• There should be a temperature shutdown function at the external post regulator. If the power stage temperature should exceed the temperature shutdown threshold, the post regulator should be switched off by its own temperature shutdown. The SCT61490S will recognize this as an under voltage and react as described above.

4.8 Power Sequencing

The SCT61490S includes a power sequencing function to ensure a proper ramping up of all output voltages. After the internal Power-On-Reset (POR) is released the standby regulator and the pre regulator start to operate.
In case of one of the microcontroller related voltages (VO_STB, VO_UC, VO_BK1, VO_BK2 or VEXT) cannot be ramped up (e.g. short to GND), the power sequence is stopped and reset output is asserted. The device will move to FAILSAFE state.
In case of one of the non microcontroller related voltages (VO_VREF, VO_COM, VO_TRK1 or VO_TRK2) cannot be ramped up (e.g. short to GND), the power sequence is stopped, but the reset output is still released after the power on reset delay time t_{RD}. The microcontroller should check the status of the outputs by reading the SPI status register (**VMONSTAT**).
In case the microcontroller is sending a SPI request to enable or disable any non microcontroller related LDO (VO_VREF, VO_COM, VO_TRK1 or VO_TRK2) during the power sequencing, the sequence will be stopped and the requested configuration will be executed.

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4.8.1 Power Sequencing from POR to INIT state

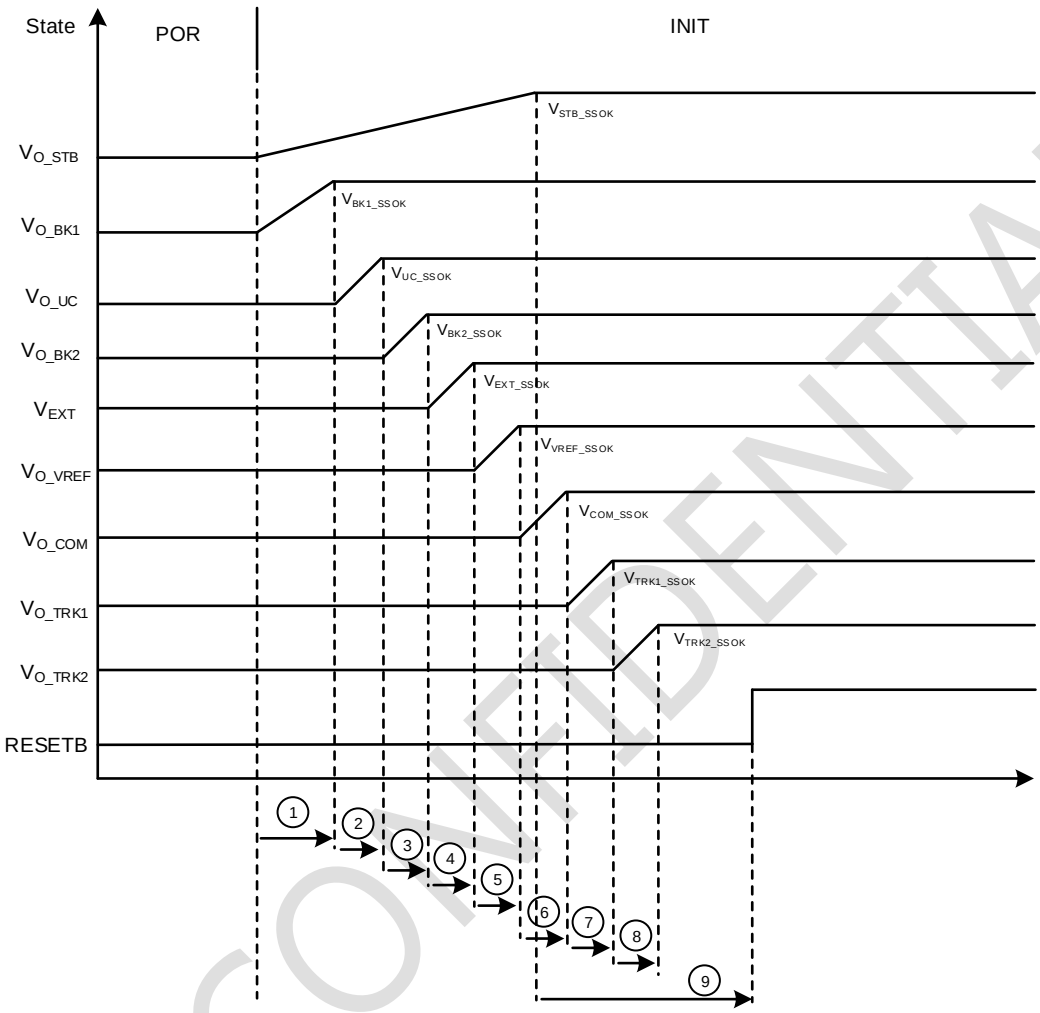


Figure 19. Power sequencing POR to INIT state

1. After POR is released the standby regulator and the pre regulator start to operate.
2. Once the VO_BK1 soft start is finished, the LDO_UC starts to operate.
3. Once the VO_UC soft start is finished, the LV Buck2 for core voltage VO_BK2 starts to operate.
4. Once the VO_BK2 soft start is finished, the external core supply will be enabled, when selected. If the external core supply is not selected, the voltage reference LDO starts to operate.
5. If the external core supply is selected and VEXT soft start is finished, the voltage VO_VREF starts to operate.
6. Once the VO_VREF soft start is finished, the LDO_COM starts to operate.
7. Once the VO_COM soft start is finished, the Tracker 1 starts to operate.
8. Once the VO_TRK1 soft start is finished, the Tracker 2 starts to operate.
9. The reset delay time t_{RD} starts after VO_STB, VO_UC and the external core supply (if selected) have completed their soft start. The reset delay time is programmable via SPI. After the rest delay time is expired, the RESETB pin is pulled to high. The figure shows the possibilities of the t_{RD} starting time.

Once the RESETB is high, the microcontroller can change the configuration of the selectable LDOs which might change the power sequencing accordingly.

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4.8.2 Power Sequencing from STANDBY to INIT state

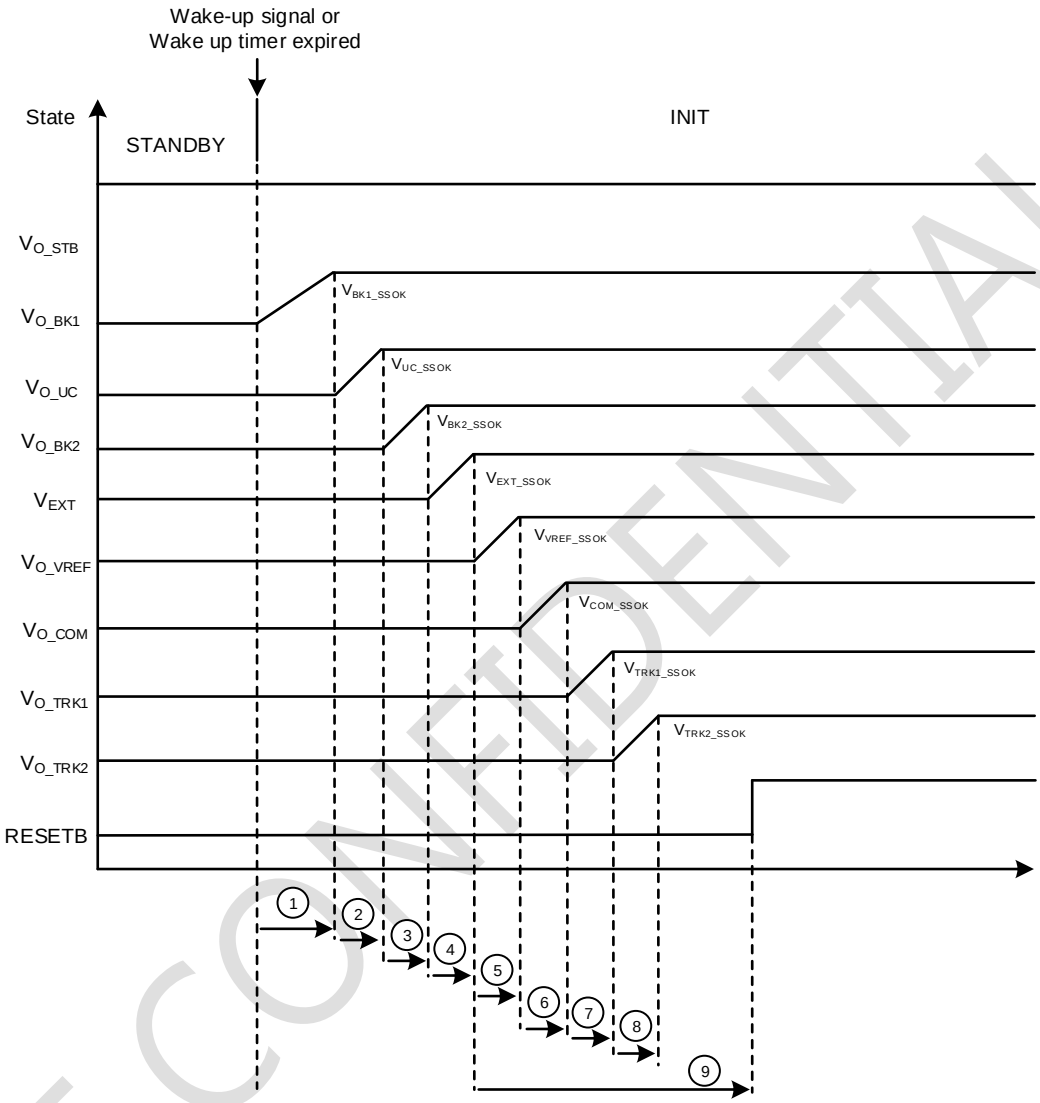


Figure 20. Power sequencing STANDBY to INIT state

Description: Input voltage is present, device is in STANDBY state, LDO_STB is active.
1. After a valid Wake-up signal or an expired wake-up timer the pre regulator starts to operate.
2. Once the VO_BK1 soft start is finished, the LDO_µC starts to operate.
3. Once the VO_UC soft start is finished, the LV Buck2 for core voltage VO_BK2 starts to operate.
4. Once the VO_BK2 soft start is finished, the external core supply will be enabled, when selected. If the external core supply is not selected, the voltage reference LDO starts to operate.
5. If the external core supply is selected and VEXT soft start is finished, the voltage VO_VREF starts to operate.
6. Once the VO_VREF soft start is finished, the LDO_COM starts to operate.
7. Once the VO_COM soft start is finished, the Tracker 1 starts to operate.
8. Once the VO_TRK1 soft start is finished, the Tracker 2 starts to operate.
9. The reset delay time t_{RD} starts after LDO_µC and the external core supply (if selected) have completed their soft start. The reset delay time is programmable via SPI. After the rest delay time is expired the RESETB pin is pulled to high. The figure shows the possibilities of the t_{RD} starting time.

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4.8.3 Power Sequencing from SLEEP to WAKE state

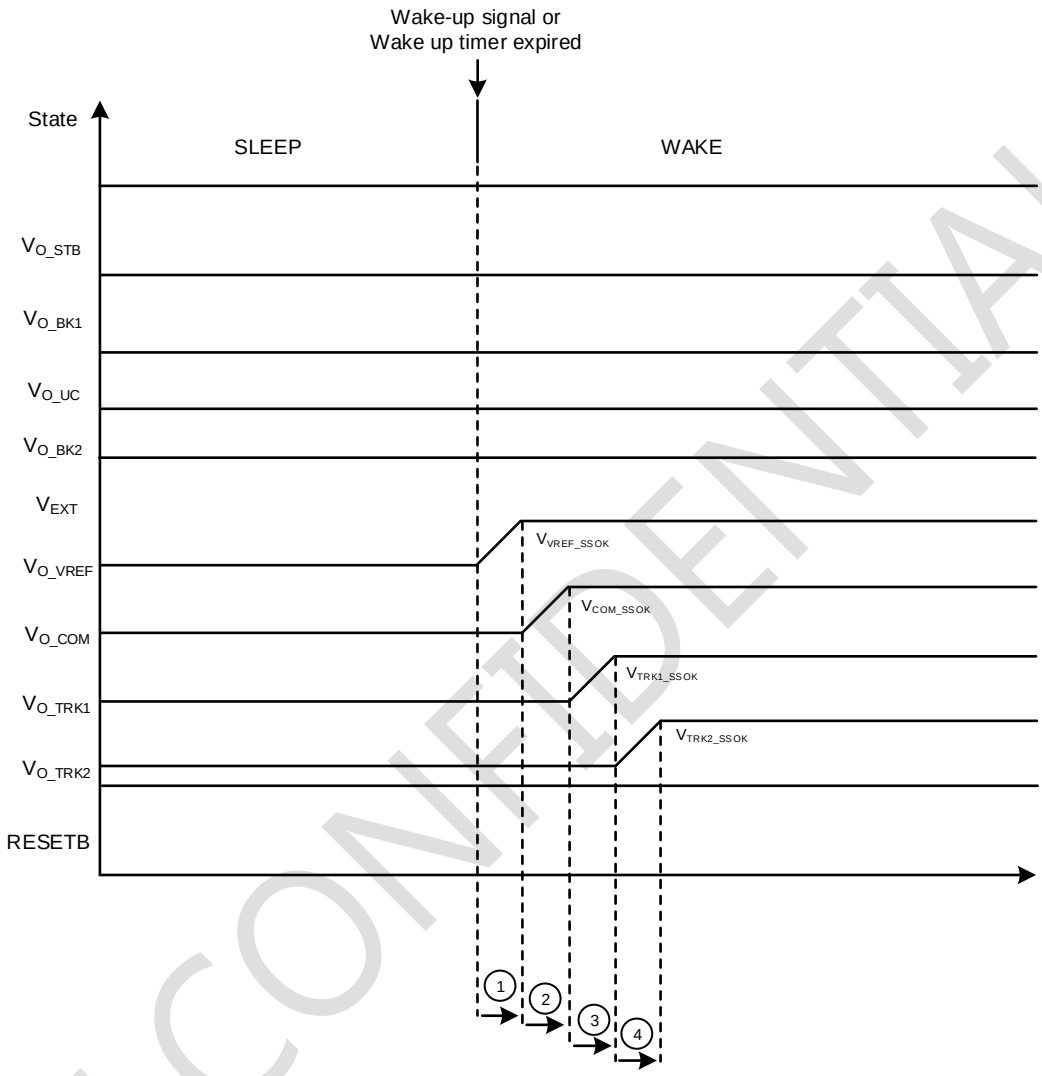


Figure 21. Power sequencing SLEEP to WAKE state

Description: Input voltage is present, device is in SLEEP state, all selectable LDOs switched off in SLEEP state, all selectable LDOs were switched on in previous NORMAL state:
1. After a valid Wake-up signal or an expired wake-up timer the voltage reference starts to operate.
2. Once the VO_VREF soft start is finished, the LDO_COM starts to operate.
3. Once the VO_COM soft start is finished, the Tracker 1 starts to operate.
4. Once the VO_TRK1 soft start is finished, the Tracker 2 starts to operate.

The reset output RESETB is high in SLEEP state and will be kept high for WAKE state.
In case a selectable LDO was switched off in the previous NORMAL state, it will not be enabled during the transition from SLEEP to WAKE, the power sequencing will follow up with the next LDO. In case a LDO was enabled during SLEEP state and was enabled in the previous NORMAL state, it will be kept enabled.

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5 Voltage Monitor

5.1 Introduction

The SCT61490S includes an independent voltage monitoring function of all output voltages, including the optional external post regulator for µC core supply, if in use.
The monitoring function consists of two comparators for each output voltage. One is for detecting over voltage, the other is for detecting under voltage. Both comparators get their reference value from an independent bandgap only used for the voltage monitoring block. This bandgap is independent from the voltage regulator bandgap. The bandgap provides the reference value for over voltage detection (highvoltage reset threshold) and for under voltage detection (low voltage reset threshold). Under normal operation conditions the output voltage of the related regulator has to stay within the voltage window defined by the upper limit and the lower limit.
There is a dedicated temperature sensor for the monitoring block. If the power stage temperature exceeds the temperature shutdown threshold, the device will move into FAILSAFE state, the regulator will be switched off and the event will be stored in an SPI status register (**OTFAIL**). The off time due to temperature shut down will be at least one second.

Characteristics:

The behavior of the over and under voltage comparators is as following:

• The upper limits and the lower limits are fixed for every regulator and cannot be programmed or varied by SPI command.

• An over voltage will be detected if the regulator output voltage is higher than the related over voltage reset threshold for more than the reset reaction time t_{RR}. An over voltage higher than the related over voltage reset threshold which is present for shorter than the reset reaction time t_{RR} will be regarded as a spike and will not be detected.

An under voltage will be detected if the regulator output voltage is lower than the related under voltage reset threshold for more than the reset reaction time t_{RR}. An under voltage lower than the related under voltage reset threshold which is present for shorter than the reset reaction time t_{RR} will be regarded as a spike and will not be detected.

• The reset reaction time t_{RR} is not valid for the internal voltage supplies in case of under and over voltage.

• The detection of an over voltage will shut down the related regulator immediately to protect the loads from harm or destruction. This shut down may lead (depending on the affected regulator) to further action, please refer to chapter **State Machine** for details.

• The detection of an under voltage will not shut down the related regulator.

• The post regulators (including the optional external post regulator for µC core supply) have a short to ground detection. If the detected under voltage is present for more than the short to ground detection time t_{STG}, the related regulator will shut down to protect itself and the chip from over heating. This shut down may lead (depending on the affected regulator) to further action, please refer to chapter **State Machine** for details. (It is mandatory that the external post regulator for µC core supply has an enable or inhibit function).

• The over and under voltage detection is active only if the related regulator is in use (including the external post regulator for µC core supply) and switched on.

Indication of over and under voltage:

Depending on the related regulator the indication of over and under voltage will be different, either by reset signal or by interrupt indication:

• Every over and under voltage detection will be stored in the SPI status register (**MONSF0**, **MONSF1**, **MONSF2**).

• For µC related output voltages (VO_STB, VO_UC, VO_BK2, VEXT), over and under voltage are indicated by the hardware reset pin RESETB. In case of an over or under voltage, pin RESETB is pulled to low.

• In case of over voltage or a detection of a short to ground at the external post regulator for µC core supply, the pin SEQ will be pulled to low to shut down the regulator.

• For the pre regulator output (VO_BK1) and the voltage reference output (VO_VREF) only over voltage is indicated by the hardware reset pin RESETB. In case of an over voltage, pin RESETB is pulled to low.

• For the pre regulator output and the voltage reference output, only under voltage is indicated by an interrupt.

• For all not µC related output voltages (VO_COM, VO_TRK1, VO_TRK2), over and under voltage are indicated by an interrupt.

• For the internal supply voltages, over and under voltage are indicated by the hardware reset pin RESETB. In case of an over or under voltage, pin RESETB is pulled to low.

Table1 Indication Pin Matrix

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Regulators	OV Indication Pin	UV Indication Pin	STG Indication Pin
VO_STB	RESETB	RESETB	RESETB
VO_UC	RESETB	RESETB	RESETB
VO_BK2	RESETB	RESETB	RESETB
VEXT	RESETB/INTB selectable	RESETB/INTB selectable	RESETB/INTB selectable
VO_BK1	RESETB	INTB	RESETB
VO_COM	INTB	INTB	INTB
VO_VREF	RESETB/INTB selectable	INTB	INTB
VO_TRK1	INTB	INTB	INTB
VO_TRK2	INTB	INTB	INTB
VSUP	RESETB/INTB selectable	RESETB	NA
VCC	RESETB	RESETB	NA
Bandgap1,2	INTB	INTB	NA

5.2 Shutdown Function

A short to ground detection time t_{STG} at the pre regulator output is only active during the power sequence in INIT state. If the output voltage of the pre regulator should not be within the specified limits within a certain time frame, the device will move into FAILSAFE state. Once VO_BK1 has entered a valid range following the completion of soft start, no reaction will be triggered on a detected short to ground. If the output voltage of the pre regulator should be too low in other cases, the behavior of the device will depend on the voltage monitoring of the post regulators.
The detection of an over voltage at output voltages VO_UC, VEXT, VO_STB, VO_VREF, VO_BK2 or VO_BK1 will shut down all regulators to protect the loads from harm or destruction and moves the device to FAILSAFE.
The detection of an over voltage at output voltages VO_COM, VO_TRK1, VO_TRK2 will shut down the related regulator to protect the loads from harm or destruction and generate an interrupt event.
If the detected under voltage at output voltages VO_UC, VEXT, VO_BK2 or VO_STB should be present for more than the short to ground detection time t_{STG}, all regulators will shut down to protect themselves and the chip from over heating and move the device to FAILSAFE.
If the detected under voltage at output voltages VO_VREF, VO_COM, VO_TRK1, VO_TRK2 should be present for more than the short to ground detection time t_{STG}, the related regulator will shut down to protect itself and the chip from over heating and generate an interrupt event.
The detection of an over voltage or under voltage at power supply voltage VSUP, internal supply voltage VCC will shut down all regulators.

Table2 Shutdown Matrix

Output	OV	UV	STG
VO_STB	All regulators shut down	No shut down	All regulators shut down
VO_UC	All regulators shut down	No shut down	All regulators shut down
VO_BK2	All regulators shut down	No shut down	All regulators shut down
VEXT	All regulators shut down/No shutdown, selectable;Assert EN_EXT	No shut down	All regulators shut down/No shutdown, selectable;Assert EN_EXT
VO_BK1	All regulators shut down	No shut down	All regulators shut down
VO_COM	VO_COM shutdown	No shut down	VO_COM shutdown
VO_VREF	All regulators shut down/No shutdown, selectable	No shut down	Related regulators shut down
VO_TRK1	VO_TRK1 shutdown	No shut down	VO_TRK1 shutdown
VO_TRK2	VO_TRK2 shutdown	No shut down	VO_TRK2 shutdown
VSUP	All regulators shut down/No shutdown, selectable	All regulators shut down	NA
VCC	All regulators shut down	All regulators shut down	NA

5.3 Reset Function

The reset generator starts to operate as soon as the internal POR is released.

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It is called a “Soft Reset” if pin RESETB goes low, but the pre and post regulator output voltages are not switched off.
It is called a “Hard Reset” if pin RESETB goes low and the post regulator output voltages are switched off. The power sequencing will be restarted after a delay of t_{SDT}.(Applicable to the second initialization timeout in a row).
The reset output pin RESETB is an open drain structure. As soon as a reset condition occurs, the RESETB pin is pulled low. An internal pull up current is pulling the output towards VO_UC.
The contribution of regulators to reset is shown in Table1. Besides, IBIAS monitoring is contributing to trigger a reset. The IBIAS monitor fault is stored in a status bit (**BIASHI** or **BIASLOW**).

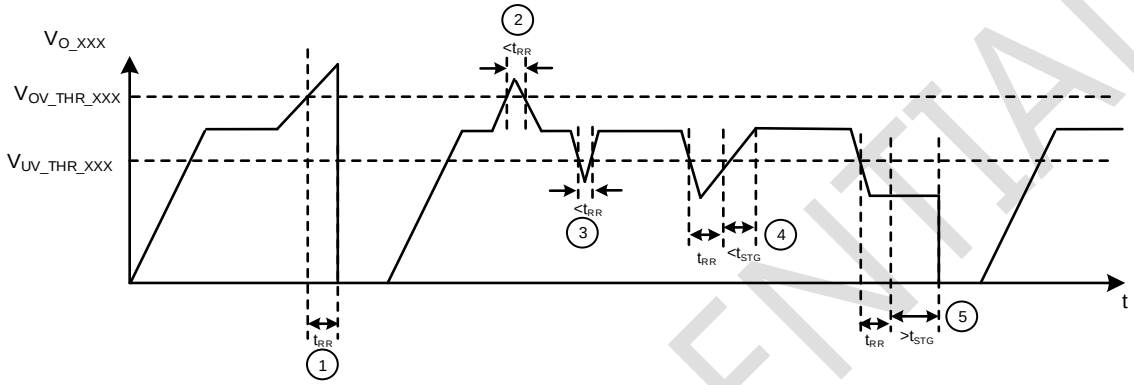


Figure 22. Timing diagram hardware reset signal RESETB for output voltages

1. Voltage exceeds OV threshold and last for longer than $t_{RR,}$ OV event is triggered.

2. Voltage exceeds OV threshold but last for shorter than t_{RR}, OV event is not triggered.

3. Voltage falls below UV threshold but last for shorter than t_{RR}, UV event is not triggered.

4. Voltage falls below UV threshold and last for longer than t_{RR}, UV event is triggered. After UV event is triggered, voltage still lower than UV threshold but last for shorter than t_{STG}, STG event is not triggered.

5.Voltage falls below UV threshold and last for longer than t_{RR}, UV event is triggered. After UV event is triggered, voltage still lower than UV threshold and last for longer than t_{STG}, STG event is triggered.

5.4 Interrupt Function

The interrupt generator starts to operate as soon as the internal POR is released.
The voltage monitoring function supervises the values of the non µC related post regulator output voltages VO_COM, VO_TRK1 and VO_TRK2, the pre regulator output voltage VO_BK1 (under voltage only) and the voltage reference output VO_VREF (under voltage and short to ground only). The result is written in a SPI status register (**IF** and **MONSF0**, **MONSF1** or **MONSF2**) and indicated via interrupt (pin INTB). The connection of all these monitoring signals is a logic OR. The interrupt pin INT does not only indicate the result of the voltage monitoring, but also interrupts due to other events in the device.
The interrupt output pin INT is a push pull structure. An interrupt is indicated by pulling the INTB pin to ground. The contribution of regulators to interrupt is shown in Table1.

6 Standby LDO and Internal Supplies

6.1 Standby LDO VO_STB

The standby regulator LDO_STB is independent from the pre regulator stage and the other post regulators. It might be switched ON or OFF in all states (for details please refer to chapter **State Machine**). The linear low drop regulator LDO_STB offers a precise 3.3 V (or 5.0 V, equal to LDO_µC) output voltage for standby supply.
The LDO_STB will keep its state by leaving the STANDBY state according to its previous configuration. For

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STANDBY state, the status of LDO_STB (ON or OFF) has to be defined in previous states.
The regulator is supplied from pin VIN_STB. Depending on the needs of the application pin VIN_STB might be connected directly to battery voltage (protected by reverse polarity diode) or to the output of the step up pre regulator.
The output voltage V_{O_STB} (at pin VO_STB) is controlled by the error amplifier. The actual value is compared to a reference voltage derived from band gap 1 for regulators. The stability of the control loop is depending on the load current, the characteristics of the output capacitor and the chip temperature. To ensure stable operation the output capacitor should be chosen according the specified requirements (capacitance value and electrical series resistance ESR) in table “Electrical characteristics”.
Protection circuitry is installed to prevent the regulator and the application from damage:
• To protect the pass element from overstress the current limitation will limit the output current to the maximum specified limit. Current sensing is done via a current mirror, no sense resistor is used. In case the maximum current should occur, it will be limited., thus the output voltage will decrease. The regulator is protected against short circuit to ground.
• The output voltage is monitored by the voltage monitoring. In case of over voltage at pin VO_STB, the LDO_STB will be switched off and the device will move into FAILSAFE state. The event will be stored in an SPI status register (**MONSF1**). In case of under voltage at pin VO_STB, the device will move into INIT state, pin RESETB will be pulled low and the event will be stored in an SPI status register (**MONSF2**). The regulator will not be switched off in case of output under voltage, which is shorter than the short to ground detection time t_{STG}. If the under voltage should be present for more than t_{STG}, the device will move into FAILSAFE state. This event will be stored in an SPI status register as well (**MONSF0**).
• There is no dedicated temperature sensor for this regulator. The temperature is sensed on the chip by other temperature sensors located at LDO_µC and step down pre regulator. In case of the chip temperature will exceed the pre warning threshold, an interrupt will indicate this event and it will be stored in an SPI status register (**OTFAIL**). If the chip temperature will exceed the temperature shutdown threshold, the post regulator will be switched off. The temperature switch off time will be at least one second. An overload at LDO STB
(over current detected for more than 1ms) will be indicated by interrupt, except if the device is in STANDBYstate and the event will be stored in SPI status register (**OTWRNSF**).
The regulator LDO_STB may be configured to be ON or OFF in every state, except FAILSAFE. The selection for STANDBY state shall be done by SPI command before entering this state.

6.2 Internal Supplies

The SCT61490S includes internal voltage supplies and bias currents to operate all regulators, monitoring and logic functions. These internal supplies are monitored internally to ensure proper functionality of the functional blocks the SCT61490S provides. The device will react on internal failure conditions as described in the State Machine, Monitoring Function, Interrupt Generation and Safe State Control Function.
The internal regulators do not require external components (i.e capacitors). The internal voltages are not visible at any pin.

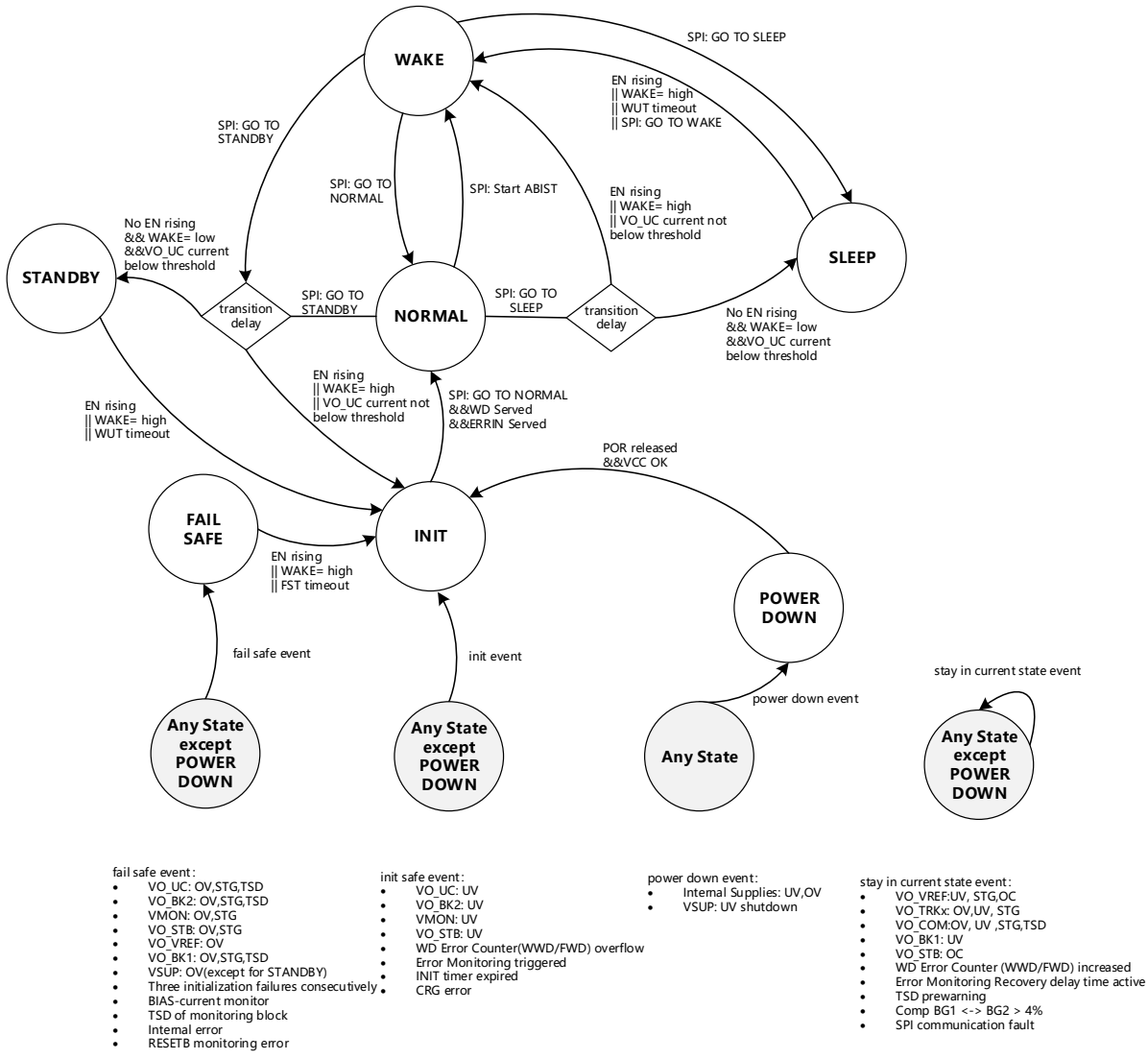
7 State Machine

7.1 Introduction

The state machine describes the different states of operation, the device may get into. The following figure shows the state machine flow diagram, for detailed information please refer to following pages.

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7.2 Detailed Operating States

7.2.1 POWERDOWN state

The device is in POWERDOWN state when supply voltage VSUP is lower than UVLO threshold or internal supplies VCC occurs OV/UV.

Table 3 POWERDOWN Operation State

Block/Function	Status	Description
LDO_STB	OFF	The LDO_STB is off
HV Buck1	OFF	The HV Buck1 is off
LDO_µC	OFF	The LDO_µC is off
LV Buck2	OFF	The LV Buck2 is off

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External Post Regulator	OFF	The External Post Regulator is off
LDO_COM	OFF	The LDO_COM is off
LDO_VREF	OFF	The LDO_VREF B is off
LDO_TRK1&2	OFF	The LDO_TRK1&2 is off
Wakeup Timer	OFF	The Wakeup Timer is off
Watchdog	OFF	The Watchdog is off
ERRIN	OFF	The ERRIN is off
RESETB	LOW	The RESETB pin is low
SS1&SS2	LOW	Both safe state signals are LOW and the application is in safe state

7.2.2 INIT state

After POR, all rails will start-up following a dedicated sequence. The device enters INIT state all outputs are power good. During INIT state the device expects valid communication with the µC within the INIT timer. Otherwise an initialization timeout will occur. The INIT timer starts with the rising edge of RESETB.
The INIT timer is stopped as soon as all three boundary conditions are fulfilled:
• Valid SPI communication received from µC
• Watchdog(s) serviced once according to default configuration or according to reconfiguration
• ERRIN monitoring serviced properly (minimum 3 periods provided) or configured to be OFF

Table 4 INIT Operation State

Block/Function	Status	Description
LDO_STB	SELECTABLE**	• The LDO_STB is switched on when entering from POWERDOWN state • It may be switched on or off by SPI command. This configuration is kept through all states, except POWERDOWN state
HV Buck1	ON	• The HV Buck1 is on • The boost is active depending on the input voltage and this option is selected by pin EN_BST.
LDO_µC	ON	The LDO_µC is on
LV Buck2	ON	The LV Buck2 is on
External Post Regulator	ADJUSTED	The External Post Regulator is switched ON or OFF depending on pin EN_EXT
LDO_COM	ON*	• The LDO_COM is on • The LDO_COM may be switched off or on by SPI
LDO_VREF	ON*	• The LDO_VREF is on • The LDO_VREF may be switched off and on by SPI
LDO_TRK1&2	ON*	• The LDO_TRK1&2 is on • The LDO_TRK1&2 may be switched off and on by SPI
Wakeup Timer	OFF	The Wakeup Timer is off
Watchdog	ON*	• The window watchdog is switched on per default in SPI triggered mode • The functional watchdog is switched off per default • The watchdogs may be configured and switched ON or OFF by SPI
ERRIN	ON	• The Errorin monitoring is switched on per default • The Errorin monitoring may be configured and switched ON or OFF by SPI
RESETB	ACTIVE	The reset output goes HIGH as soon as all µC related output voltages VO_STB, VO_UC and VEXT are above their under voltage reset threshold

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SS1&SS2	LOW	Both safe state signals are LOW and the application is in safe state

7.2.3 NORMAL state

In NORMAL-state the device is supplying the µC and the applications. Safety and monitoring functions (like resetblock and safe state control) are active. The µC may configure several post regulators of the device and the wakeup timer via SPI command for this state.

Table 5 NORMAL Operation State

Block/Function	Status	Description
LDO_STB	SELECTABLE	The LDO_STB may be switched on or off by SPI command.
HV Buck1	ON	• The HV Buck1 is on • The boost is active depending on the input voltage and this option is selected by pin EN_BST.
LDO_µC	ON	The LDO_µC is on
LV Buck2	ON	The LV Buck2 is on
External Post Regulator	ADJUSTED	The External Post Regulator is switched ON or OFF depending on pin EN_EXT
LDO_COM	SELECTABLE	The LDO_COM may be switched off or on by SPI
LDO_VREF	SELECTABLE	The LDO_VREF may be switched off or on by SPI
LDO_TRK1&2	SELECTABLE	The LDO_TRK1&2 may be switched off or on by SPI
Wakeup Timer	OFF	The Wakeup Timer is off
Watchdog	SELECTABLE	The watchdogs may be configured and switched ON or OFF by SPI
ERRIN	SELECTABLE	The Error monitoring may be configured and switched ON or OFF by SPI
RESETB	HIGH	The RESETB pin is high
SS1&SS2	HIGH	Both safe state signals are high

7.2.4 STANDBY state

The STANDBY state is a low power state which the µC may enter to reduce the current consumption to a minimum when the application is not used for a long time. The application is in a safe state.

Table 6 STANDBY Operation State

Block/Function	Status	Description
LDO_STB	SELECTABLE	The LDO_STB may be switched on or off depending on its configuration.
HV Buck1	OFF	The HV Buck1 is off
LDO_µC	OFF	The LDO_µC is off
LV Buck2	OFF	The LV Buck2 is off
External Post Regulator	OFF	The External Post Regulator is off
LDO_COM	OFF	The LDO_COM is off
LDO_VREF	OFF	The LDO_VREF B is off
LDO_TRK1&2	OFF	The LDO_TRK1&2 is off

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Wakeup Timer	SELECTABLE	The wakeup timer may be switched on or off depending on its configuration.
Watchdog	OFF	The Watchdog is off
ERRIN	OFF	The Error monitoring is off
RESETB	LOW	The RESETB pin is low
SS1&SS2	LOW	Both safe state signals are LOW and the application is in safe state

7.2.5 SLEEP state

The device is in POWERDOWN state when supply voltage VSUP is lower than UVLO threshold or internal supplies VCC occurs OV/UV.

Table 7 SLEEP Operation State

Block/Function	Status	Description
LDO_STB	SELECTED	The LDO_STB may be switched on or off depending on its configuration.
HV Buck1	ON	• The HV Buck1 is on • The boost is active depending on the input voltage and this option is selected by pin EN_BST.
LDO_µC	ON	• The LDO_µC is switched on • In SLEEP-state the device is monitoring the output current of LDO_µC: If the LDO_µC current exceeds a certain threshold I_{VUC_ATT} an interrupt will be generated and the device will move to WAKE state
LV Buck2	SELECTED	The LV Buck2 is switched ON or OFF depending on the configuration by the state transition request to move into SLEEP and cannot be changed in SLEEP state.
External Post Regulator	ADJUSTED	The External Post Regulator is switched ON or OFF depending on pin EN_EXT (EN_EXT pin considered only during power-sequencing)
LDO_COM	SELECTED	The LDO_COM is switched ON or OFF depending on the configuration by the state transition request to move into SLEEP and cannot be changed in SLEEP state.
LDO_VREF	SELECTED	The LDO_VREF B is switched ON or OFF depending on the configuration by the state transition request to move into SLEEP and cannot be changed in SLEEP state.
LDO_TRK1&2	SELECTED	The LDO_TRK1&2 is switched ON or OFF depending on the configuration by the state transition request to move into SLEEP and cannot be changed in SLEEP state.
Wakeup Timer	SELECTED	The Wakeup Timer may be switched on or off depending on its configuration.
Watchdog	SELECTED	The Watchdog may be switched on or off depending on its configuration.
ERRIN	SELECTED	The Error monitoring may be switched on or off depending on its configuration.
RESETB	HIGH	The RESETB pin is low
SS1&SS2	LOW	Both safe state signals are LOW and the application is in safe state

7.2.6 WAKE state

The WAKE state is an intermediate state between NORMAL and the low power states SLEEP and STANDBY. This state provides the same functionality as the NORMAL state, but shall ensure the application being in safe state by keeping low the safe state outputs. It should be used to prepare the system for a correct and safe reentry to the NORMAL state by servicing the watchdogs and the error monitoring (minimum 3 periods) according to the selected configuration. Furthermore it provides the possibility to move the device into the low power states SLEEP and STANDBY.

The SCT61490S moves from SLEEP or from the transition to SLEEP into WAKE state, if the output current from LDO_µC exceeds a certain threshold I_{VUC_ATT}, an valid EN or WAKE signal is recognized or the SPI command GoToWake is sent. Another transition into WAKE state is initiated by the usage of the ABIST in NORMAL state.

By entering the state an interrupt is generated and the supervision functions (watchdogs and ERR monitoring) will

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become active according to their previous configuration in NORMAL state. Upon entering the WAKE-state the configuration of the LDOs resumes to the one of the previous NORMAL state. The application is in a safe state

Table 8 WAKE Operation State

Block/Function	Status	Description
LDO_STB	SELECTABLE	The LDO_STB may be switched on or off by SPI command.
HV Buck1	ON	• The HV Buck1 is on • The boost is active depending on the input voltage and this option is selected by pin EN_BST.
LDO_µC	ON	The LDO_µC is on
LV Buck2	SELECTABLE	• The LV Buck2 will be switched ON or OFF depending on its configuration in the NORMAL-state prior to SLEEP-state when entering WAKE-state • It may be switched on of off by SPI command
External Post Regulator	ADJUSTED	The External Post Regulator is switched ON or OFF depending on pin EN_EXT (EN_EXT pin considered only during power-sequencing)
LDO_COM	SELECTABLE	• The LDO_Com will be switched ON or OFF depending on its configuration in the NORMAL-state prior to SLEEP-state when entering WAKE-state • It may be switched on of off by SPI command
LDO_VREF	SELECTABLE	• The voltage reference will be switched ON or OFF depending on its configuration in NORMAL-state prior to SLEEP-state when entering WAKE-state • It may be switched on of off by SPI command
LDO_TRK1&2	SELECTABLE	• Both trackers 1 & 2 will be switched ON or OFF depending on their configuration in NORMAL-state prior to SLEEP-state when entering WAKE-state • It may be switched on of off by SPI command
Wakeup Timer	OFF	The Wakeup Timer is off
Watchdog	SELECTABLE	• The watchdogs will be switched ON or OFF depending on their configuration in NORMAL-State prior to SLEEP-state when entering WAKE-State • The watchdogs may be configured and switched ON or OFF by SPI
ERRIN	SELECTABLE	• The Error monitoring will be switched ON or OFF depending on the configuration in NORMAL-state prior to SLEEP-state when entering WAKE-state • The Error monitoring may be configured and switched ON or OFF by SPI
RESETB	HIGH	The RESETB pin is high
SS1&SS2	LOW	Both safe state signals are LOW and the application is in safe state

7.2.7 FAILSAFE state

FAILSAFE state occurs after the detection of a severe failure. In FAILSAFE-state all regulators are switched off. The application is in a safe state.

Table 9 FAILSAFE Operation State

Block/Function	Status	Description
LDO_STB	OFF	The LDO_STB is off
HV Buck1	OFF	The HV Buck1 is off
LDO_µC	OFF	The LDO_µC is off
LV Buck2	OFF	The LV Buck2 is off
External Post Regulator	OFF	The External Post Regulator is off

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LDO_COM	OFF	The LDO_COM is off
LDO_VREF	OFF	The LDO_VREF B is off
LDO_TRK1&2	OFF	The LDO_TRK1&2 is off
Wakeup Timer	OFF	The Wakeup Timer is off
Watchdog	OFF	The Watchdog is off
ERRIN	OFF	The Error monitoring is off
RESETB	LOW	The RESETB pin is low
SS1&SS2	LOW	Both safe state signals are LOW and the application is in safe state

7.3 Transition Between States

State transitions requested via SPI command are initiated with a valid positive going edge of the chip select.

7.3.1 POWERDOWN → INIT State

The device moves from POWERDOWN to INIT state when the Power-on-Reset (POR) is released. The POR is only released when all of the following conditions are met:
• V_{SUP} above V_{SUP_UVLO} when increasing
• no under or over voltage on internal supplies VCC

7.3.2 INIT → NORMAL State

Prerequisites:
• Watchdog(s) need to be serviced once according to default configuration or according to reconfiguration within the INIT timer
• ERR monitor needs to be serviced with a valid signal (minimum 3 periods) or disabled within the INIT timer.
• If functional watchdog is activated, a valid FWD triggering needs to be provided.
• A delay of 60µs after the provided services has to be considered to ensure proper release of internal validation signals.
Triggering Events:
• State transition is only initiated by the SPI command “Go to NORMAL”.
Exceptions:
• none

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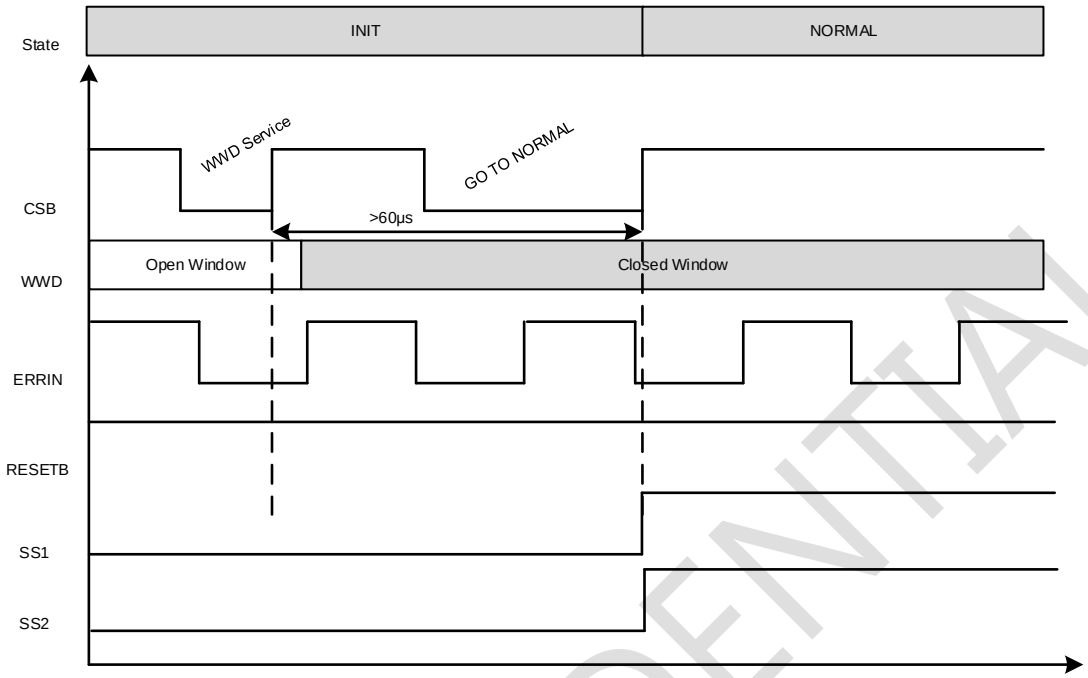


Figure 23. Transition from INIT to NORMAL state

• A valid SPI command “Go to NORMAL” (valid with chip select high at pin CSB) will move the device from INIT state to NORMAL state.
• Reset pin RESETB stays HIGH as the post regulators are already active in INIT state.
• With the positive edge of chip select high (at pin CSB) the safe state signals SS1 and SS2 are pulled to HIGH at same time. (Internal reaction time for the safe state outputs up to 30µs has to be considered)

7.3.3 NORMAL → SLEEP State

Prerequisites:
• Selection of LDO_µC current monitor or absolute transition timer.
• Transition delay timer t_{TR_DEL} needs to be configured or default is used.
• Optionally LDO_µC current threshold needs to be defined or default is used.
Triggering Events:
• State transition is only initiated by the SPI command “Go to SLEEP”.
Exceptions:
• If a valid EN (edge) or WAKE (level) signal is detected in the transition state to SLEEP state, the device will move to the WAKE state and send an interrupt (at pin INTB)
• If the LDO_µC current monitor is activated and the current consumption of the microcontroller is not below the selected LDO_µC current threshold before the transition delay timer t_{TR_DEL} has expired, the device will move to the WAKE state and send an interrupt (at pin INTB)

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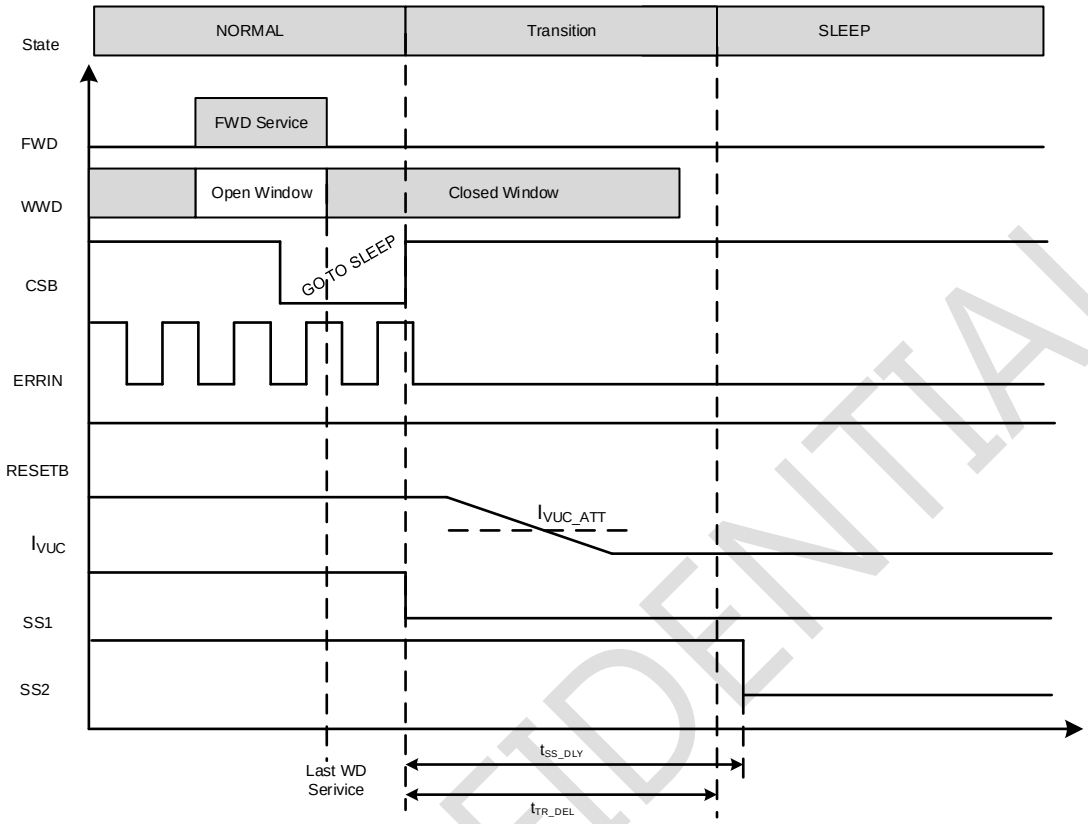


Figure 24. Transition from NORMAL to SLEEP state

Before the SPI command “Go to SLEEP” is applied, the watchdog(s) - if in use should be serviced, so that the positive edge of CSB signal is well in between the “closed window” of the window watchdog. This is recommended to avoid interference between a missing watchdog trigger and the transition command “Go to SLEEP”

• The positive edge of chip select (pin CSB) after the SPI command “Go to SLEEP” initiates the transition. With chip select high the safe state signal SS1 is pulled to zero and the device leaves NORMAL state and enters the transition state (to SLEEP state). (Internal reaction time for the safe state outputs has to be considered)

• With chip select (pin CSB) high the error monitoring (pin ERRIN) is stopped - the toggling may end with the positive edge at pin CSB. If the error monitoring should be selected to be active in SLEEP state continuous toggling is mandatory.

• The monitoring of window watchdog and functional watchdog is stopped with the positive edge at pin CSB. If one or both watchdogs should be selected to be active in SLEEP state continuous watchdog service is mandatory.

• Reset pin RESETB stays high as the post regulators are not switched off.

• In case the absolute transition timer is selected, the device moves from transition state to SLEEP state after the transition delay time t_{TR_DEL}. The transition time t_{TR_DEL} can be determined by SPI command between 100 µs to 1.6 ms, the default setting is 900 µs. After this transition time it should be ensured that the µC current consumption has fallen below the LDO_µC monitoring threshold I_{VUC_ATT} to keep the device in SLEEP state.

• If the LDO_µC current monitor is enabled the µC current out of pin VO_UC must fall below the LDO_µC monitoring threshold I_{VUC_ATT} within the configured maximum transition time t_{TR_DEL} in **DEVCFG0**.**TRDEL**. The time for the transition is depending, how long it takes that the µC current falls below the LDO_µC monitoring threshold I_{VUC_ATT}, if it is below the transition is done.

• After delay time t_{SS_DLY} the safe state signal SS2 goes to zero. The adjusted delay time t_{SS_DLY} is independent from the transition delay time t_{TR_DEL}

7.3.4 SLEEP → WAKE State

Prerequisites:

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• none

Triggering Events:

• SPI command “Go to WAKE”.
• Valid Wake-up signal (EN or WAKE).
• Current of LDO_µC exceeding the configured threshold.
• Wake-up timer expired, if enabled

Exceptions:

• none

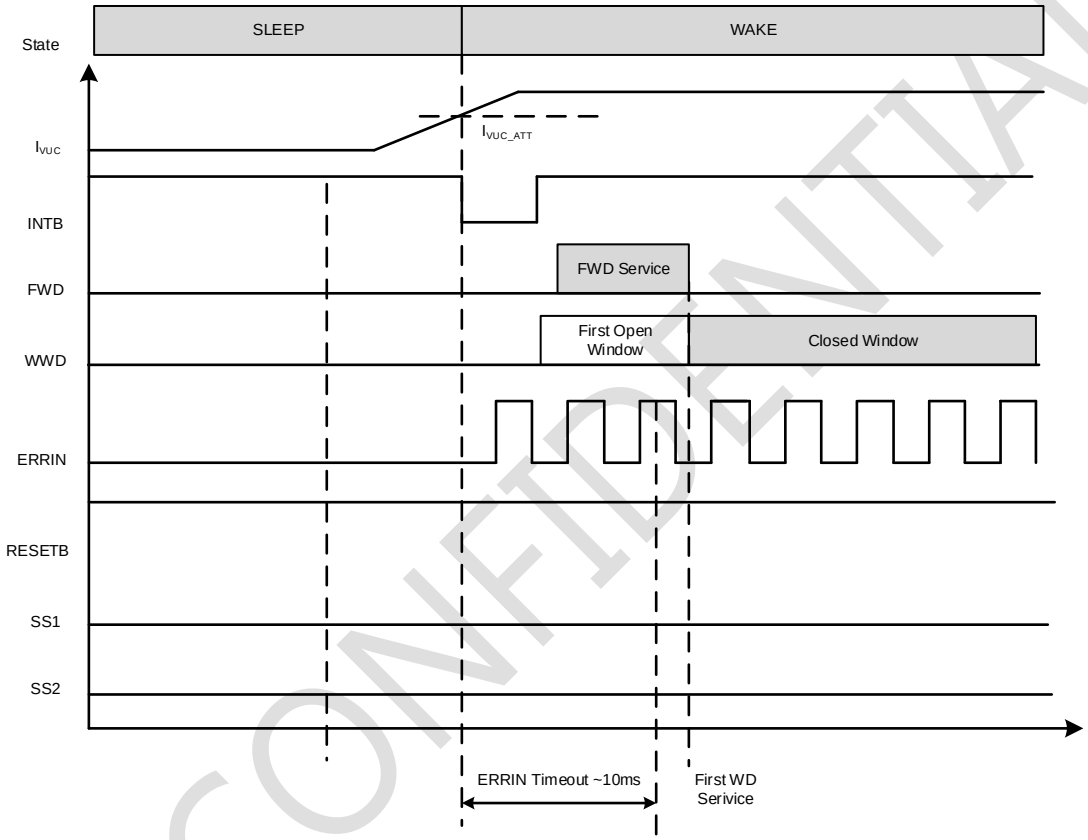


Figure 25. Transition from SLEEP to WAKE state

• The state transition is completed without a transition time and is indicated by an interrupt at pin INTB. The triggering event for the transition from SLEEP can be read from the status register **WKSF**.
• All three monitoring functions (window watchdog, functional watchdog and error monitoring) will recover to the condition active or inactive (switched off) as they were in the NORMAL state previous to the SLEEP state.
• The configuration of the LDOs will recover to the condition active or inactive (switched off) as they were in the NORMAL state previous to the SLEEP state.
• In case the window watchdog was active in the previous NORMAL state, with the negative edge of interrupt signal (at pin INTB) the window watchdog will open the first Open Window, the time of this first Open Window depends on the configured cycle time and is 600 ms (**WDCYC** = 1) or 60 ms (**WDCYC** = 0) (if the window watchdog has not been active in SLEEP state) and requires service. If the window watchdog has been active in SLEEP state continuous service is mandatory.
• In case the functional watchdog was active in the previous NORMAL state, with the negative edge of interrupt signal (at pin INTB) the functional watchdog will start the heartbeat timer and require service. If the functional watchdog has been active in SLEEP state continuous service is mandatory.
• In case the ERRIN pin monitoring was active in the previous NORMAL state, with the negative edge of interrupt signal (at pin INTB) the error monitoring will become active again. Latest 10 ms after the activation a toggling signal

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(with at least three periods past) at pin ERRIN is required. If the error monitoring has been active in SLEEP state continuous toggling is mandatory.
• Reset pin RESETB stays HIGH as the post regulators are active in SLEEP state and in WAKE state.
• The safe signals SS1 and SS2 will stay LOW in SLEEP and in WAKE state.
• If all active monitoring functions (window watchdog, functional watchdog and error monitoring) are serviced properly in WAKE state, you may stay in WAKE state as long as you want.
• If all three monitoring functions (window watchdog, functional watchdog and error monitoring) are inactive (switched off) in WAKE state, you may stay in WAKE state as long as you want.

7.3.5 WAKE → SLEEP State

Prerequisites:
• Selection of LDO_µC current monitor or absolute transition timer.
• Transition delay timer t_{TR_DEL} needs to be configured or default is used.
• Optionally LDO_µC current threshold needs to be defined or default is used.
Triggering Events:
• State transition is only initiated by the SPI command “Go to SLEEP”.
Exceptions:
• If a valid EN (edge) or WAKE (level) signal is detected in the transition state to SLEEP state, the device will move back to the WAKE state and send an interrupt (at pin INTB)
• If the LDO_µC current monitor is activated and the current consumption of the microcontroller is not below the selected LDO_µC current threshold before the transition delay timer t_{TR_DEL} has expired, the device will move back to the WAKE state and send an interrupt (at pin INTB)

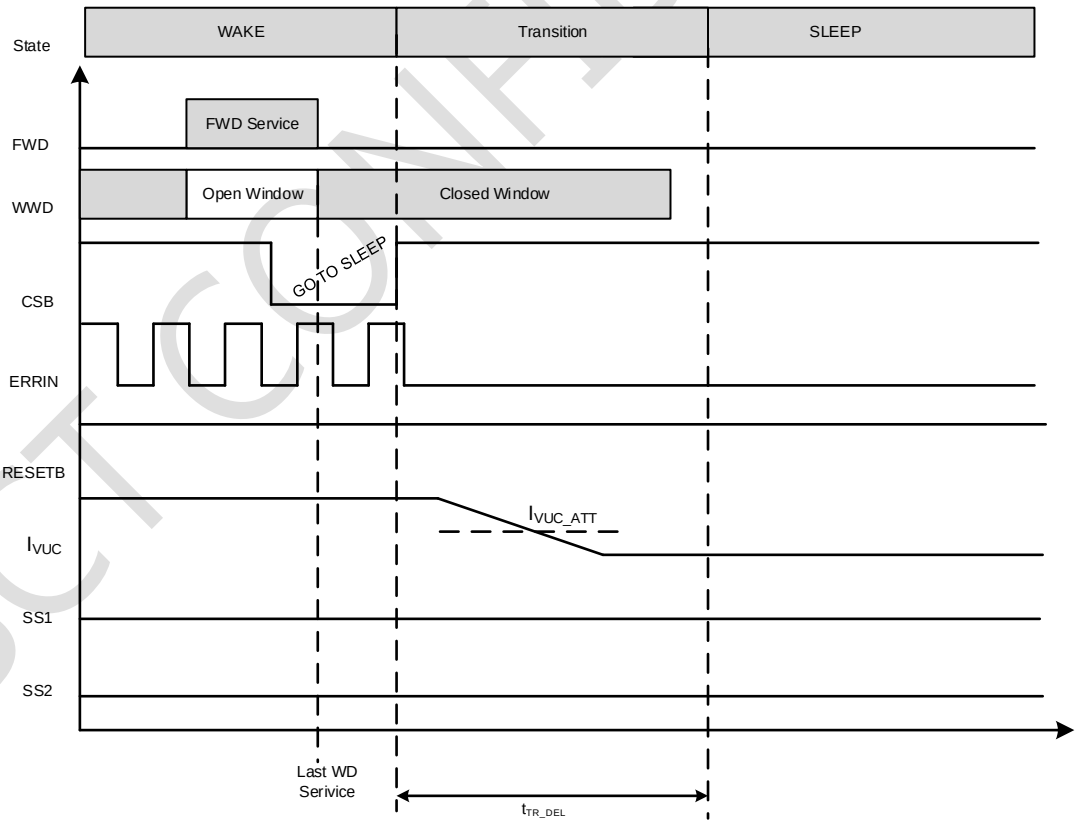


Figure 26. Transition from WAKE to SLEEP state

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• Before the SPI command “Go to SLEEP” is applied, the watchdog(s) - if in use should be serviced, so that the positive edge of CSB signal is well in between the “closed window” of the window watchdog. This is recommended to avoid interference between a missing watchdog trigger and the transition command “Go to SLEEP”
• The positive edge of chip select (pin CSB) after the SPI command “Go to SLEEP” initiates the transition. With chip select high the device leaves WAKE state and enters the transition state (to SLEEP state).
• With chip select (pin CSB) high the error monitoring (pin ERRIN) is stopped - the toggling may end with the positive edge at pin CSB. If the error monitoring should be selected to be active in SLEEP state continuous toggling is mandatory.
• The monitoring of window watchdog and functional watchdog is stopped with the positive edge at pin CSB. If one or both watchdogs should be selected to be active in SLEEP state continuous watchdog service is mandatory.
• Reset pin RESETB stays HIGH as the post regulators are not switched off.
• If the LDO_µC current monitor is enabled the µC current out of pin VO_UC must fall below the LDO_µC monitoring threshold I_{VUC_ATT} within the configured maximum transition delay time t_{TR_DEL}. The time for the transition is depending, how long it takes that the µC current falls below the LDO_µC monitoring threshold I_{VUC_ATT} , if it is below the transition is done.
• Safe state signals SS1 and SS2 stay LOW all the time.

7.3.6 NORMAL → STANDBY State

Prerequisites:
• Selection of LDO_µC current monitor or absolute transition timer.
• Transition timer needs to be configured or default is used.
• Optionally LDO_µC current threshold needs to be defined or default is used.
Triggering Events:
• State transition is only initiated by the SPI command “Go to STANDBY”.
Exceptions:
• If a valid EN (edge) or WAKE (level) signal is detected in the transition state to STANDBY state, the device will move to the INIT state and a reset is generated.
• If the LDO_µC current monitor is activated and the current consumption of the microcontroller is not below the selected LDO_µC current threshold before the transition delay timer t_{TR_DEL} has expired, the device will move to the INIT state and a reset is generated

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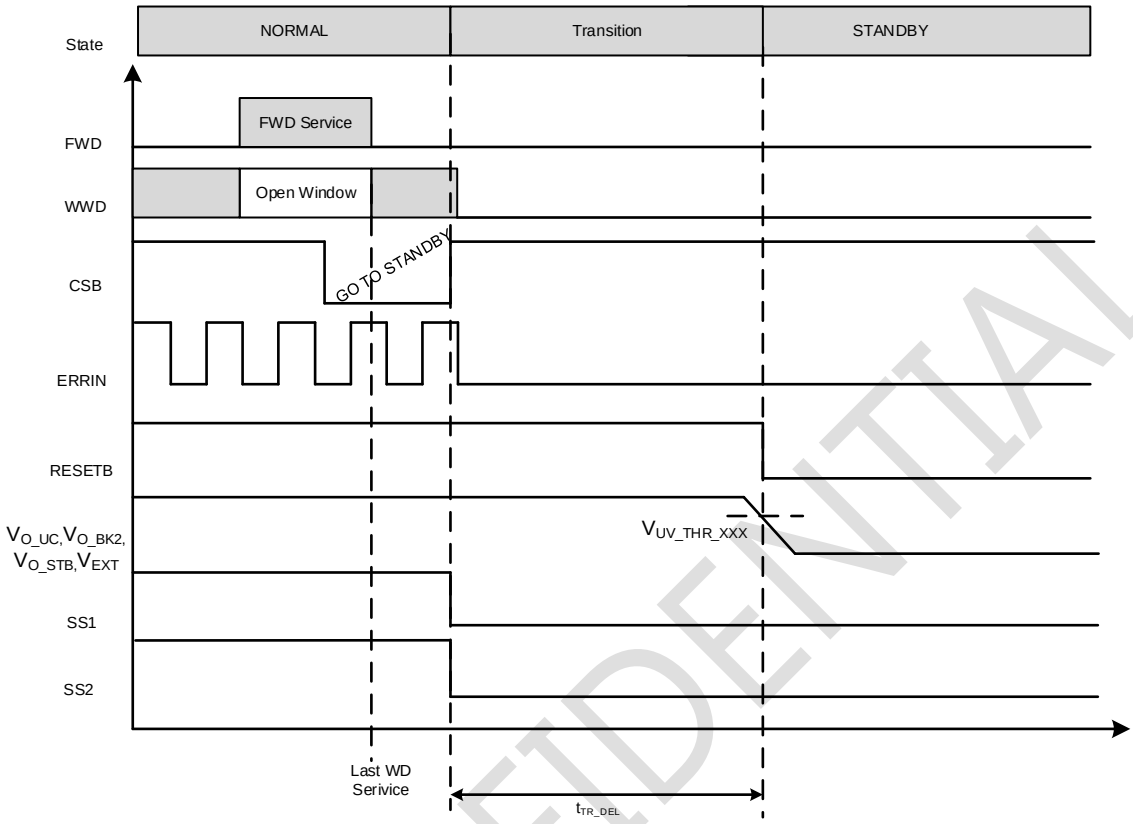


Figure 27. Transition from NORMAL to STANDBY state

• Before the SPI command “Go to STANDBY” is applied, the watchdog(s) - if in use should be serviced, so that the positive edge of CSB signal is well in between the “closed window” of the window watchdog. This is recommended to avoid interference between a missing watchdog trigger and the transition command “Go to STANDBY”
• The positive edge of chip select (pin CSB) after the SPI command “Go to STANDBY” initiates the transition. With chip select high the safe state signals SS1 and SS2 are pulled to zero without delay between SS1 and SS2. The device leaves NORMAL state and enters the transition state (to STANDBY state). (Internal reaction time for the safe state outputs has to be considered)
• With chip select (pin CSB) high the error monitoring (pin ERRIN) is stopped - the toggling may end with the positive edge at pin CSB.
• The monitoring of window watchdog and functional watchdog is stopped with the positive edge at pin CSB.
• With a successful transition from NORMAL to STANDBY state the RESETB is pulled to LOW after the transition time after chip select (pin CSB) going high.
• All pre regulators and all post regulators (with the exception of the standby LDO - it may be ON or OFF in STANDBY state) are switched off at the point when the transition is completed after the RESETB is pulled low.
• In case the absolute transition timer is selected, the device moves from transition state to STANDBY state after the transition delay time t_{TR_DEL}. The transition time t_{TR_DEL} can be determined by SPI command between 100 µs to 1.6 ms, the default setting is 900 µs.
• In case the LDO_µC current monitor is selected for the transition, the device moves from transition state to STANDBY state at the point the current consumption measured at the LDO_µC drops below the selected threshold before the transition delay timer t_{TR_DEL} has expired.

7.3.7 STANDBY → INIT State

Prerequisites:
• none
Triggering Events:

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• Valid EN (edge) or WAKE (level) signal.
• Wake-up timer expired, if enabled

Exceptions:

• none

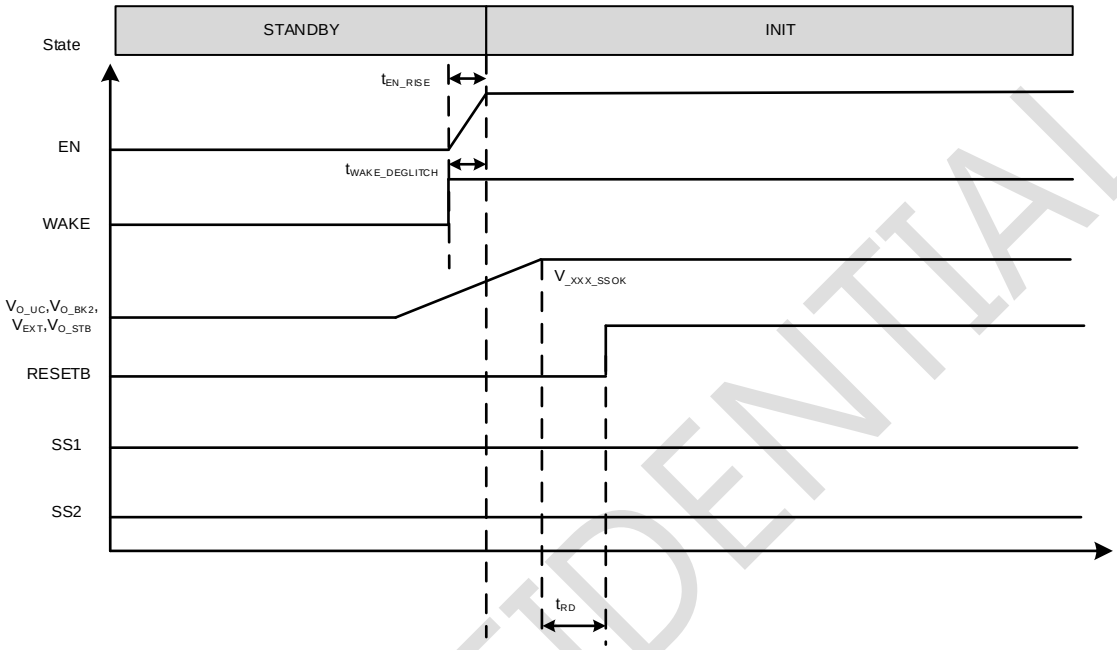


Figure 28. Transition from STANDBY to INIT state

• All pre regulators and all post regulators are switched on according to the power sequencing, except the LDO_STB is kept ON or OFF according to its configuration (simplified in figure above).
• The power on reset delay time is started as soon as the latest of the µC related regulators V_{O_UC}, V_{EXT} or V_{O_STB} (according to the previous configuration) have completed their soft start.
• After the power on reset delay time has expired the RESETB is set to HIGH.
• The safe signals SS1 and SS2 will stay LOW in STANDBY state and in INIT state.

7.3.8 WAKE → NORMAL State

Prerequisites:

• The activated supervision functions (e.g. window watchdog, functional watchdog, ERR pin monitoring) need to be serviced at least once (minimum 3 periods for ERR monitoring) in the active WAKE state, if they are restarted/reinitialized in WAKE state (e.g. watchdog being inactive in previous SLEEP state)

Triggering Events:

• State transition is only initiated by the SPI command “Go to NORMAL”.

Exceptions:

• none

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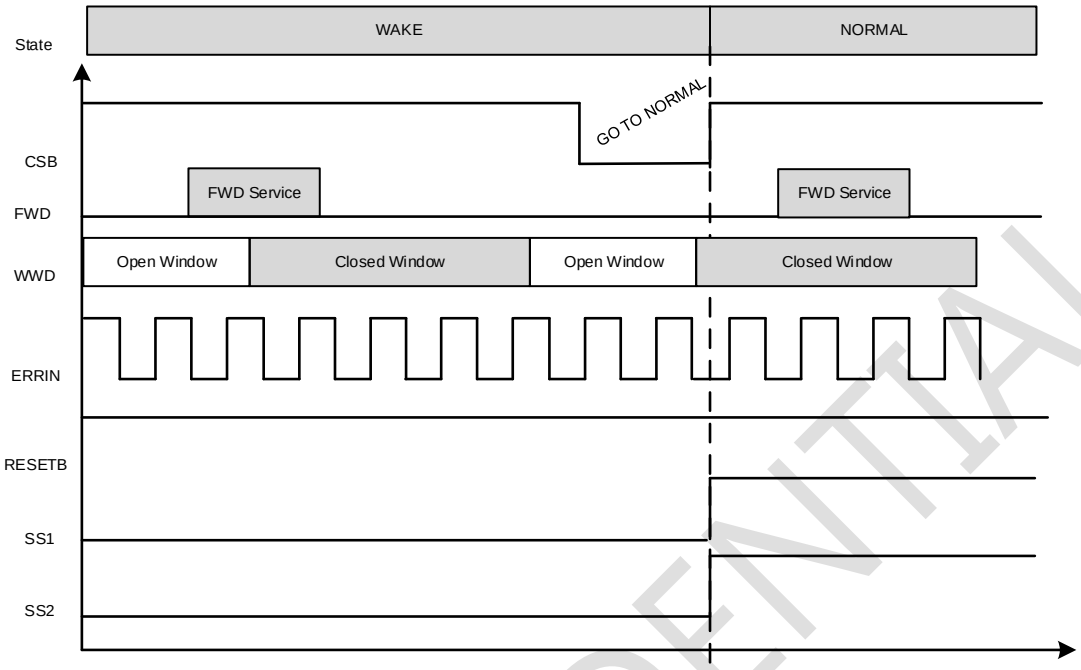


Figure 29. Transition from WAKE to NORMAL state

• The enable signal will be disregarded. A valid enable (edge) signal will not move the device from WAKE to NORMAL state.
• The state of wake signal will be disregarded. A valid wake (level) signal will not move the device from WAKE to NORMAL state.
• The window watchdog (if active in WAKE state) will require continuous service - not synchronized to the transition from WAKE state to NORMAL state.
• The functional watchdog (if active in WAKE state) will require continuous service - not synchronized to the transition from WAKE state to NORMAL state.
• The error monitoring (at pin ERRIN) (if active in WAKE state) will require a continuous toggling signal – not synchronized to the transition from WAKE state to NORMAL state - but minimum 3 periods detected to enter accept the movement into NORMAL state.
• Reset pin RESETB stays HIGH as the post regulators are active in WAKE state and in NORMAL state.
• With the positive edge of chip select high (at pin CSB) the safe state signals SS1 and SS2 are pulled to HIGH at same time. (Internal reaction time for the safe state outputs has to be considered)

7.3.9 WAKE → STANDBY State

Prerequisites:
• Selection of LDO_µC current monitor or absolute transition timer.
• Transition timer needs to be configured or default is used.
• Optionally LDO_µC current threshold needs to be defined or default is used.
Triggering Events:
• State transition is only initiated by the SPI command “Go to STANDBY”.
Exceptions:
• If a valid EN (edge) or WAKE (level) signal is detected in the transition state to STANDBY state, the device will move to the INIT state and a reset is generated.
• If the LDO_µC current monitor is activated and the current consumption of the microcontroller is not below the selected current threshold before the transition timer has expired, the device will move to the INIT state and a reset is generated.

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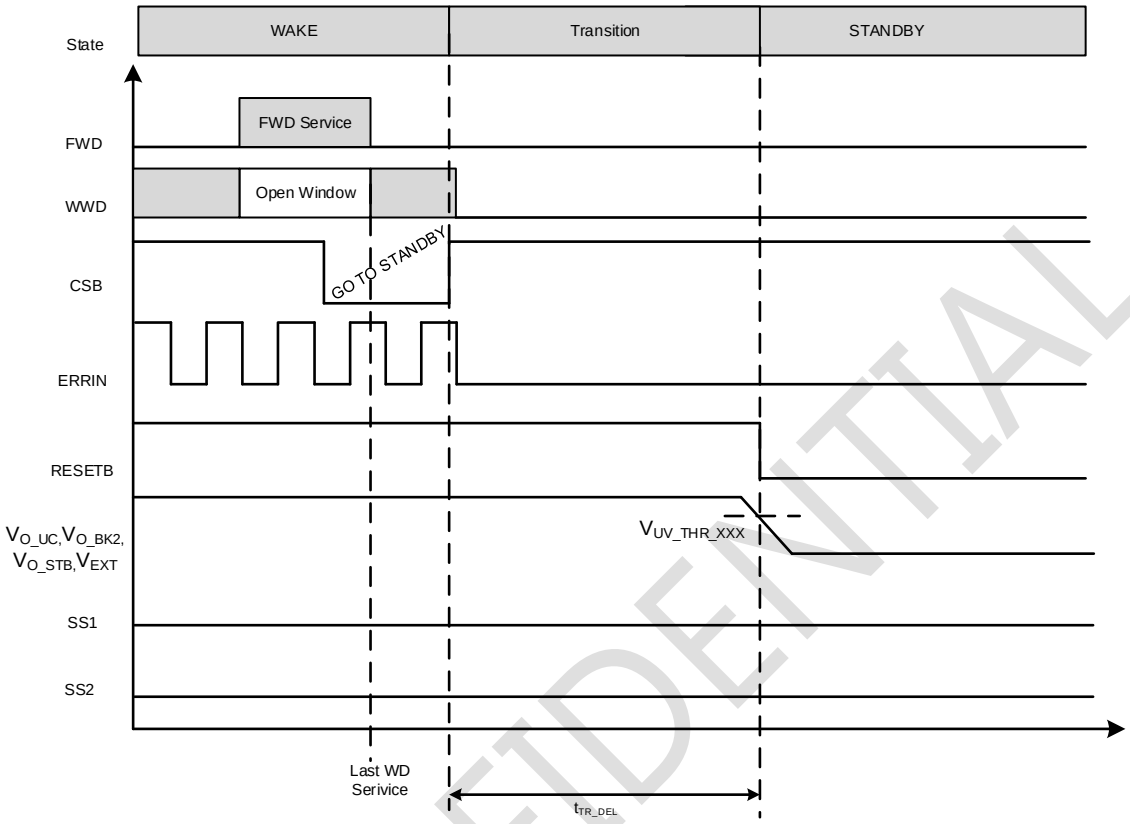


Figure 30. Transition from WAKE to STANDBY state

• Before the SPI command “Go to STANDBY” is applied, the watchdog(s) - if in use should be serviced, so that the positive edge of CSB signal is well in between the “closed window” of the window watchdog. This is recommended to avoid interference between a missing watchdog trigger and the transition command “Go to STANDBY”
• The positive edge of chip select (pin CSB) after the SPI command “Go to STANDBY” initiates the transition. In the WAKE state the safe state signals SS1 and SS2 are LOW and will be kept LOW for the transition to STANDBY. The device leaves WAKE state and enters the transition state (to STANDBY state).
• With chip select (pin CSB) high the error monitoring (pin ERRIN) is stopped - the toggling may end with the positive edge at pin CSB.
• The monitoring of window watchdog and functional watchdog is stopped with the positive edge at pin CSB.
• With a successful transition from WAKE to STANDBY state the reset (RESETB) is pulled to LOW after the transition time after chip select (pin CSB) going high.
• All pre regulators and all post regulators (with the exception of the standby LDO - it may be ON or OFF in STANDBY state) are switched off at the point when the transition is completed after the reset (RESETB) is pulled low.
• In case the absolute transition timer is selected, the device moves from transition state to STANDBY state after the transition time t_{TR_DEL}. The transition time t_{TR_DEL} can be determined by SPI command between 100 µs to 1.6 ms, the default setting is 900 µs.
• In case the LDO_µC current monitor is selected for the transition, the device moves from transition state to STANDBY state at the point the current consumption measured at the LDO_µC drops below the selected threshold before the transition delay timer t_{TR_DEL} has expired.

7.3.10 FAILSAFE → INIT State

Prerequisites:
• FAILSAFE timer has expired.
Triggering Events:

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• Self triggered transition after the prerequisite is fulfilled.
• Valid EN (edge) or WAKE (level) signal (only needed if exception true)

Exceptions:

• In case the FAILSAFE is entered three times in a row with the same failure the self-triggered transition is blocked.

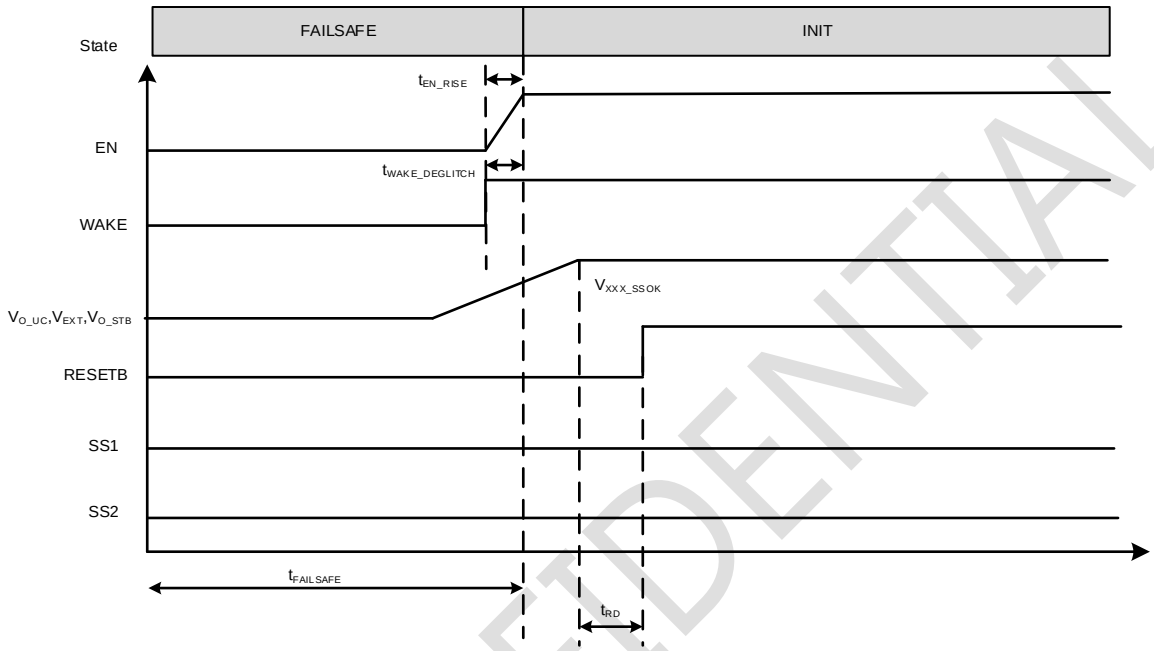


Figure 31. Transition from FAILSAFE to INIT state

• The device transition from FAILSAFE state to INIT state happens earliest after the minimum FAILSAFE time $t_{FAILSAFE}$ which is 20 ms for all failures except a thermal shutdown. In case of a thermal shutdown the minimum FAILSAFE time $t_{FAILSAFE_TSD}$ is 1s. A command to transition before the minimum FAILSAFE time $t_{FAILSAFE}$ has expired, will not be executed.
• After entering INIT state the voltage regulators will ramp up according to the power sequencing.
• The power on reset delay time is started as soon as the latest of the µC related regulators V_{O_UC}, V_{EXT} or V_{O_STB} (according to the previous configuration) have completed their soft start.
• After the power on reset delay time has expired the reset (RESETB) is set to HIGH.
• The device needs to be configured and initiated. All settings done in the configuration registers before the device went into FAILSAFE state are lost, except the configuration of the LDO_STB (**RSYSPCFG0**) and the reset delay time (**DEVCFG1**).
• The safe state signal SS1 and SS2 are LOW in FAILSAFE state and will be LOW in INIT state

7.4 Reaction on detected faults

Errors are classified according to their severity into 4 different error classes:
• Stay in Current State - Failures affecting peripherals without direct risk for the microcontroller, that are indicated by an interrupt to allow analysis by the microcontroller without changing the state.
• Move to INIT - Medium severity errors that brings the device back to INIT state and generate a reset for the microcontroller.
• Move to FAILSAFE - Critical error with high risk of damaging the microcontroller.
• Move to POWERDOWN - Most critical error with high risk of damaging ourself plus the microcontroller
The error classes are overruled according to their severity, e.g. movement to POWERDOWN takes precedence over movement to FAILSAFE which takes precedence over movement to INIT.
The move to INIT, FAILSAFE and POWERDOWN errors are named “error triggered state transitions” in this

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document.

7.4.1 INTERRUPT Events

The following failures will not trigger a movement of the device to another state by themselves, but will indicate the failure by an interrupt event:

• Detection of under voltage or a short to ground or overload detection at voltage reference

• Detection of over voltage, under voltage or a short to ground at trackers 1 or 2

• Detection of over voltage, under voltage, a short to ground or thermal shutdown at LDO_COM

• Detection of under voltage at pre regulator.

• Detection of overload at standby regulator

• Increase of window/functional watchdog status counter, but actual value still stays below the threshold

• Error monitoring recovery delay time is active and ERR signal stops toggling.

• Thermal shutdown pre warning (Step down pre regulator or/and LDO_μC or/and LDO_COM)

• Bandgap monitoring: If the deviation between both bandgaps is larger than 4%

The interrupt may not be visible on the INTB pin in STANDBY and FAILSAFE state due to microcontroller supplies being switched off. The event is stored in the status flags (IF, SYSSF, MONSF0, MONSF1, MONSF2, OTWRNSF, OTFAIL).

7.4.2 INIT Events

The following failures will bring the device from any state to INIT state:
• Detection of under voltage at LDO_UC, VEXT. or LDO_STB
• Detection of window/functional watchdog status counter overflow
• Stop of error signal detected (immediate reaction mode) or stop or error signal detected for more than recovery delay time (recovery mode)
• One or two consecutive expires of the INIT timer (configuration in INIT state failed)

- **Transition into INIT State due to INIT timer expired for the first time**

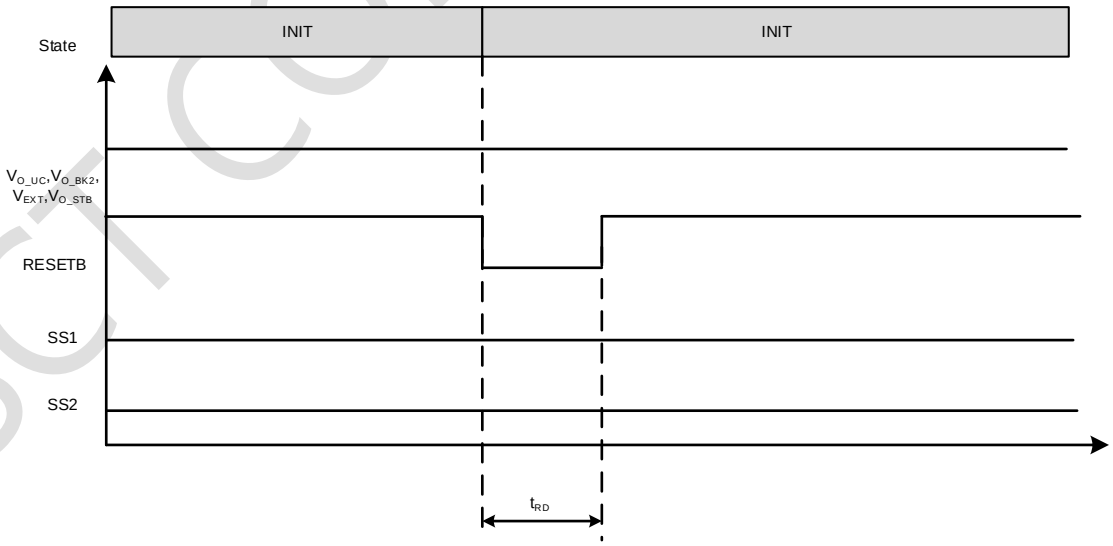


Figure 32. Transition from INIT to INIT state - first movement

Description:
• The device transition from INIT to INIT state (or stays in INIT state) for the first time is issuing a “soft reset”. Pin

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RESETB is pulled to LOW for the reset delay time t_{RD} in case all µC related voltages are in valid range. The power sequence is started after entering the INIT state: the disabled outputs are re-activated, the other ones are kept enabled, except the LDO_STB will keep its configuration being ON or OFF.

- **Transition into INIT State due to INIT timer expired for the second time**

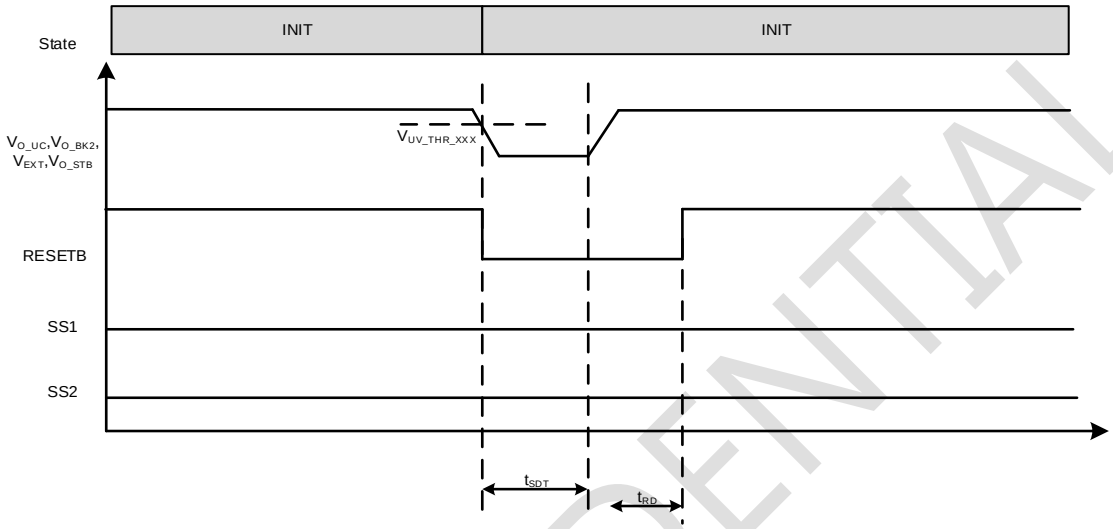


Figure 33. Transition from INIT to INIT state - second movement

Description:

• The device transition from INIT to INIT state (or stays in INIT state) for the second time is issuing a “hard reset” - pin RESETB is pulled to LOW and all outputs are disabled for the time *t* and restarted according to the power sequencing, except the LDO_STB will restore its configuration being ON or OFF.

• The RESETB pin will be released according to the power sequencing using the reset delay time t_{RD}.

Note:Please refer also to the transition INIT to FAILSAFE

- **Transition into INIT State due to other INIT events**

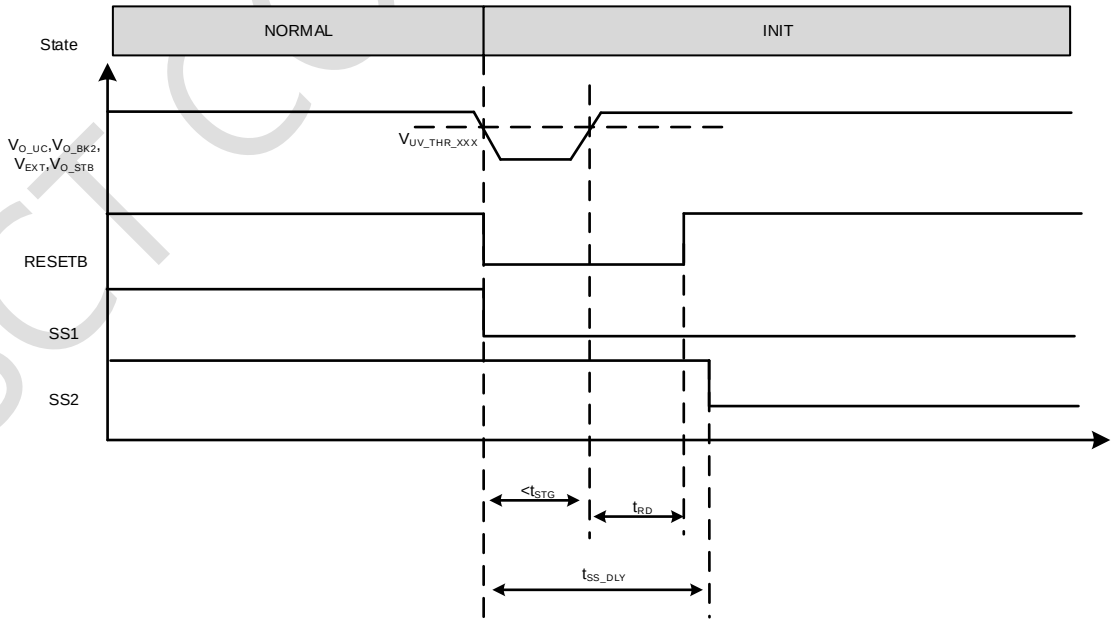


Figure 34. Transition from NORMAL to INIT state

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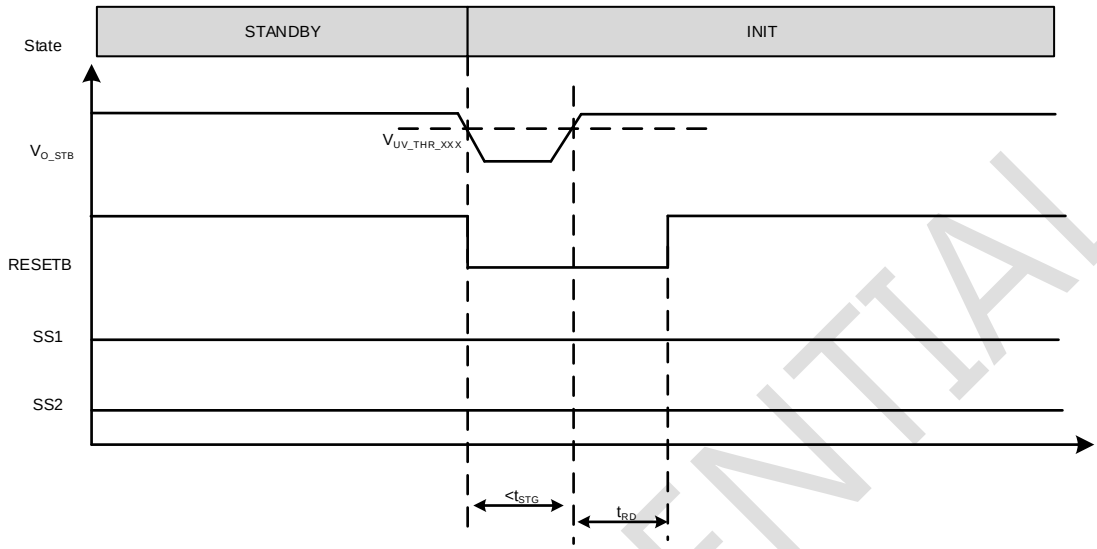


Figure 35. Transition from STANDBY to INIT state

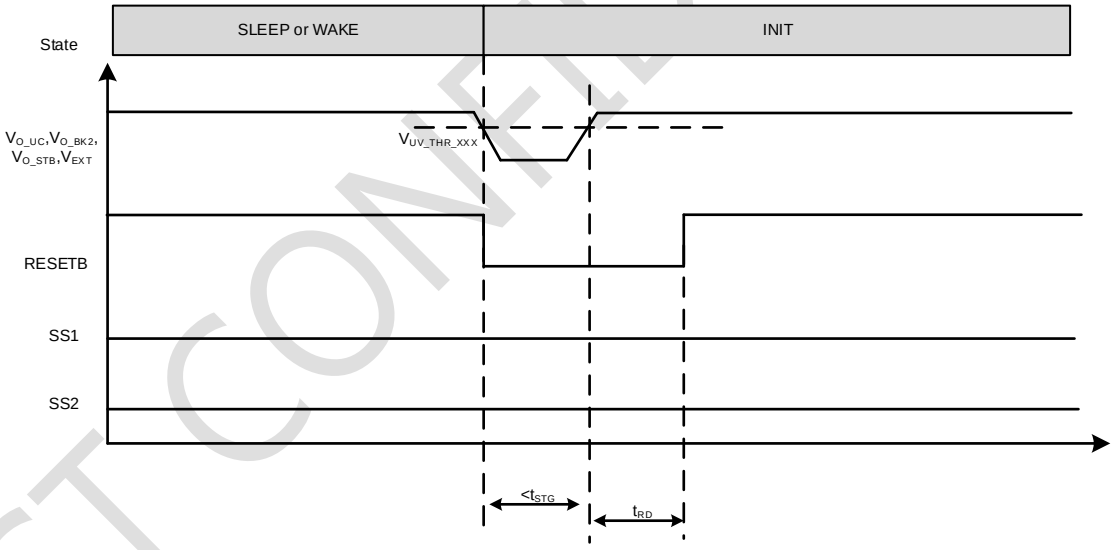


Figure 36. Transition from SLEEP or WAKE to INIT state

Description:

• The device transitions from NORMAL/SLEEP/INIT/WAKE into INIT state might be issued by an undervoltage of the µC related voltages VO_UC, VO_BK2, VO_STB or VEXT as shown in the figure. The pin RESETB is pulled to LOW and all the outputs are enabled, except the LDO_STB will keep its configuration being ON or OFF. Disabled outputs will get switched on again. The under voltage is shorter than the short to ground detection time t_{STG}. The reset delay time t_{RD} is started as soon as all µC related voltages VO_UC, VO_BK2, VO_STB or VEXT are back in the valid range. The RESETB pin is released accordingly. An under voltage longer than the short to ground detection time t_{STG} would first lead to a transition from NORMAL/SLEEP/INIT/WAKE to INIT state and then, after the short to ground detection time t_{STG} has expired, to a transition from INIT to FAILSAFE state.

• The device transitions from STANDBY into INIT state might be issued by an undervoltage of the VO_STB as shown in the figure. The pin RESETB is pulled to LOW and all the outputs are enabled, except the LDO_STB will keep its configuration being ON or OFF. Disabled outputs will get switched on again. The under voltage is shorter

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than the short to ground detection time t_{STG}. The reset delay time t_{RD} is started as soon as all µC related voltages VO_UC, VO_BK2, VO_STB or VEXT are back in the valid range. The RESETB pin is released accordingly. An under voltage longer than the short to ground detection time t_{STG} would first lead to a transition from STANDBY to INIT state and then, after the short to ground detection time t_{STG} has expired, to a transition from INIT to FAILSAFE state.

• The “soft reset” can also be initiated by a window watchdog error counter overflow (> ∑WWD), a functional watchdog error counter overflow (> ∑FWO), an error indication (immediate or recovery delay time mode), if these monitoring functions are in use. In this case the reset delay time t_{RD} will be started falling edge of the RESETB pin. Please consider the state transition time to INIT state.

• If the previous state is NORMAL state, SS1 will be pulled to LOW immediately with pin RESETB, SS2 will be pulled to LOW after the selected t_{SS_DLY}.

• Please mind that in case of an UV event on VO_UC, a delayed SS2 signal will follow VO_UC as it is supplied from LDO_UC.

Note: In case the device is sent back to NORMAL state before the configured t_{SS_DLY} has expired the SS2 will be kept HIGH without being set to LOW.

7.4.3 FAILSAFE Events

The following failures will bring the device from any state to FAILSAFE state:

• Detection of over voltage, a short to ground or thermal shutdown at LDO_UC
• Detection of over voltage or a short to ground at Core_Sup adj. or LDO_STB
• Detection of over voltage at VO_VREF
• Detection of over voltage, short to ground1) (only during startup phase in INIT state) or thermal shutdown at pre regulator
• Three consecutive initialization failures(e.g. configuration in INIT state failed)
• A BIAS current monitor failure
• A over temperature shutdown due to exceeded temperature in the monitoring block.
• A fuse selection monitor failure
• An over voltage at the supply pins (VSUP) will trigger the overvoltage protection and move the device into FAILSAFE-state (except for STANDBY state)

- **Transition into FAILSAFE State due to STG**

Description:

• The detection of an under voltage of the µC related voltages VO_UC, VO_BK2,VO_STB or VEXT as shown in the figure will initiate the transition from NORMAL/SLEEP/INIT/WAKE into INIT state. (please refer to previous chapter Transition into INIT state)

• Pin RESETB will be pulled to LOW as soon as the under voltage is detected (at one or more of the regulators mentioned above - whichever is the first)

• The safe state signal SS1 will be pulled to LOW together with pin RESETB going to low

• If the short to ground maintains for longer than the short to ground detection time t_{STG} a short to ground event is detected.

• All regulators will be switched off as soon as the short to GND is detected, regardless if they are in under voltage condition or not.

• The device moves from INIT state to FAILSAFE state

• The safe state signal SS2 will be pulled to LOW together with the transition from INIT to FAILSAFE state, even if the delay time t_{SS_DLY} has not expired yet, because LDO_µC is switched off (LDO_µC is switched on in INIT state, but switched off in FAILSAFE state).

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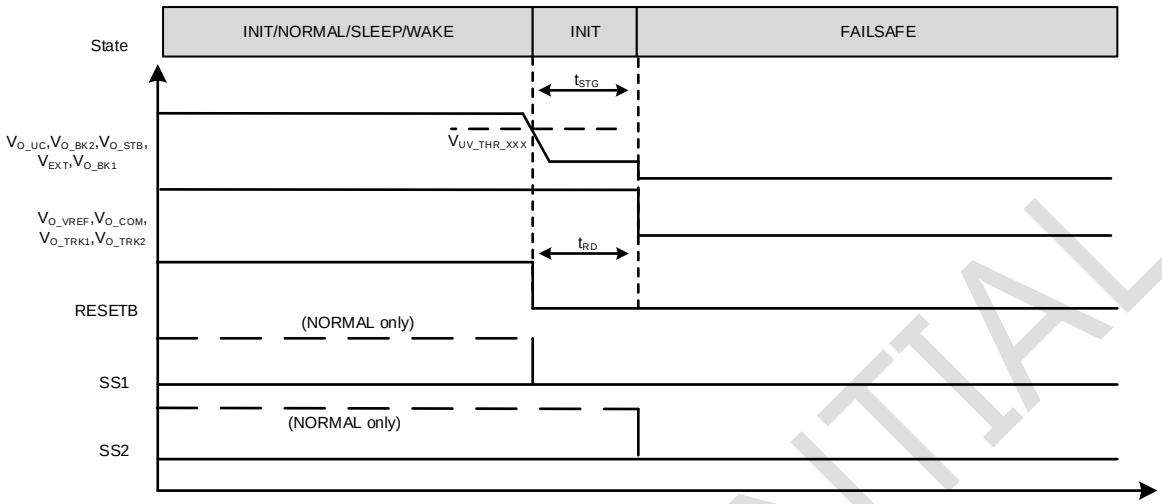


Figure 37. Transition into FAILSAFE state due to STG fault

• The device transitions from STANDBY into INIT state might be issued by an undervoltage of the VO_STB. The pin RESETB is pulled to LOW and all the outputs are enabled, except the LDO_STB will keep its configuration being ON or OFF. Disabled outputs will get switched on again. An under voltage longer than the short to ground detection time t_{STG} would lead to a transition from INIT to FAILSAFE state and all regulators will be switched off.

- **Transition into FAILSAFE State due to OV**

Description:

• The detection of an over voltage of the preregulator voltage VO_BK1 or the µC related voltages VO_UC, VO_BK2, VO_STB, VEXT or VO_VREF as shown in the figure will initiate the transition from INIT / NORMAL / SLEEP / WAKE / STANDBY state to FAILSAFE state.

• Pin RESETB will be pulled to LOW as soon as the over voltage event is detected (at one or more of the regulators mentioned above - whichever is the first).

• All regulators will be switched off, when the device turns from current state into FAILSAFE state, regardless if they are in over voltage condition or not.

• Out of NORMAL state the safe state signals SS1 and SS2 will be pulled to LOW immediately with pin RESETB going to low, because the LDO_µC is switched off. Out of any other state the safe state signals SS1 and SS2 are LOW and will stay low.

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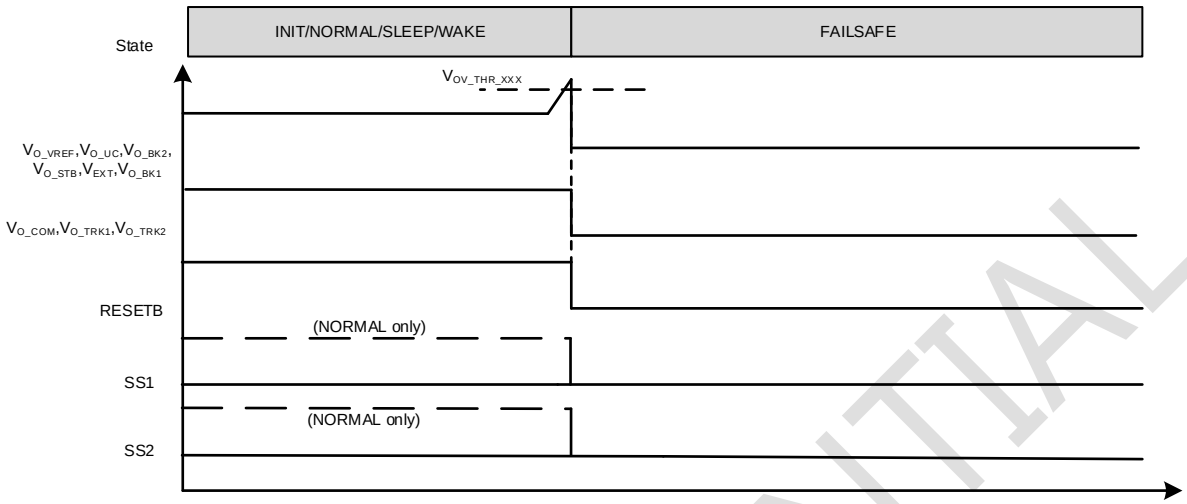


Figure 38. Transition into FAILSAFE state due to OV fault

- **Transition into FAILSAFE State due to Thermal Shutdown**

Description:

• The transition from any state into FAILSAFE state will be initiated by a thermal shutdown (TSD).
• Pin RESETB will be pulled to LOW as soon as the thermal shutdown will be detected.
• All regulators will be switched off, when the device turns from current state into FAILSAFE state. regardless if they are in over temperature condition or not
• Out of NORMAL state the safe state signals SS1 and SS2 will be pulled to LOW immediately with pin RESETB going to low, because the LDO_µC is switched off. Out of any other state the safe state signals SS1 and SS2 are LOW and will stay low.
• The device will stay in FAILSAFE state after a thermal shutdown (TSD) at least for 1 s.

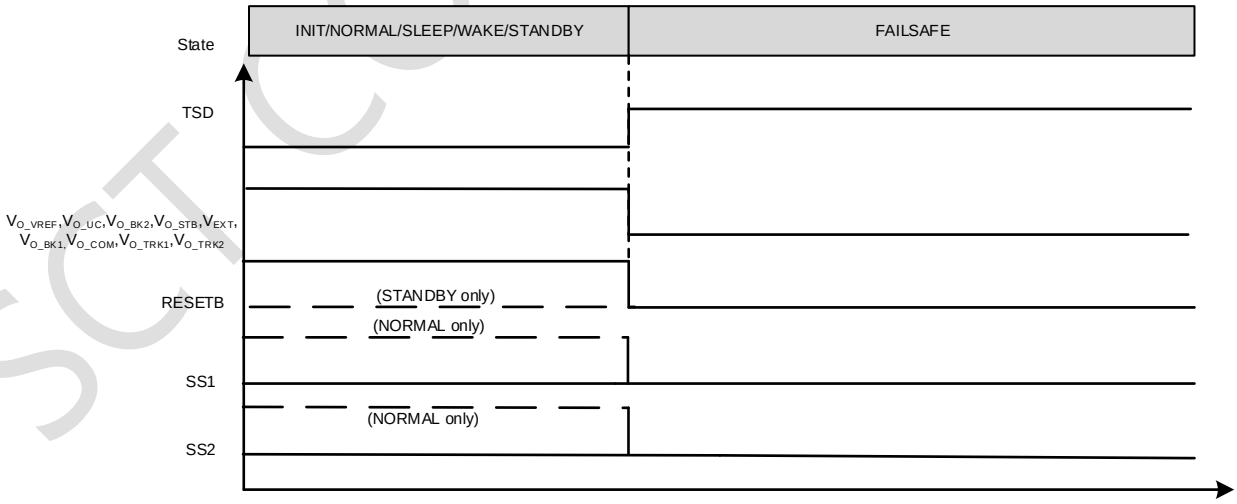


Figure 39. Transition into FAILSAFE state due to TSD fault

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7.4.3 POWEROFF Events

The following failures/event will bring the device always with highest priority to POWERDOWN state:
• V_{SUP} below V_{SUP_UVLO}-$V_{SUP_UVLO_HYS}$ when decreasing
• Detection of over- or under voltage on internal supplies

7.5 Built In Self Test (BIST) Features

SCT61490S provides the option to test certain observation functions with the assistance of the external µC via built in self-test features. These features are described in the following chapters.

7.5.1 Analog Built In Self Test (ABIST)

The device will run the ABIST automaticallywhen exiting from POWERDOWN state, which performs tests on each comparator generating artificial undervoltage and overvoltage (or current) conditions. If any comparator is failed to detect the artificial fault, the device moves from ABIST state to FAILSAFE state. The ABIST result will be indicated by **ABIST_CTRL0**.**STATUS.**

7.5.2.1 Online Analog Built In Self Test (ABIST)

SCT61490S provides the option to test the comparator and evaluation logic related to the monitoring functions contributing to the activation of the secondary safety shutdown path and the generation of an interrupt. Further on additional comparators and evaluation logic related to the safe state control itself can be tested (SSC overvoltage watchdog and toggling monitor). This is accomplished via an internal ABIST controller which performs tests on each comparator generating artificial undervoltage and overvoltage (or current) conditions, is checking the result and generates the information which needs to be evaluated by the µC to judge, if the ABIST operation has been performed successfully or not.
The following status information on ABIST operation is generated by the system:
• In case an ABIST operation has been requested by the µC, a status is provided after the ABIST has been performed (**ABIST_CTRL0**.**STATUS**). This status needs to be evaluated by the µC. The provided status is just a GO-NOGO information, which means information about a particularly tested path is provided. The basic comparator function is tested, but not the respective threshold values.
The test of the monitoring and safety relevant output functions is run on three different areas in the system:
• The functionality of a comparator and its corresponding deglitching logic can be tested by a “comparator only” test. This test is performed by generating the failure condition for a time shorter than the deglitching time, accordingly the secondary safety shutdown path nor the interrupt is triggered due to the detected failure. During this test only the selected comparator(s) are tested. In case more than one comparator is selected, the test is performed with a fixed sequence of comparators to be tested. The completion of the test is indicated by an interrupt.
• The functionality of a comparator including its corresponding deglitching logic and the contribution to the respective safety measure can be tested. The safety measure is either the activation of the secondary safety shutdown path or the generation of an interrupt. This test is performed in a time longer than the deglitching time.
• While the device provides information about the status for the first and the second ABIST, further microcontroller cooperation is required for the third area. The µC is responsible to check if the secondary safety shutdown path has been activated successfully (SS1/SS2 are set low) or an interrupt event has been detected by the µC.

7.5.2.2 How to run the ABIST

During ABIST, servicing of the watchdog(s) and error monitoring is required to be performed according to the configuration by the microcontroller. Error in not doing so will lead to failure events in these functions and will lead to the assertion of interrupt, reset or safe state output events accordingly, which is disturbing the proper analysis of the ABIST results. Optionally watchdog functionality and/or error monitoring can be disabled during ABIST operation via a protected register access. In this case, no servicing is required.
During a performed ABIST including the deglitching logic the FLAG registers (**SYSFAIL**, **INITERR**, **IF**) as well as the status information (**MONSF1**, **MONSF2**, **MONSF3**) are triggered and updated by out of range conditions caused by the ABIST functionality, which has to be considered beside the results provided in the ABIST related registers (**ABIST_CTRL0** to **ABIST_SELECT2**).
During the time, when the ABIST is performed by internal hardware, the assertion of RESETB due to the occurrence of any event which is supposed to trigger the respective action and is part of the logic which is affected by the ABIST control is blocked. In addition, the state machine will not change its state according to the reaction on detected

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faults. In case an ABIST contributing to the secondary safety shutdown path is started and the device is in NORMAL state, the state machine will move from NORMAL to WAKE state.
Furthermore, all voltages will be kept enabled regardless of any out of range detection caused by ABIST itself. The test of a single functionality is basically always performed in the same way:
• All comparators are assumed to be enabled in case they are selected to be tested, while this is true for any µC related voltage it might not be the case for non µC related voltages. Accordingly, configurable LDO's have to be enabled before they can be tested. On the other hand the ABIST test on a comparator which is not used by the system is not required to be performed.
• The comparators to be tested shall be selected by setting the individual bit(s) in the respective register(s) (**ABIST_SELECT0**, **ABIST_SELECT1** and **ABIST_SELECT2**). For this selection it is necessary to differentiate by the contribution to the different safety measure.
• The microcontroller shall configure the register **ABIST_CTRL0** according to the functionality to be tested. The configuration consist of the tested safety measure (**ABIST_CTRL0**.**INT**), the tested area/coverage by the ABIST (**ABIST_CTRL0**.**PATH**) and the configuration whether a sequence or a single comparator shall be tested (**ABIST_CTRL0**.**SINGLE**).
• The microcontroller shall set the global ABIST start bit (**ABIST_CTRL0**.**START**) to start the ABIST.
• The global ABIST start bit shall be read by the µC. If this bit is still set, ongoing ABIST functionality is performed. Upon completion of the selected ABIST operation(s) the start bit is cleared and an interrupt event is generated.
• Each bit which has been set to select the test of a dedicated comparator (**ABIST_SELECT0**, **ABIST_SELECT1** and **ABIST_SELECT2**) is cleared once a successful ABIST operation has been performed on the particular comparator. Each bit which has been set to select the test of a dedicated comparator is kept unchanged if the ABIST operation on this particular comparator has not been performed successfully. In this way the µC can determine which comparator failed in case the ABIST status information shows a failing ABIST operation.

7.5.2.3 Testing the comparator logic only

During the ABIST operation the comparators are triggered by the ABIST controller for a time shorter than the internal deglitching time t_{RR} (reset reaction time). A properly working comparator signals an out of range condition to its output for the time the failure condition is applied.
The provided information of each comparator is checked against the expected value. If the comparator output value matches the expected value this is considered as a passing test by the ABIST controller. If any of the provided output values do not match the expected value, this is considered as a failing test. The general result of the ABIST is provided by the **STATUS** in the register **ABIST_CTRL0**. The detailed result for each selected comparator can be checked by the registers **ABIST_SELECT0**, **ABIST_SELECT1** and **ABIST_SELECT2**. In case the previously selected bits are reset after the test is finished, it can be considered as pass. A bit which is still set, would indicated the failing comparator(s), that makes the overall **STATUS** to be failed.
Accordingly the maximum selection(1) (including possible ones) for the comparator test would be the following:
Secondary safety shutdown path (SS1/2) related:
• **ABIST_SELECT0** : 00101111b (2Fh)
• **ABIST_SELECT1** : 00001110b (0Eh)
• **ABIST_SELECT2** : 11001001b (C9h)
• Start of the test by **ABIST_CTRL0** : 00000001b (01h)
Interrupt (INTB) related:
• **ABIST_SELECT0** : 11010000b (D0h)
• **ABIST_SELECT1** : 11110001b (F1h)
• **ABIST_SELECT2** : 00110000b (30h)
• Start of the test by **ABIST_CTRL0** : 00001001b (09h)
This type of ABIST can be performed in the following states of the **State Machine**: INIT, NORMAL, WAKE. In case of an successful ABIST there shall be no reaction of secondary safety shutdown path SS1/2 and only an interrupt generated due to the finished ABIST (**IF**.**ABIST** set and **IF**.**MON** not set, considering cleared interrupt flags prior to the ABIST and no real failure events during the ABIST).
1) Please mind that for a test of a comparators the corresponding output has to be enabled.

7.5.2.4 Testing the comparator logic and the corresponding deglitching logic

During the ABIST operation the comparators are triggered by the the ABIST controller for a time longer than the internal deglitching time t_{RR} (reset reaction time). A properly working comparator signals an out of range condition

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to its output for the time the failure condition is applied. The deglitching logic will forward the failure trigger after *t*rr and makes the device react on the recognized failure event. This reaction consists the storage of the respective monitoring failure flags and as well the triggering of the respective output function, which is either the interrupt INTB or the secondary safety shutdown path SS1/2. The reaction of the safe state outputs SS1/2 can only be observed in case the test is started in NORMAL state.
Furthermore the provided information of each deglitching logic output is checked against the expected value. If the deglitching logic output value matches the expected value this is considered as a passing test by the ABIST controller. If any of the provided output values do not match the expected value, this is considered as a failing test.
The general result of the ABIST is provided by the **STATUS** in the register **ABIST_CTRL0**. The detailed result for each selected comparator can be checked by the registers **ABIST_SELECT0**, **ABIST_SELECT1** and **ABIST_SELECT2**. In case the previously selected bits are reset after the test is finished, it can be considered as pass recognized by the ABIST controller. A bit which is still set, would indicated the failing comparator(s), that makes the overall **STATUS** to be failed.
Beside the results read from the ABIST controller related registers, the result provided in the failure/interrupt flags (**SYSFAIL**, **INITERR** and **IF**) and monitoring status flags (**MONSF1**, **MONSF2** or **MONSF3**) have to be read and checked by the microcontroller against the expected result considering the configuration set before the start of the ABIST. **INTOV** located in register **ABIST_SELECT2** cannot be tested in this way, testing of the comparator logic only is required.
The maximum selection(1) for the comparator and deglitching logic test would be the following:
Secondary safety shutdown path (SS1/2) related:
• **ABIST_SELECT0** : 00101111b (2Fh)
• **ABIST_SELECT1** : 00001110b (0Eh)
• **ABIST_SELECT2** : 11000001b (C1h)
• Start of the test by **ABIST_CTRL0** : 00000011b (03h)
Interrupt (INTB) related:
• **ABIST_SELECT0** : 11010000b (D0h)
• **ABIST_SELECT1** : 11110001b (F1h)
• **ABIST_SELECT2** : 00110000b (30h)
• Start of the test by **ABIST_CTRL0** : 00001011b (0Bh)
The analysis based on the maximum possible selection would consist the following:
Secondary safety shutdown path (SS1/2) related:
• **IF** : 01000000B (40h)
• **INITERR** : 00000100b (04h)
• **SYSFAIL** : 00000100b (04h)
• **MONSF1** : 00101111b (2Fh)
• **MONSF2** : 00001110b (0Eh)
• **MONSF3** : 11000001b (C1h)
• Start of the test by **ABIST_CTRL0** : 00000011b (03h)
Interrupt (INTB) related:
• **IF** : 01001000b (48h)
• **INITERR** : 00000000b (00h)
• **SYSFAIL** : 00000000b (00h)
• **MONSF1** : 11010000b (D0h)
• **MONSF2** : 11110001b (F1h)
• **MONSF3** : 00110000b (30h)
• Start of the test by **ABIST_CTRL0** : 00001011b (0Bh)
This type of ABIST can be performed in the following states of the **State Machine**: INIT, WAKE, NORMAL. If this test is run in NORMAL state on comparators contributing to the secondary safety shutdown path the device will switch low the safe state outputs SS1/2 and the **State Machine** will move to WAKE state, without triggering a reset. It has to be considered that testing the complete monitoring chain till the respective output (SS1/2 or INTB) in this way will cover only the first comparator in the sequence, as this one will trigger the output reaction.
If this test is run in INIT or WAKE state, contribution to activation of the secondary safety shutdown path cannot be tested. The system is in a safe state already and the secondary safety shutdown path is already activated. In any way the proper behavior of the secondary shutdown path as well as the interrupt signal needs to be checked by the microcontroller.

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7.5.2.5 Testing the complete monitoring chain (comparators, deglitching and output)

The testing of the complete monitoring chain from the comparator till the respective output function has to be divided into the two functions available in SCT61490S. First the secondary safety shutdown path called SS1/2 for severe microcontroller related failure events and secondly the interrupt function INTB for peripheral related failure events in terms of voltage and current monitoring.

• **Testing the activation of the secondary safety shutdown path:**

To test the activation of the secondary safety shutdown path, the device has to be brought into NORMAL state. The µC shall check if the secondary safety shutdown path has been de-activated successfully (SS1/2 high).

Once in NORMAL state a single comparator contributing to the secondary safety shutdown path shall be selected. A single bit ('x') has to be set for a corresponding comparator in registers **ABIST_SELECT0** (00x0xxxxb), **ABIST_SELECT1** (0000xxx0b) or **ABIST_SELECT2** (xx00000xb). A randomized selection by the microcontroller ensures maximum coverage of the contributions to the secondary safety shutdown path. Then a single comparator ABIST operation on the full path of the secondary safety shutdown path needs to be started (register **ABIST_CTRL0**: 00000111b (07h)). Upon completion of the requested ABIST operation the device will autonomously move into WAKE state and an interrupt event is generated. The interrupt event will indicate the completion of the ABIST (**IF**.**ABIST**). Furthermore the respective monitoring failure flag for the selected comparator will be set (either **INITERR**.**VMONF** for "**Move to INIT State**" failures or **SYSFAIL**.**VMONF** for "**Move to FAILSAFE State**" failures) which has to be checked and cleared by the microcontroller.

The secondary safety shutdown path shall be activated (SS1/2 low), it is the responsibility of the µC to check the activation of the secondary safety shutdown path. If SS2 delay is enabled, this delay will be applied when the ABIST operation is performed, i.e. the activation of the shutdown path connected to SS2 will be delayed according to the programmed value for failure cases not leading to FAILSAFE.

The µC needs to read and check the status of the requested ABIST operation (**ABIST_CTRL0**.**STATUS**), the respective monitoring status flag (**MONSF1**, **MONSF2** or **MONSF3**) to be set according to the previous selection and **ABIST_SELECT0**, **ABIST_SELECT1** and **ABIST_SELECT2** bits to be cleared.

Furthermore, the microcontroller has to proceed with the following steps to check the safe state control and the safe state outputs:

• Check that the secondary safety shutdown path has been activated successfully (SS1/2 low)
• Enable overvoltage trigger of the safe state control (set **ABIST_CTRL1**.**OV_TRIG**)
• Wait for 50µs and check that the secondary safety shutdown path is still activated successfully (SS1/2 low)
• Select generation of valid toggling signal for the safe state control (set **ABIST_CTRL1**.**ABIST_CLK_EN**)
• Wait for 50µs and check that the secondary safety shutdown path is still activated successfully (SS1/2 low)
• De-select generation of toggling signal for the safe state control (reset **ABIST_CTRL1**.**ABIST_CLK_EN**)
• Wait for 50µs and check that the secondary safety shutdown path is still activated successfully (SS1/2 low)
• Disable overvoltage trigger of the safe state control (set **ABIST_CTRL1**.**OV_TRIG**)
• Wait for 50µs and check that the secondary safety shutdown path is still activated successfully (SS1/2 low)

Afterwards a test of all comparators which contribute to the activation of the secondary safety shutdown path shall be configured and started.

• **Testing the generation of an interrupt event:**

The test of the generation of an interrupt event can be done in the states INIT, NORMAL and WAKE state. Even though it is recommended to have the application in safe state (INIT or WAKE state).

For this test first a single comparator contributing to the interrupt function shall be selected. A single bit ('x') has to be set for a corresponding comparator in registers **ABIST_SELECT0** (xx0x0000b), **ABIST_SELECT1** (xxxx000xb) or **ABIST_SELECT2** (00xx0000b). A randomized selection by the microcontroller ensures maximum coverage of the contributions to the interrupt function. Then a single comparator ABIST operation on the full path of the interrupt needs to be started (register **ABIST_CTRL0**: 00001111b (0Fh)). The artificial failure, triggered by the ABIST controller, on the selected comparator will generate an interrupt (INTB) event. It is the responsibility of the µC to check the generation of this interrupt event on the triggered failure. As this is a test of the generation of an interrupt based on a failure event, there is no dedicated ABIST completion event, nor the **ABIST** bit in the interrupt flags will be set. Accordingly it is recommended to store the information about the started ABIST in the firmware.

After the interrupt has been generated the interrupt flag register shall be checked for the monitoring bit (**IF**.**MON**) set and the ABIST completion bit (**IF**.**ABIST**) not set.

The µC needs to read and check the status of the requested ABIST operation (**ABIST_CTRL0**.**STATUS**), the respective monitoring status flag (**MONSF1**, **MONSF2** or **MONSF3**) to be set according to the previous selection and **ABIST_SELECT0**, **ABIST_SELECT1** and **ABIST_SELECT2** bits to be cleared.

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Afterwards a test of all comparators which contribute to the interrupt generation shall be configured and started.

7.5.2.6 Abort conditions for ABIST operation

In case of an severe monitoring failure event (contribution to the secondary safety shutdown path) detected on a not selected comparator1) or a severe failure event not related to the voltage or bias current monitoring function during the proceeding of an ABIST operation on the comparators only (**ABIST_CTRL0**.**PATH** not set), the device will react as it is supposed to do in normal operation. Accordingly the monitoring, reset and safe state control are reacting. Bringing the device into safe state and trigger the **State Machine** to move into FAILSAFE or INIT state. The ABIST is aborted in this case.
In case of an ABIST operation on the full path (**ABIST_CTRL0**.**PATH** set) the comparators for voltage and bias current monitoring are blind for the time of the ABIST operation. Therefore it is recommended to do the test in safe state unless it is needed to start the test in NORMAL state (e.g. test of activation of secondary safety shutdown path). Severe failure events not related to the voltage and bias current monitoring will trigger the same device reaction as in usual condtion. Bringing the device into safe state and trigger the **State Machine** to move into FAILSAFE or INIT state. The ABIST is aborted in this case.
This ABIST abort will be recorded in the register **SYSFAIL**.**ABISTERR**. The artificial failure events, that have been generated until the abort of the ABIST due to the detected real failure, will be stored as well in the monitoring registers.

7.6 Microcontroller Programming Support

The device offers a microcontroller programming support feature, that can be used to avoid periodic reset triggering due to missing triggering of the window watchdog and error monitoring within the INIT timer. The activation of the microcontroller programming support feature shall be done by pulling the DEBUG pin to 5 V. The voltage shall be provided earliest with the enabling of the voltage reference. Therefore it would be one option to connect the DEBUG pin to the output VO_VREF during microcontroller programming.
The active microcontroller programming support feature includes the following changes to the normal operation of the device:

- The INIT timer will be stopped.
- The contribution of the window watchdog failure counter overflow to the reset will be blocked.
- The contribution of the functional watchdog failure counter overflow to the reset will be blocked.
- The contribution of the error monitoring to the reset will be blocked.

As only the contribution of the watchdogs and the error monitoring to the reset function is blocked/disconnected, the state machine and safe state control function are not affected. Accordingly an overflow of the window or functional watchdog failure counter will trigger a “Move to INIT” event, but without issuing a reset of the microcontroller.
The microcontroller programming support feature offers as well the possibility to move the device to any other state according to the state machine. E.g. in case PROG pin is high in NORMAL and there is a watchdog error counter overflow the device would move into INIT without issuing a reset.

8 Safe State Control Function

8.1 Introduction

The safe state control monitors safety related signals and controls the safe state signals SS1 and SS2.
The following description summarizes the contributors to the safe state control function and the possibilities to adjust them.
Principle of operation:
The safe state control function monitors the following inputs:
- Result of the Error Monitoring. “Error”-signal at pin ERRIN is expected to be a toggling signal. A permanent low or high signal will be detected as an error.
- Over and under voltage of the microprocessor related regulators
- Result of Window Watchdog Failure Counter Threshold Comparator. Whether threshold ∑WWO for “Invalid window watchdog triggering” has been exceeded.

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• Result of Functional Watchdog Failure Counter Threshold Comparator: Whether threshold ∑FWO for “Invalid functional watchdog triggering” has been exceeded.
• Thermal shutdown signal (TSD) for relevant events moving the device into FAILSAFE state.
• Internal clock
• SPI state transition request. A valid GoToNORMAL command triggers the signals SS1/2 to switch high in case the other boundary conditions are fulfilled. Moving the device out of NORMAL state by SPI command will switch the signals SS1 and 2 (optionally delayed by t_{SS_DLY}) to low.
The following parameters of the safe state control function are programmable via SPI, this settings can be done during INIT, NORMAL, SLEEP and WAKE state, WWD and FWD configuration and error pin configuration including disabling of individual functionality via protected register:
• Number of invalid watchdog triggers, that lead to activating SS1 and SS2: There are two watchdog trigger failure counters implemented, one for the window watchdog the other for the functional watchdog. Every counter increments by two at every invalid watchdog triggering and decrements by one at every valid watchdog triggering. (valid and invalid triggering is described in chapter functional and window watchdog). An incrementing change is indicated by an interrupt. A decrementing change is not indicated by an interrupt. The thresholds can be programmed by SPI command for each counter individually. This function might be used to test the watchdog function.
• Immediate reaction or recovery delay reaction, only related to input signal ERR: This parameter determines whether the safe state control will immediately react to an error indicated by SMU or react after a certain delay, if the error indication is still present. In recovery delay reaction the safe state control will generate an interrupt and start the programmed recovery delay time. If within this time the error should disappear (means the error signal should toggle again, before the recovery delay time has ended), the safe state control will keep the safe state output SS1/2 high. If within this time the error signal should not disappear and maintain the error indication (means the error signal should not toggle again, before the recovery delay time has ended), the safe state control will activate the safe state signals SS1 and SS2 after the recovery delay time has ended.
Immediate reaction means reaction after signal detection delay time.
• Recovery delay time Δt_{REC}, only related to input signal ERR: An error (violation of valid ERR signal) has to be longer than this delay time to lead to activating the safe state signals SS1 and SS2. This delay time is only active if recovery delay time mode was selected.
• Delay time t_{SS_DLY} between safe state signal 1 and safe state signal 2
The safe state function offers two output signals, both of them as output stages to drive external switches (additional driver stage is necessary):
• Safe state signal 1 (present at pin SS1)
• Safe state signal 2 (present at pin SS2), it may be delayed to safe state signal 1 by an adjustable delay time Δt_{SS_DLY} (via SPI)

Error signal from microcontroller safety management unit (SMU) at pin ERRIN:
The error monitoring function requires a toggling signal at pin ERRIN with a determined timing in case of fault-free operation of the microcontroller by its SMU. This toggling signal is considered as a “being alive” indication. An error should be indicated by a constant low signal. A constant high signal will also be regarded as a failure indication, probably caused by a short circuit. The result is given to the safe state control.

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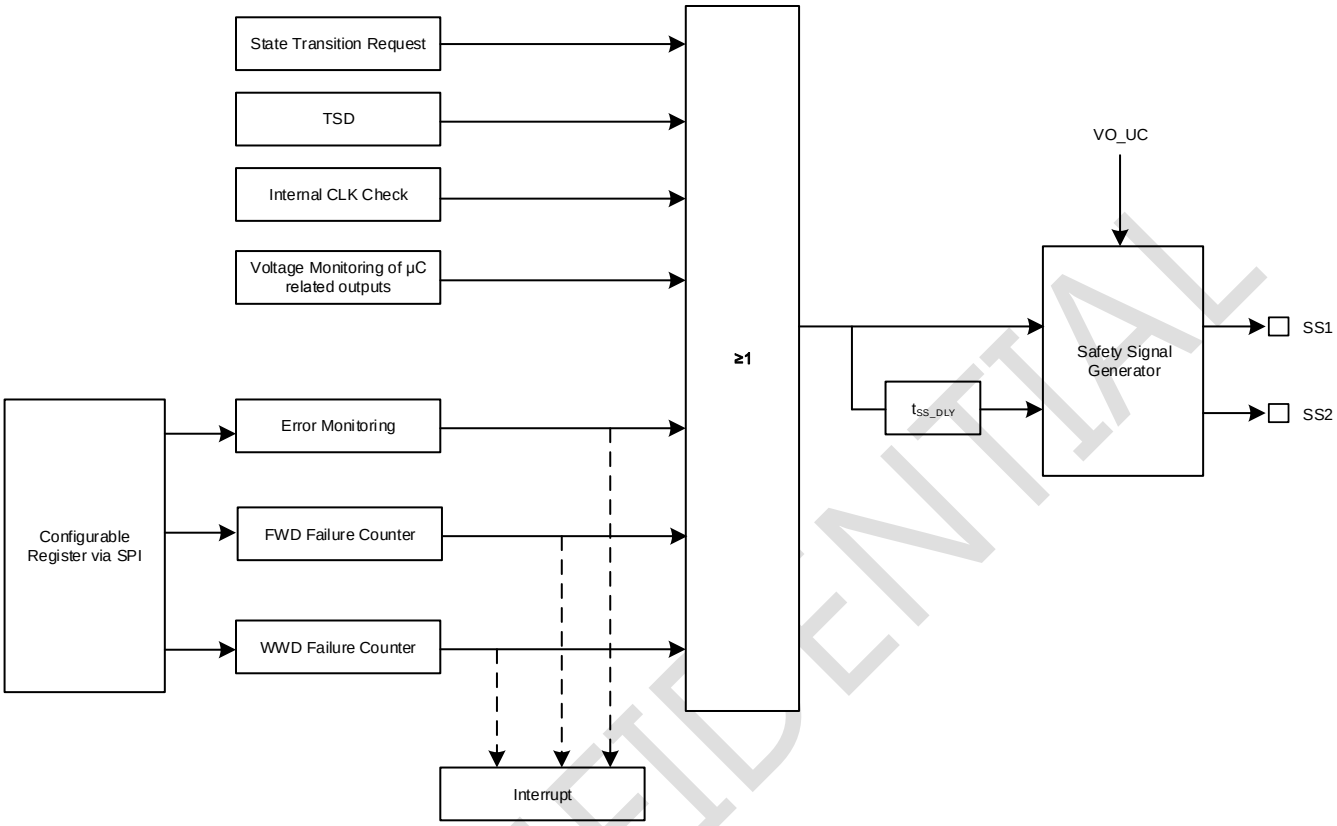


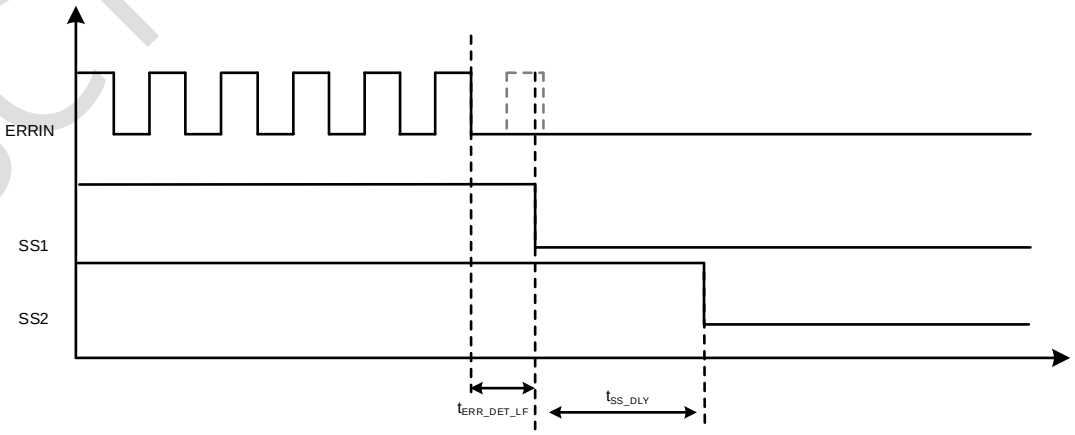
Figure 40. Principle of post regulators

8.2 Reaction on Microprocessor Safety Management Unit (SMU - Pin ERRIN)

8.2.1 Immediate reaction on ERR monitoring failure

The microprocessor safety management unit (SMU) indicates a serious error by stopping the toggling signal at pin ERRIN, immediate reaction to error signal is set:

- **ERRIN signal remains low**



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Figure 41. Flow diagram reaction on SMU signal (ERRIN signal remains low)

• ERRIN signal remains high

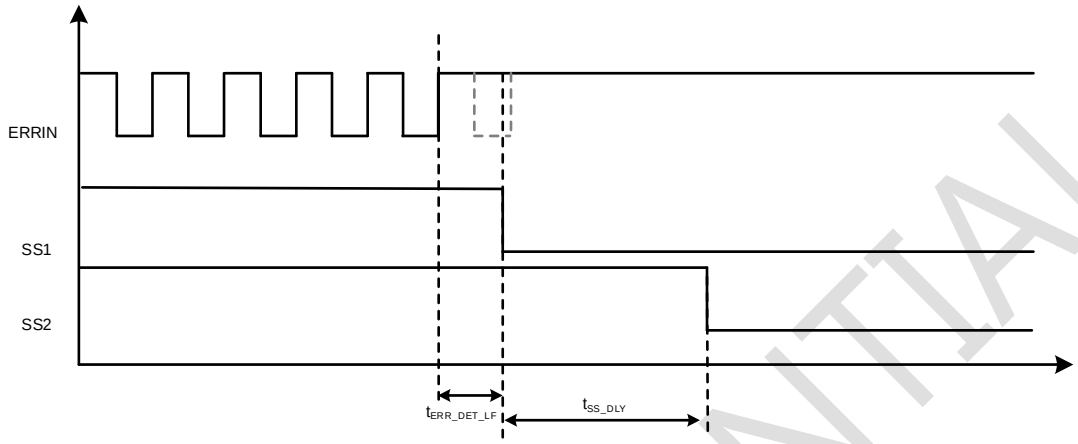


Figure 42. Flow diagram reaction on SMU signal (ERRIN signal remains high)

• ERRIN signal frequency too high

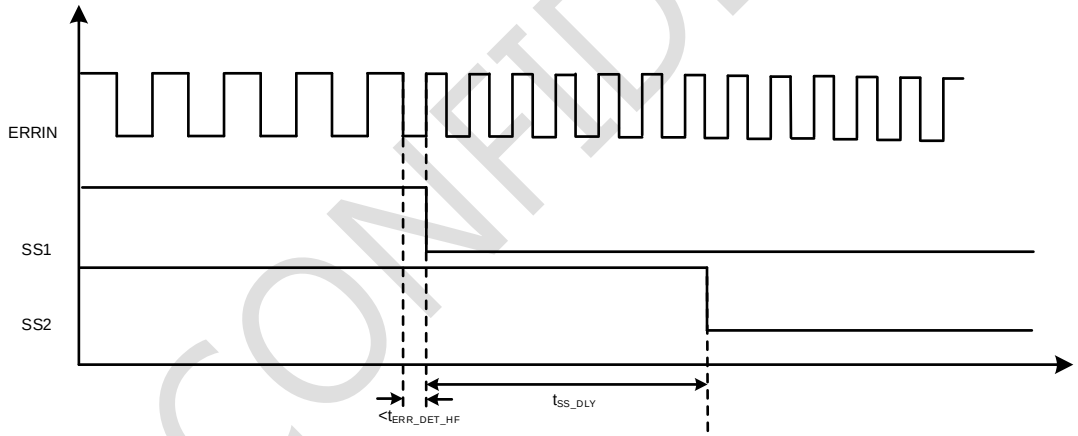


Figure 43. Flow diagram reaction on SMU signal (ERRIN signal frequency too high)

• ERRIN signal too long with changing high and low times(duty cycle can vary as well)

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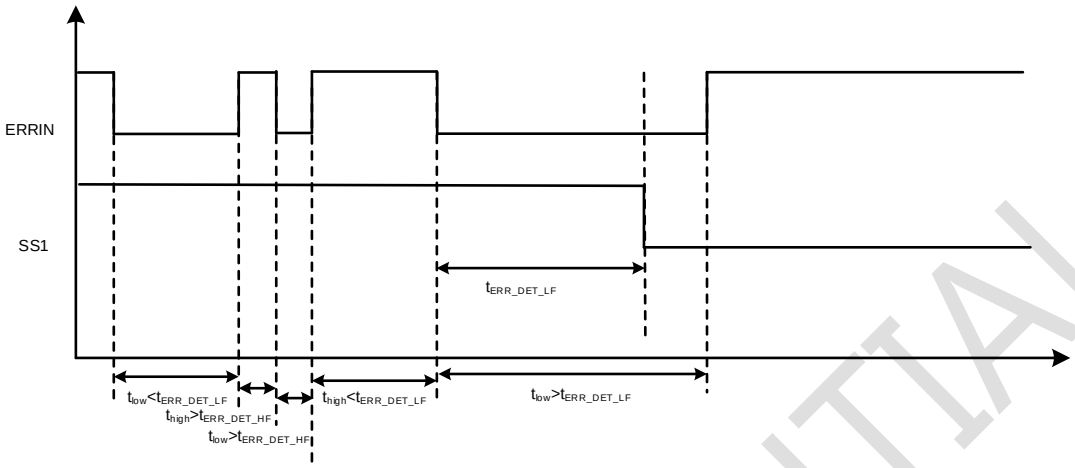


Figure 44. Flow diagram reaction on SMU signal (ERRIN signal too long)

• ERRIN signal too short with changing high and low times(duty cycle can vary as well)

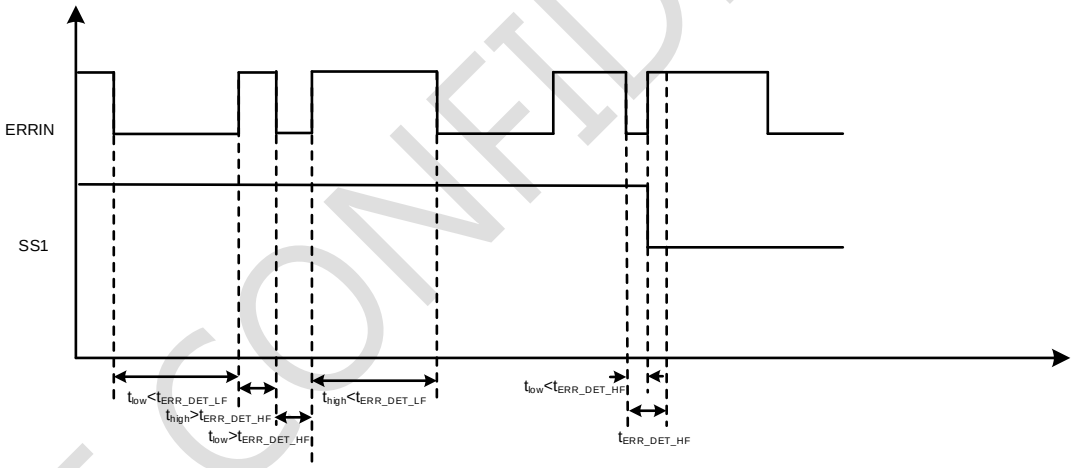


Figure 45. Flow diagram reaction on SMU signal (ERRIN signal too short)

8.2.2 Recovery delay reaction on ERR monitoring failure

The microprocessor safety management unit (SMU) indicates a serious error by stopping the toggling signal at pin ERRIN, recovery delay time reaction to error signal is set - the SMU is given time to recover:

• ERRIN signal remains low or high

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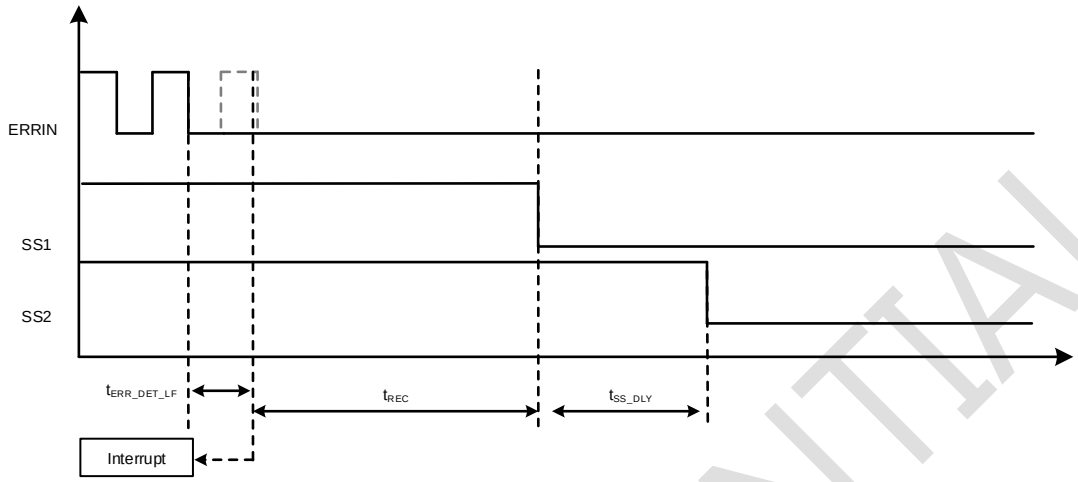


Figure 46. Flow diagram reaction on SMU signal, error longer than recovery delay time

• ERRIN signal frequency too high

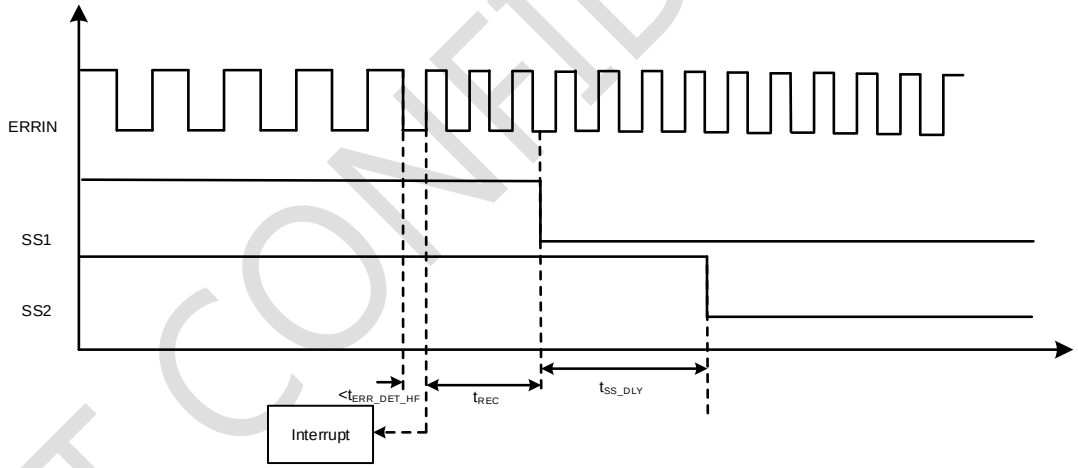


Figure 47. Flow diagram reaction on SMU signal, error longer than recovery delay time (ERRIN signal frequency too high)

• ERRIN remains low or high and error shorter than recovery delay time

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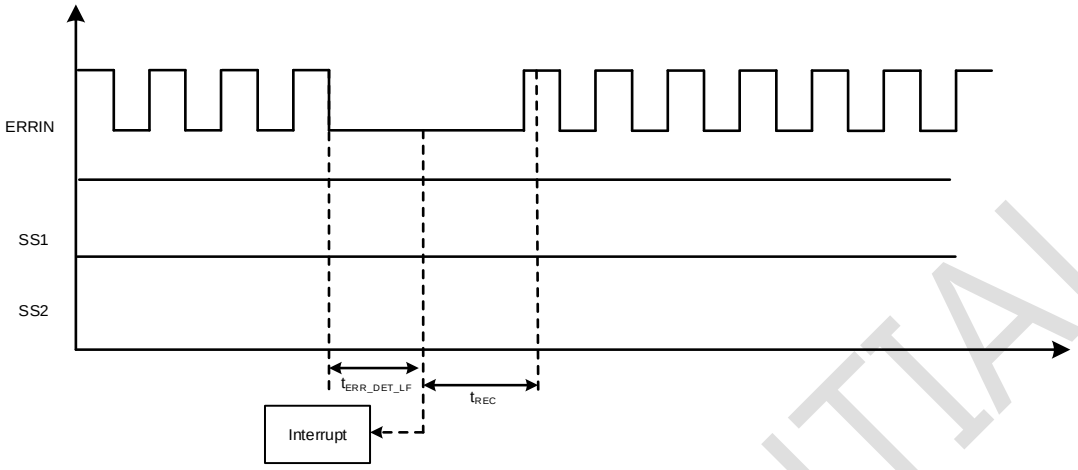


Figure 48. Flow diagram reaction on SMU signal, error shorter than recovery delay time

• ERRIN signal frequency too high and error shorter than recovery delay time

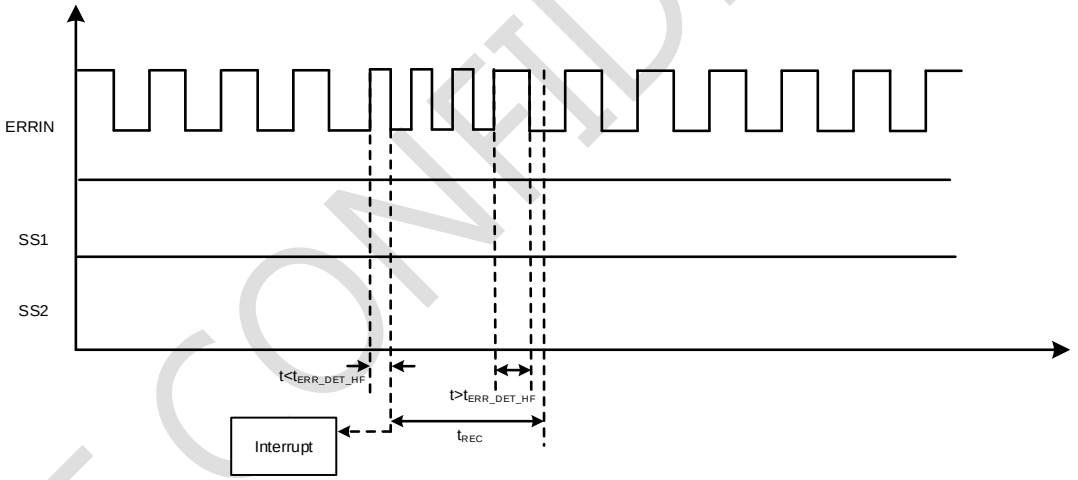


Figure 49. Flow diagram reaction on SMU signal, error shorter than recovery delay time (ERRIN signal frequency too high)

8.3 Reaction on Error Triggered State Transitions

• Soft reset

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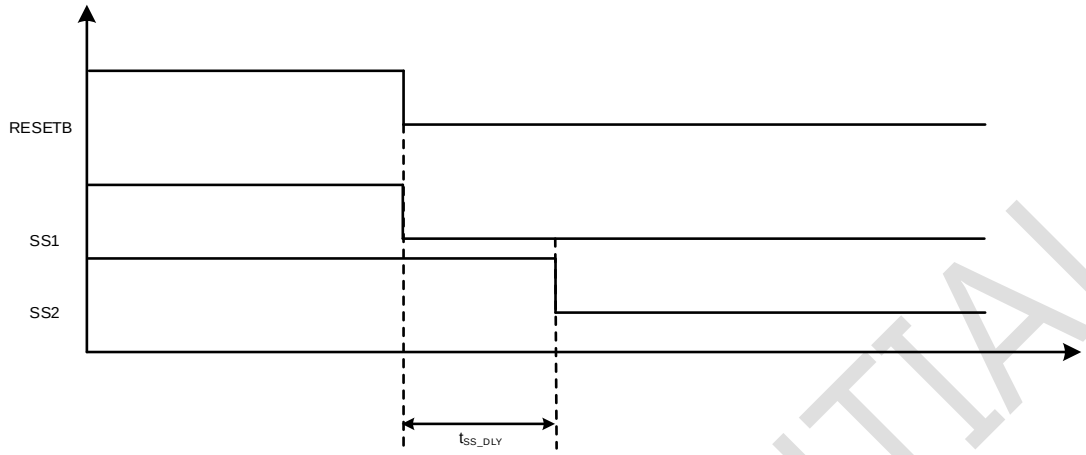


Figure 50. Flow diagram reaction on an error triggered state transition- soft reset

• **Hard reset**

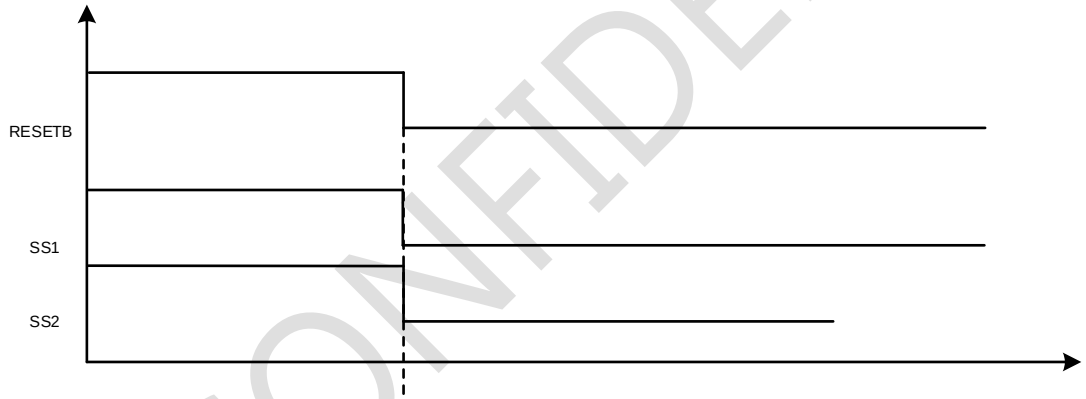


Figure 51. Flow diagram reaction on an error triggered state transition- hard reset

8.4 Reaction on Window Watchdog Output (WWO)

The SCT61490S has an implemented window watchdog failure counter (**WWDSTAT**.**WWDECNT**). The counter increments by two at every invalid window watchdog triggering and decrements by one at every valid window watchdog triggering.
The status of the window watchdog failure counter is written in the so called window watchdog status counter. Any incrementation of the window watchdog status counter is indicated by an interrupt. Any decrementation of thewindow watchdog status counter is not indicated by an interrupt. The content of the window watchdog status counter cannot be less than zero.
The threshold for activating the safe state signals SS1 and SS2 ΣWWO can be changed in INIT, NORMAL and WAKE state. (**WDCFG0**.**WWDETHR**)
The content of the status counter will be compared to the programmed threshold ΣWWO (**RWDCFG0**.**WWDETHR**). If the content of the status counter is equal or higher than ΣWWO, the safe state signals SS1 and SS2 will be activated (low).

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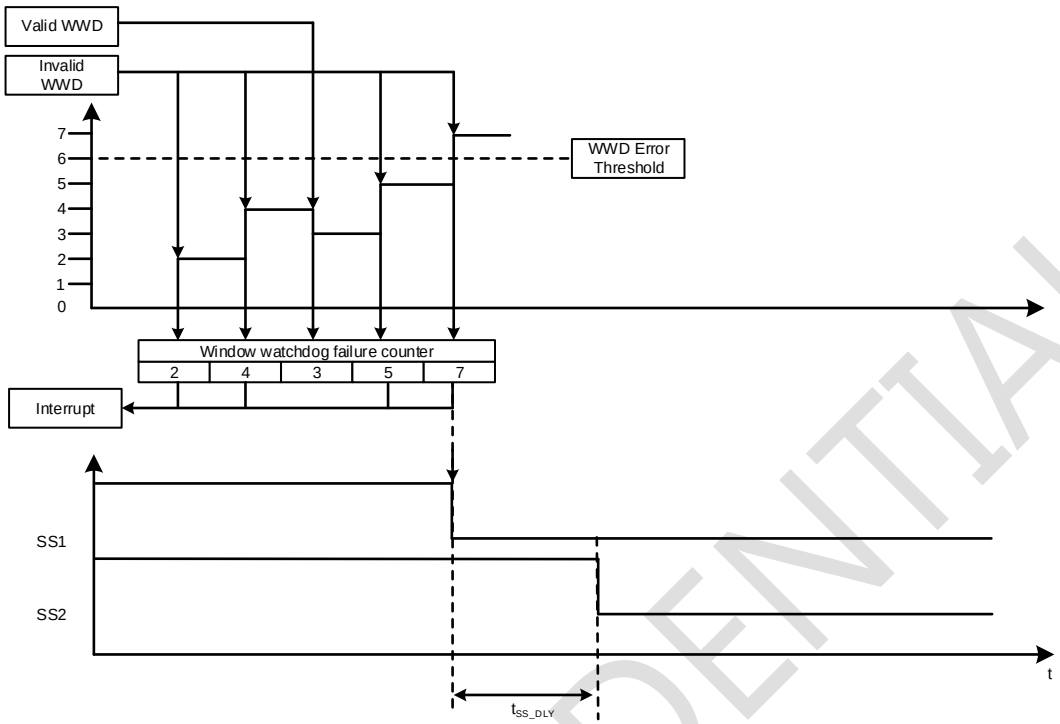


Figure 52. Flow diagram reaction on WWO

8.5 Reaction on Functional Watchdog Output (FWO)

The SCT61490S has an implemented functional watchdog failure counter (**FWDSTAT1**.**FWDECNT**). The counter increments by two at every invalid functional watchdog triggering and decrements by one at every valid functional watchdog triggering. (For specification of valid and invalid triggering please refer to chapter functional and window watchdog).

The status of the functional watchdog failure counter is written in the so called functional watchdog status counter. Any incrementation of the functional watchdog status counter is indicated by an interrupt. Any decrementation of the functional watchdog status counter is not indicated by an interrupt. The content of the functional watchdog status counter cannot be less than zero.

The threshold for activating the safe state signals SS1 and SS2 ΣFWO can be changed in INIT, NORMAL and WAKE state. (**WDCFG1**.**FWDETHR**)

The content of the status counter will be compared to the programmed threshold ΣFWO (**RWDCFG1**.**FWDETHR**). If the content of the status counter is equal or higher than ΣFWO, the safe state signals SS1 and SS2 will be activated (low).

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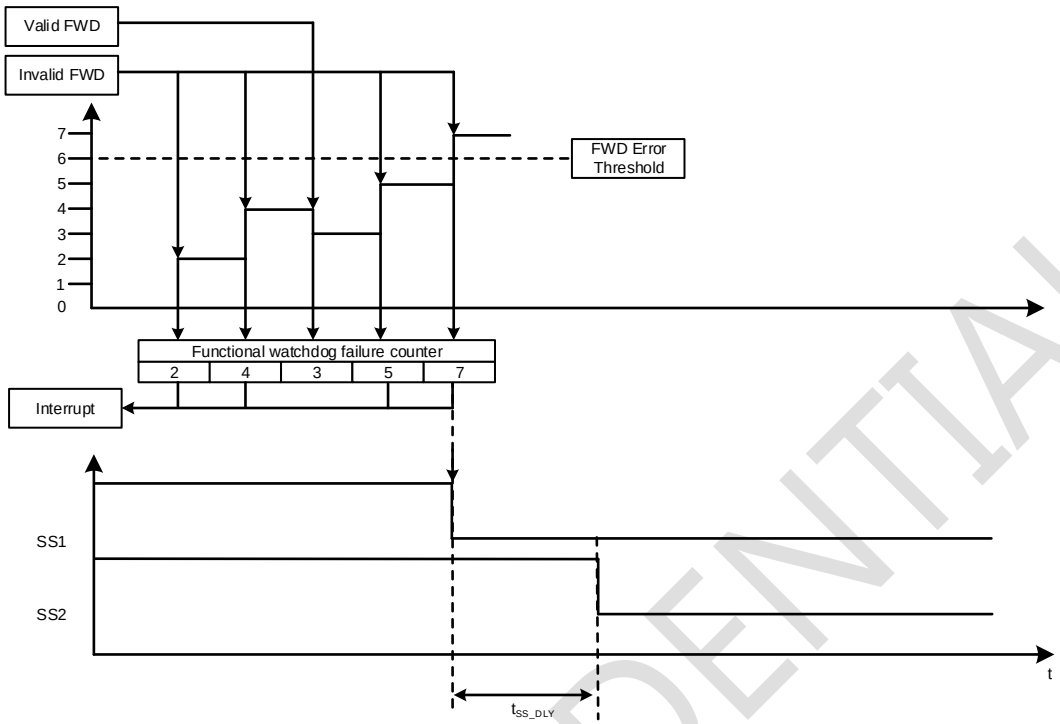


Figure 53. Flow diagram reaction on FWO

8.6 Reaction on Thermal Shutdown (TSD)

The thermal shutdown (TSD) indicates temperature overstress: on the chip: As a consequence all pre and post regulators will be shut down immediately.

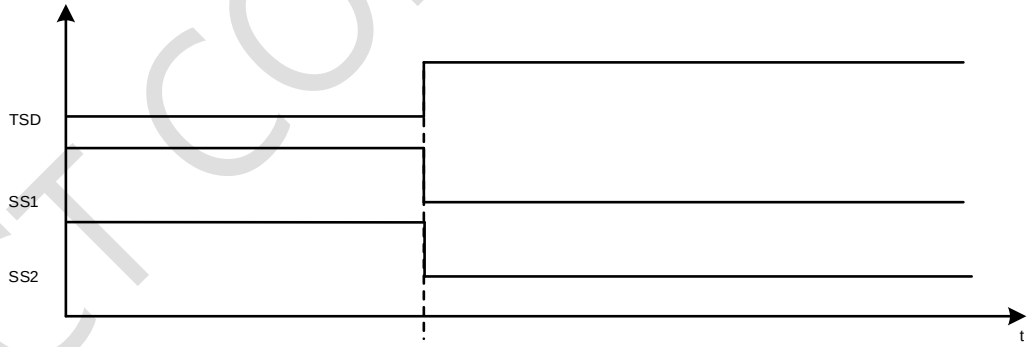


Figure 54. Flow diagram reaction on TSD

9 SPI - Serial Peripheral Interface

9.1 Introduction

Main functions

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The serial peripheral interface bus or SPI bus is a synchronous serial data link that operates in full duplex mode. The SCT61490S communicates in slave mode where the master (µC) initiates the data frame. The SCT61490S should be addressed via a dedicated chip select line. This allows a connection of other slave devices to the SPI bus.

Data transmission

To begin a communication, the µC first configures the clock, using a frequency less than or equal to the maximum frequency the SCT61490S supports. The µC pulls down the chip select for the SCT61490S.

Functional description

SPI basic access: All data on MOSI (pin SDI) is captured on the rising edge of SPI clock signal (pin SCL) and shifted on the falling edge of SPI clock signal (pin SCL). The same methodology needs to be applied in the SPI master for MISO (SDO). A read operation has to start with CMD-bit being 1'b0 and a write operation has to start with CMD-bit being 1'b1.

In case of a write operation is performed the written command to SDI is looped back to SDO.

The parity is calculated for the output data stream in case a read operation is performed. The data for the calculation consists of 1'b1, status [5:0] and rd_data[7:0]. The parity bit is set to '1' if the number of '1' in the output data stream is odd, i.e.XOR function between all 15 bits to send out.

Parity is checked on write data. The parity is calculated on the incoming bit stream for the cmd bit, the six address bits and the eight data bits.

Configuration via SPI can be done anytime, if the state machine (FSM) is in INIT state, NORMAL state, WAKE state or SLEEP state. During SLEEP state the SPI has a decreased maximum clock frequency.

SPI access timing can be found in the following diagram:

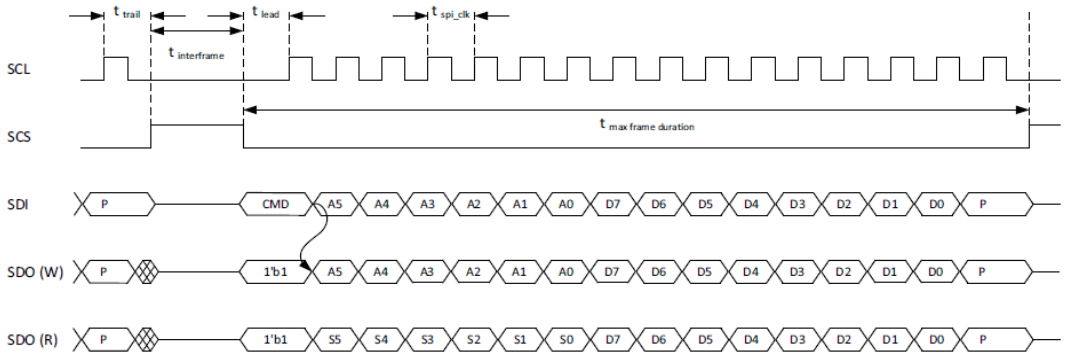


Figure 55. SPI - frame in normal mode

SPI MISO:

During write, data from MOSI is directly looped back, during read, the addressed register content will be provided in the very same SPI frame

• The cmd bit is always set to 1'b1. All other status bits are set to zero.

SPI errors:

• Wrong parity bit during write, write data is ignored.

• Write to invalid address, write data is ignored.

• Wrong number of SPI clock cycles while CSB is low, write data is ignored, read data is provided by the device with each SPI clock cycle.

• Read from invalid address (all data bits zero returned on MISO for read data). For this case the parity bit is inverted/corrupted after complete calculation by the device.

• Invalid frame duration, write data is ignored and the output driver for SDO is turned off internally by the device after t_{SPI_fl}. Read data is provided with each SPI clock cycle as long as CSB is low for less than t_{SPI_fl}.

• If the number of SPI clock cycles is different than 16 and an invalid frame duration error is detected by the device, the invalid frame duration status flag is set and the wrong number of SPI clock cycle status flag is set.

In case of an SPI error occurs, an interrupt will be generated.

Interrupts on SPI errors are initiated only after CSB has been driven high or the frame time-out occurred.

9.2 SPI Write Access To Protected Registers

Certain internal registers (**SYSPCFG0**, **SYSPCFG1**, **WDCFG0**, **WDCFG1**, **FWDCFG**, **WWDCFG0**, **WWDCFG1**) need to be protected against being overwritten accidently. The status of the protection can be checked by reading

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the **LOCK** bit in the register **PROTSTAT**.
Write access to these registers is only possible after a dedicated 32 bit UNLOCK sequence has been sent via SPI. The four bytes need to be send without any other SPI write access in between. Error in doing so will reset the sequence detection, i.e. a new UNLOCK sequence has to be send. An interrupt is generated and the number of successfully detected UNLOCK sequence bytes is set to zero if a write access to any other register then **PROTCFG** is detected in between. The access to the protected registers is possible in INIT, NORMAL and WAKE state.
The UNLOCK sequence consists of a 32-bit sequence of 4 consecutive bytes (1: 0xAB; 2:0xEF; 3:0x56; 4:0x12) which have to be sent with no other SPI write access in between. The correctness of every written byte can be checked by reading the register **PROTSTAT**. Once the UNLOCK sequence has been performed successfully, any protected configuration request register can be written. In order to ensure proper writing to the protected configuration request registers the microcontroller shall read back the register values and verify the correctness by checking data. The data bits written to the protected configuration request registers are send back inverted during read operation, that means the microcontroller can calculate an XOR of the register data read and expected. The results should be 0xFF in case of correct register data. The SCT61490S will not check the correctness of the values in the register.
All protected configuration request register values are captured by the respective functions only after a successful LOCK sequence has been performed. A successful LOCK sequence consists of a 32-bit sequence of 4 consecutive bytes (1: 0xDF; 2:0x34; 3:0xBE; 4:0xCA) which have to be send with no other SPI write access in between. The correctness of every written byte can be checked by reading the register **PROTSTAT**.
Error in doing so will reset the sequence detection, i.e. a new LOCK sequence has to be sent. In this case (any SPI write access in between LOCK sequence) an interrupt is generated.
Upon detection of a successful LOCK sequence the configuration registers and all internal functions are updated with the values from the protected configuration request registers. It is the responsibility of the uC to ensure all registers are configured properly by either writing a new value into a particular register or by reading back a register which is supposed to be unchanged. Partial reconfiguration of the protected registers, i.e. configuring just a single function and leaving other functions unchanged is not supported as with the successful LOCK sequence all protected configuration request registers are taken over into the configuration (**RSYSPCFG0**, **RSYSPCFG1**, **RWDCFG0**, **RWDCFG1**, **RFWDCFG**, **RWWDCFG0**, **RWWDCFG1**).
After the LOCK sequence an internal configuration time of max. 60 µs has to be considered to ensure that the new configuration is taken over.
Affected functions:
• All watchdog configuration registers for WWD and FWD.
• Enabling of WD while the device is in SLEEP state
• All Error pin monitoring configuration registers
• Enabling of Error pin monitoring while the FSM is in SLEEP
• A dedicated register to enable or disable the STDBY LDO
• Configuration of SS2 delay time failure events not leading to FAILSAFE state
Read access to any protected configuration request register is always possible.

9.3 SPI Write Initiated State Transition Request And Regulator Configuration

A State machine transition can be initiated via SPI command(s). In case the state of any selectable voltage source (post regular) is expected to change for the next state, this information has to be sent together with the command into the same register. In case the setting for a particular voltage source (post regulator) is supposed to change but the state needs to be unchanged, the same approach can be applied. This basically means, the SPI command contains the current state of the FSM but a different setting for configurable voltage source (post regulator).
In order to request a state transition and/or a change of the LDO configuration the request data have to be written to two separated registers **DEVCTRL** and **DEVCTRLN** after each other consequently. The data written to **DEVCTRLN** have to be inverted bitwise compared to the data written to **DEVCTRL**. The request will be only accepted when the two registers are written consecutively after each other (first **DEVCTRL** and second **DEVCTRLN**) and will be taken over with the rising edge of the CS at the end of the second command.
In case of an invalid request (wrong sequence or DEVCTRLN not inverted to DEVCTRL) it will be rejected, an interrupt is generated and the corresponding status flag (**NO_OP**) is set. Incase of an invalid state transition request, the request is ignored without issuing an interrupt.

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10 Interrupt Generation

A dedicated interrupt generation block is implemented which is handling requests from independent sources to generate an interrupt. The different requesters are as follows:

• State machine in case:

– A requested state transition has not been performed successfully, e.g. SLEEP state could not be entered because of LDO_µC current consumption above the selected threshold level.

– A requested state transition from SLEEP has been performed successfully, i.e. the system has either successfully entered WAKE state. The uC may only send (additional) SPI commands after an interrupt event has been generated by the system. The purpose of the interrupt event is to inform the uC that a state transition has been performed successfully and that the system is capable of performing SPI communication at full SPI speed.

• Watchdog, an interrupt request is generated if the Watchdog is not serviced properly and configured in a way to allow service errors to occur, i.e. an error counter threshold value of more than 2 is configured. In this case an interrupt is generated only if the error counter threshold is not exceeded due to this error.

• Error pin monitoring, an interrupt request is generated if the error pin monitoring block detects an error and is configured in a way to allow occurrence of this error for a certain amount of time (recovery delay action enabled). In this case an interrupt is requested if an error is detected by the error pin monitoring and the recovery delay has not expired.

• Monitoring Block, an interrupt request is generated based on the defined system reaction described in INTERRUPT events

• Overtemperature warnings and over temperature shutdown of communication LDO

• Overcurrent conditions of voltage reference or standby LDO

• SPI block in case an SPI error has occurred

• ABIST operation has been completed

• Double bit error in the protected configuration

An interrupt is generated to inform a connected uC that a non-severe system condition has occurred. This allows the uC to perform proper action based on the source of the interrupt. A single interrupt line exists, which is high on default. All Internal interrupt sources are enabled by default and cannot be disabled.

An interrupt is signaled by pulling the interrupt line low for at least t_{INT} (interrupt min. pulse width) after an internal interrupt condition occurs. The interrupt line will be driven high if all of the **IF** register flag(s) has/have been cleared via SPI operation earliest after t_{INT} has expired but latest after t_{INTTO} has expired.

Special cases:

• If an interrupt is signaled by pulling INTB low and not all interrupt status flags are cleared by the uC within t_{INTTO}, the INT will stay low until t_{INTTO} has expired, but no additional interrupt will be generated. Information about a pending interrupt event can be derived via the INTMISS status flag. This status flag is cleared each time the interrupt line is driven low.

• If an interrupt is signaled by pulling INTB low and an additional bit is set in the **IF** register interrupt flag after the interrupt bits have been read by the uC and this outdated information is used to clear the interrupt flags, the interrupt line will stay low until t_{INTTO} has expired, but no additional interrupt will be generated. Information about a pending interrupt event can be derived via a status flag.

• After releasing the interrupt line to high, the interrupt line will stay high for at least t_{INTTO} regardless if any additional internal interrupt condition has occurred or not. If a new interrupt event occurs during the delay time out (t_{INTTO}), this will be signaled by generating a new pulse after the delay time out t_{INTTO}.

All interrupt sources can only be cleared by a “write-1-to-clear” (W1C) SPI operation, i.e. writing a logic one to the corresponding bit(s) in the interrupt register will clear the event.

Interrupt events are organized in a two level approach. The first level (interrupt flag) provides information about different groups of interrupt events. The second level (status flags) provides detailed information about which particular event(s) generated the interrupt. To service an interrupt one would only need to write the interrupt flag register (**IF**). The status flag registers are only meant to provide detailed information. However all status flags can be cleared as well.

Recommended interrupt service routine:

After an interrupt has been detected by an uC, the recommended interrupt service routine would need to perform the following tasks via SPI:

1. Read interrupt flag register (**IF**)
2. Read status flag register(s) based on information from first read
3. Take the proper action based on interrupt flag(s) and status flag(s)

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4. Write back the status flag register(s) to clear particular status flag(s)
5. Write back the interrupt flag register (**IF**) with the previously read value to clear
6. Recommended: Read interrupt flag register (**IF**) again to check for occurrence of another interrupt event. In case step back to 2).
7. Writing back the interrupt register (**IF**) will release the interrupt line INTB if all bits are cleared (interrupt timing requirements will be fulfilled).

An interrupt is only generated after the reset signal to the uC has been released. An interrupt event which occurred while the reset line for the uC is still active is not signaled at the interrupt line but the particular status bit for this event is set.

Details about the timing of the interrupt line are depicted in the following figure:

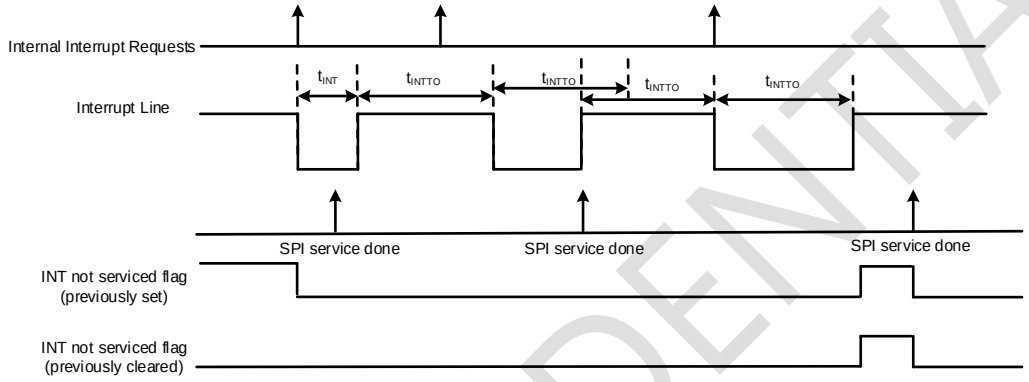


Figure 56. Interrupt timing

Details about the system behavior in case not all interrupt status flags have been cleared are depicted in the following figure:

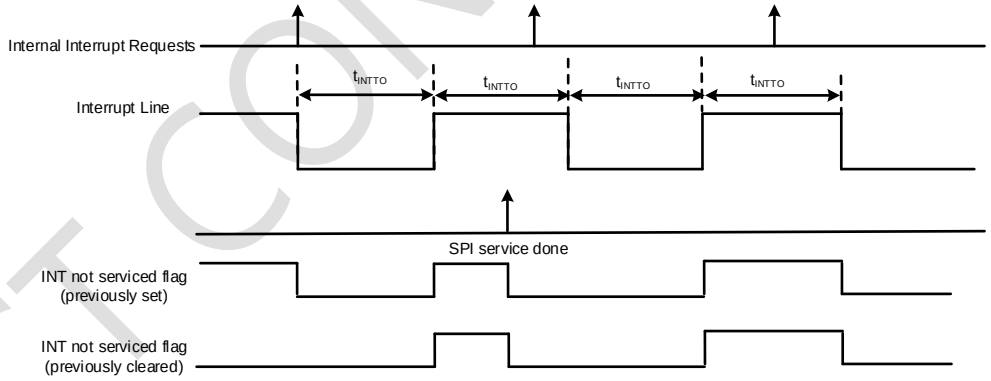


Figure 57. Interrupt timing without service in time

An interrupt is always generated if an internal status flag is set, irrespective of the current state of this status flag. For example, if a parity error on SPI communication is detected for the first time, the flag **SPISF.PARE** is set and an interrupt is generated. This flag will also set the corresponding SPI interrupt flag (**IF.SPI**). If the flag **IF.SPI** is not cleared, but a second SPI parity error occurs, a new interrupt will be generated regardless. The timings shown in the two figures above will be fulfilled for generating a new interrupt.

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11 Window Watchdog And Functional Watchdog

11.1 Introduction

Two independent types of watchdogs are implemented in the SCT61490S:
• A standalone window watchdog (WWD) with programmable input trigger signal (either pin WDI or trigger via SPI command to **WWDSCMD** register)
• A standalone functional or question/answer watchdog (FWD).
The watchdogs have independent timers and error counters, which allows to run both watchdogs in parallel.

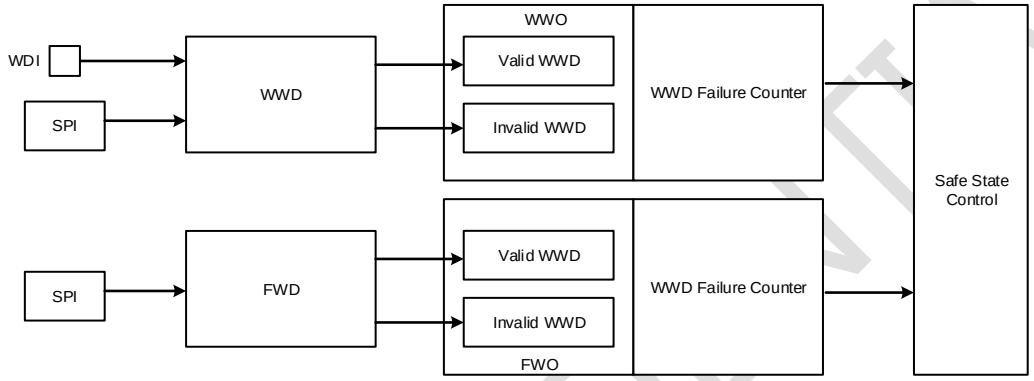


Figure 58. Window watchdog and functional watchdog

Description:
• The functional watchdog is not synchronized to the window watchdog, both are fully independent.
• The functional watchdog and the window watchdog can be activated and deactivated independently.
• The result of the watchdogs (valid or invalid triggering) are monitored independently by the related watchdog failure counters.
• The status of the window watchdog is WWO, it may have the values “Valid WWD triggering” or “Invalid WWD triggering”
• The status of the functional watchdog is FWO, it may have the values “Valid FWD triggering” or “Invalid FWD triggering
• The influence of the settings of both watchdogs on safe state control is described in chapter safe state control for better understanding

11.2 Window Watchdog

11.2.1 Operation of WWD

Principle of Operation
The window watchdog is integrated in the SCT61490S to monitor the microcontroller. The microcontroller that is being monitored has to provide periodical triggering within the "Open Windows". A triggering can consist of a falling edge on the WDI pin or writing to the register **WWDSCMD** by an SPI command depending on the configuration. This triggering terminates the “Open Window”. The watchdog output indicates a “Valid” or “Invalid” WWD triggering to the WWD failure counter. In case of a “Valid” triggering a “Closed Window” is started. In case there is no triggering during the “Open Window” or a triggering during a "Closed Window", the watchdog output indicates an “Invalid WWD triggering” to the WWD failure counter and a new “Open Window” is started.
In case the microcontroller is not able to trigger the window watchdog with a correct timing, it is assumed that the microcontroller doesn’t work as expected. The microcontroller will get informed by the SCT61490S and a reset in case of multiple failure events.
Configuration
The following parameters of the window watchdog can be configured in INIT, NORMAL and WAKE state:
• The triggering can be set either to pin triggering (pin WDI) or triggering via SPI command (register **WWDSCMD**). The default configuration is the triggering via SPI.

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• The length of open and closed window can be modified according to the application needs by SPI. (combination of cycle time **WDCYC** and number of cycles for open **OW** and closed **CW** window)
• The threshold for the window watchdog failure counter overflow can defined by SPI

Initialization

The window watchdog will become active in INIT state as soon as reset output pin RESETB turns from low to high. After activation the watchdog opens a so called “Long Open Window” (LOW) of duration of t_{LOW}. During the ”Long Open Window” the window watchdog expects a valid triggering, which has to be provided via SPI in case the default configuration is kept, since any signal to watchdog trigger pin WDI is ignored. This is to avoid wrong triggering at pin WDI due to glitches at the micro controller outputs during startup and initialization.
The microcontroller can change the configuration of the window watchdog during the “Long Open Window” to change the trigger selection as well as the times for the “Open” and “Closed Window”. With a reconfiguration the window watchdog will be restarted with the new configuration. A “Open Window” will be started accordingly, expecting a valid triggering by the selected triggering input.
If no valid triggering or configuration of the watchdog takes place during the “Long Open Window”, the window watchdog recognizes an “invalid WWD triggering”. If the INIT timer expires with an invalid WWD triggering present, a so-called “Soft Reset” will be issued. After the so-called “Soft-Reset” the window watchdog opens a new “Long Open Window”. This is not indicated by interrupt. The repetition of “Long Open Windows” is limited. Should within the second “Long Open Window” the window watchdog not be triggered correctly, a normal or “hard” reset will occur, which means that pin RESETB goes to zero and the post regulator output voltages will be switched off. After the third “Long Open Window” without valid triggering in a row the state machine will bring the device into “FAILSAFE state.

Normal Operation

A trigger signal within the "Long Open Window" will terminate the "Long Open Window" and start the "Closed Window". The "Closed Window" has a fixed duration for operation without invalid triggering.. During normal operation no valid trigger signal is allowed during the "Closed Window”. If a valid trigger signal is received within the “Closed Window”, the window watchdog recognizes “invalid WWD triggering”. The “Closed Window” will be terminated with this invalid triggering and an “Open Window” will be started.
An “invalid WWD triggering” will increment the window watchdog failure counter by two. This is indicated by interrupt. After the “Closed Window” has ended, the window watchdog starts an “Open Window”.
Within the “Open Window” a valid trigger signal is expected. If a valid trigger signal is received within the "Open Window" the watchdog terminates the "Open Window" and starts the "Closed Window". “Valid WWD triggering” will decrement the window watchdog failure counter by one in case it is greater than zero, this is not indicated by interrupt.
If no valid triggering should be received during the “Open Window”, the window watchdog recognizes “Invalid WWD triggering” and increments the window watchdog failure counter by two and a new “Open Window” is started. This is indicated by interrupt.
In normal operation, the watchdog continues to cycle between the "Open Window" and "Closed Window" as long as valid triggering is received.

Window watchdog output WWO

The window watchdog output WWO is an internal signal: It is connected to the safe window watchdog failure counter. The value of WWO is either “Valid WWD triggering” or “Invalid WWD Triggering”.

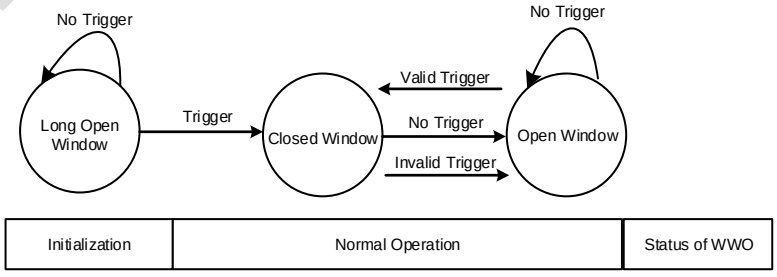


Figure 59. Watchdog state diagram

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Window watchdog trigger pin WDI

The watchdog input pin WDI has an integrated pull-down current I_{WDI_PULL}. The watchdog input WDI can transition to high within the "Closed Window" or during the following "Open Window".

Valid Trigger Signal at WDI

Watchdog input WDI is periodically sampled with a period of t_{WD_SAMPLE}. A valid trigger signal is a falling edge from V_{WDI_H} to V_{WDI_L}. To improve immunity against noise or glitches on the WDI input, at least two high samples followed by two low samples are required for a valid trigger signal, the valid triggering is considered with the second consecutive sampling point measuring low signal. For example, if the first three samples (two high one low) of the trigger pulse at pin WDI are inside the “Closed Window” and only the fourth sample (the second low sample) is taken in the “Open Window” then the watchdog output WWO will indicate “valid WWD triggering”.

Invalid Triggering at WDI

No trigger signal detected during the "Open Window" or a trigger signal detected during the "Closed Window", is considered invalid triggering. Watchdog output WDO indicates “invalid triggering” immediately after no valid trigger during the "Open Window" or immediately if a trigger signal is detected during the "Closed Window".

11.2.2 Timing Diagrams

Correct triggering

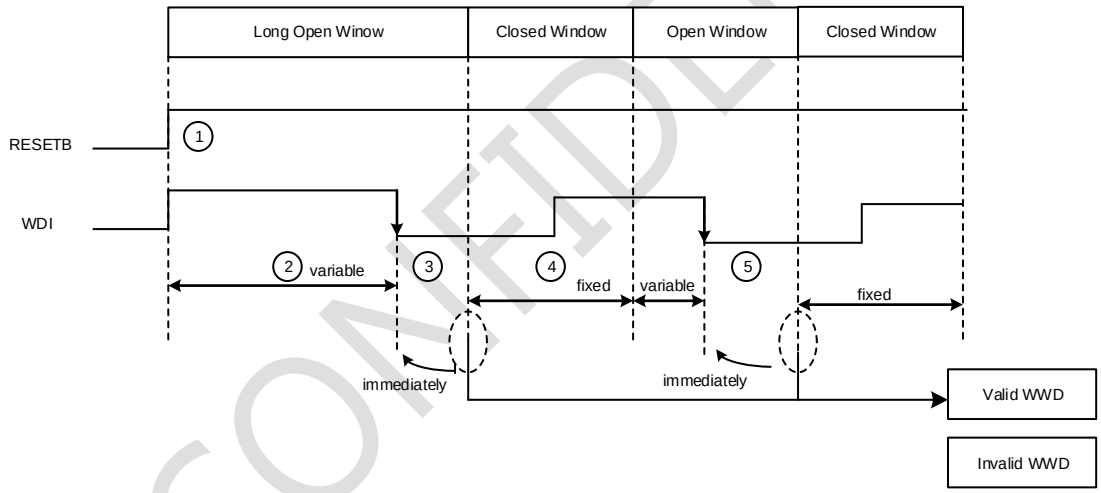


Figure 60. Normal operation: Correct triggering

1. The “Long Open Window” starts in INIT state if the reset output of RESETB (monitoring the microcontroller related voltages) turned high. In case the window watchdog was deactivated in SLEEP, the first Open Window starts with the transition from SLEEP state to WAKE state which is indicated by interrupt. The time of this first Open Window depends on the configured cycle time and is 600 ms (**WDCYC** = 1) or 60ms (**WDCYC** = 0)
2. During the “Long Open Window” valid triggering of the WWD according to the configured trigger selection is expected. The maximum time of the “Long Open Window” is fixed, but it will be terminated as soon as a “Valid WWD triggering” is recognized.
3. The window watchdog will enter now the ”Closed Window”. After receiving this first valid trigger the device will be allowed to move from INIT to NORMAL state or from WAKE to NORMAL state.
4. The “Closed Window” has a fixed duration t_{WD_CW} (can be determined by SPI command). It starts right after the valid trigger signal, that closes the “Open Window” or the “Long Open Window”. During the “Closed Window” no trigger signal should be applied. A transition from low to high at the WDI pin is not detected and will not lead to a trigger event,
5. A valid trigger signal terminates the “Open Window” immediately, thus the time of the “Open Window” is variable and depending on the time the microcontrollers schedules the triggering. This is counted as a “Valid WWD triggering”

Incorrect triggering: No trigger in W1D

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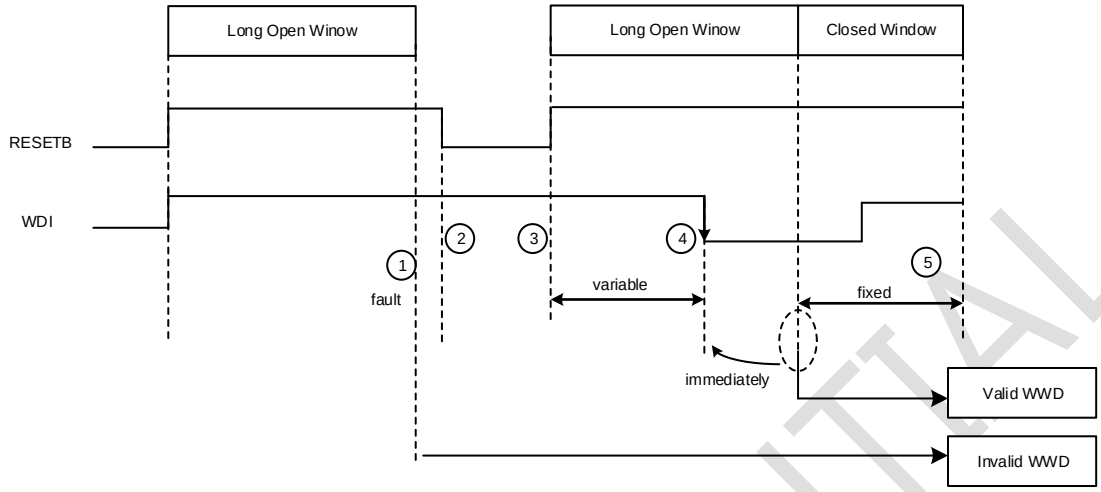


Figure 61. Fault operation: No trigger in Open Window after initialization

1. The initialization timeout and the long open window (LOW) do have the same typ. length. Usually this leads to the initialization timeout finishing at the slightly before or at same time as the LOW, which would skip the interrupt event (1). Even though due to the given accuracy, the missing valid triggering within the “Long Open Window” might lead to an interrupt event after the LOW has ended which is increasing the window watchdog failure counter by two.
2. The INIT state timer expires for the first time. As no valid triggering of the window watchdog was received during INIT state as expected, a so-called “Soft-Reset” will be issued: Pin RESETB goes to zero, but the output voltages of the post regulators remain on.
Additional information: In case the window watchdog should not be triggered correctly within the next “Long Open Window” of the following INIT phase, a “Hard-Reset” will be issued, which means pin RESETB will go to zero and the output voltages will also be switched off. After a third invalid triggering during INIT phase the device will go into FAILSAFE state.
3. After the so-called “Soft-Reset” pin RESETB turns high again after the power-on reset delay time t_{RD} and the watchdog opens a “Long Open Window” to give the microcontroller the chance to trigger and synchronize to the watchdog period.
4. A valid triggering terminates the “Long Open Window”, which makes the duration of the “Long Open Window” variable and depending on the triggering. This is counted as a “Valid WWD triggering” and a “Closed Window” is started. The window watchdog failure counter will be decremented by one without an interrupt issued.
5. The following “Closed Window” lasts for the time t_{WD_CW}. Triggering within this time will be considered as an ”Invalid WWD triggering”.

Incorrect triggering: No trigger in open window

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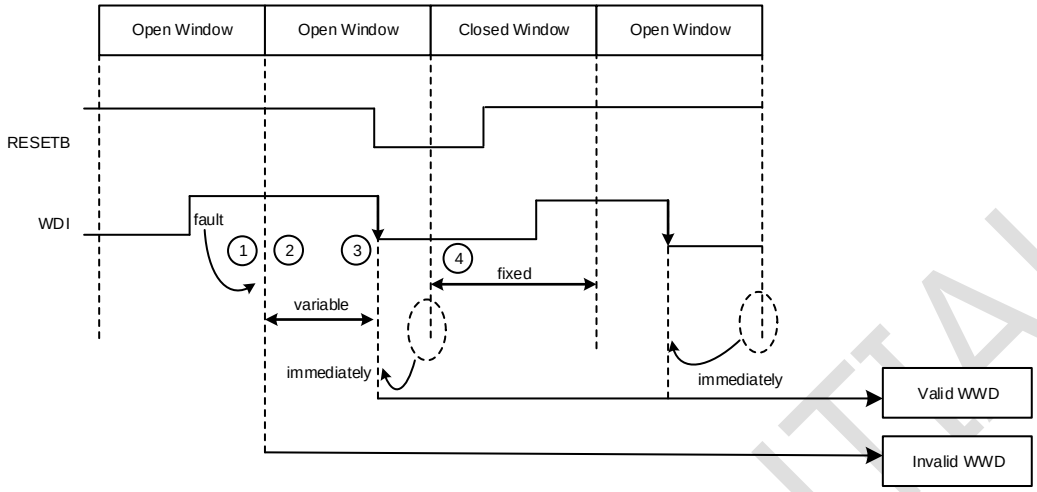


Figure 62. Fault operation: No trigger in Open Window in steady state

1. A missing valid triggering within the “Open Window” leads after the window has ended to an “Invalid WWD triggering”. This event is indicated by an interrupt, the window watchdog failure counter increases by two.
2. Having detected an “Invalid WWD triggering” the watchdog will start a new “Open Window” with duration t_{WD_OW} to give the microcontroller the chance to trigger and synchronize to the watchdog period.
3. A valid triggering terminates the “Open Window”, which makes the duration of the “Open Window” variable and depending on the triggering. This is counted as a “Valid WWD triggering” and a “Closed Window” is started.
The window watchdog failure counter will be decremented by one without an interrupt issued.
Additional informations: In case of multiple “Invalid WWD triggering” within the “Open Windows”, the window watchdog failure counter would be incremented again by two until it reaches the configured threshold. In this case a reset will be issued.
4. The following “Closed Window” lasts for the time t_{WD_CW}. Triggering within this time will be considered as an ”Invalid WWD triggering”.
The behavior of pin RESETB is depending on the value of ΣWWO. In the example above it was assumed, that the invalid triggering will not lead to exceed the threshold ΣWWO.

Incorrect triggering: False trigger in W1D

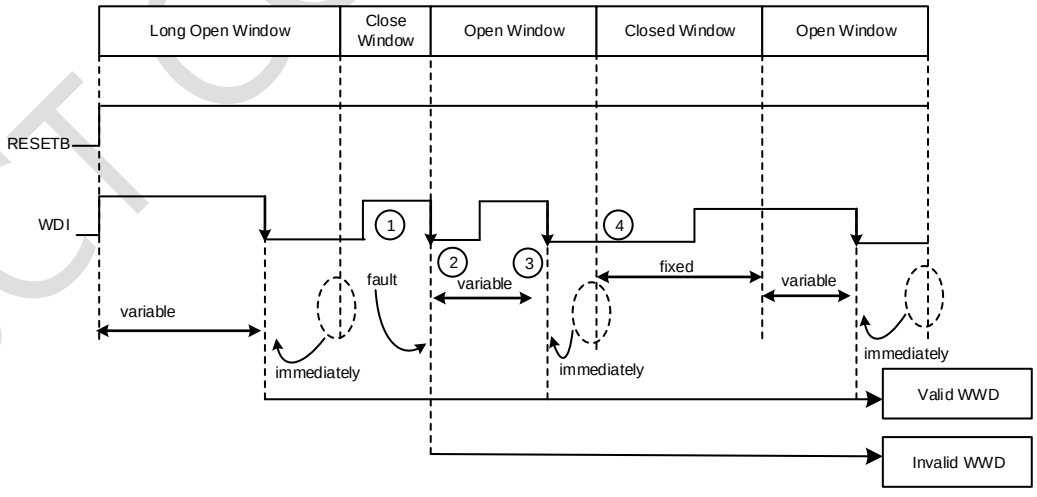


Figure 63. Fault operation: False trigger in Closed Window after initialization

1. A triggering during the “Closed Window” is indicated as “Invalid WWD triggering”. This event is indicated by an

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interrupt and the window watchdog failure counter increases by two.
2. The “Closed Window” will be closed with the “Invalid WWD triggering”. Originally it would last for the time t_{WD_CW}. The false triggering terminates the “Closed Window” and starts an “Open Window” to give the microprocessor the opportunity to synchronize to the window watchdog period.
3. Within this “Open Window” a valid triggering is expected. A valid triggering terminates the “Open Window”, which makes the duration of the “Open Window” variable and depending on the triggering. This is counted as a “Valid WWD triggering” and a “Closed Window” is started. The window watchdog failure counter will be decremented by one without an interrupt issued.
4. The following “Closed Window” lasts for the time t_{WD_CW}. Triggering within this time will be considered as an ”Invalid WWD triggering”.
The behavior of pin RESETB is depending on the value of ∑WWO. In the example above it was assumed, that the invalid triggering will not lead to exceed the threshold ∑WWO.

Incorrect triggering: False trigger in close window

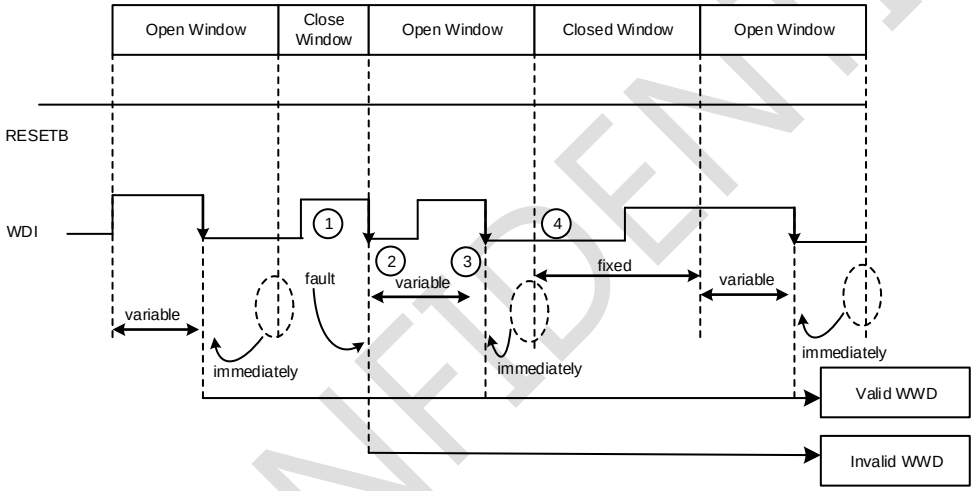


Figure 64. Fault operation: False trigger in Closed Window

1. A triggering during the “Closed Window” is indicated as “Invalid WWD triggering”. This event is indicated by an interrupt and the window watchdog failure counter increases by two.
2. The “Closed Window” will be closed with the “Invalid WWD triggering”. Originally it would last for the time t_{WD_CW}. The false triggering terminates the “Closed Window” and starts an “Open Window” to give the microprocessor the opportunity to synchronize to the window watchdog period.
3. Within this “Open Window” a valid triggering is expected. A valid triggering terminates the “Open Window”, which makes the duration of the “Open Window” variable and depending on the triggering. This is counted as a “Valid WWD triggering” and a “Closed Window” is started. The window watchdog failure counter will be decremented by one without an interrupt issued.
4. The following “Closed Window” lasts for the time t_{WD_CW}. Triggering within this time will be considered as an “Invalid WWD triggering”.
The behavior of pin RESETB is depending on the value of ∑WWO. In the example above it was assumed, that the invalid triggering will not lead to exceed the threshold ∑WWO.

11.3 Functional Watchdog

11.3.1 Operation of FWD

Principle of Operation

A functional or question/answer watchdog is integrated in the SCT61490S to monitor the microcontroller. In a steady state a question is generated (taken out of table), in parallel the so called heartbeat counter starts counting from zero. The heartbeat counter counts up, until the heartbeat period has ended. The duration of the heartbeat period

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is set to a default value, but can be adjusted via SPI command. The question consists of 4 bits, the expected answer consists of 4 responses of 8 bits each. The four responses shall be sent before the heartbeat period has ended. The last response shall be written to the synchronized response register to reset the heartbeat counter.

Initialization

The functional watchdog is off per default when the device is powered up for the first time. It can be enabled by SPI writing to **WDCFG0**.**FWDEN**.

Configuration

The functional watchdog can be configured in INIT, NORMAL and WAKE state. “Configured” means:

• Modify the length of the heartbeat period by SPI command, depending on the needs of the application. (combination of cycle time **WDCYC** and number of cycles for heartbeat **WDHBTP**)

• The threshold for the functional watchdog failure counter overflow can defined by SPI The heartbeat period is based on the cycle time t_{CYCLE}.

Normal Operation

The question is taken out of the below table, the correct responses are listed in the same row. The sequence of responses must be kept and can be derived from the response counter **FWDSTAT0**.**FWDRSPC** before sending the response.

The response to the actual question defined in the table shall be composed by four subsequent response bytes. A correct response to the given question in **FWDSTAT0**.**FWDQUEST** register shall be done in the following way.

• The first three responses shall be written into **FWDRSP**

• The last response should be written into **FWDRSPSYNC** to reset the heartbeat timer

All four responses must be written before the heartbeat period expires.

If the complete response (32 bits) is correct and if the last response byte was sent with synchronized respond, the heartbeat counter will be reset and set to zero. If the complete answer (all four responses - 32 bits) is correct, it is regarded as “Valid FWD triggering”, the functional watchdog error counter ΣFWO is decremented by 1. If the last response was sent with synchronized response, the heartbeat counter will be reset, but if the answer is wrong, this is regarded as “Invalid FWD triggering” and the functional watchdog error counter ΣFWO is incremented by 2.

An overflow of the functional watchdog error counter ΣFWO will trigger a “Move to INIT” event, reset the heartbeat counter and set the functional watchdog error counter ΣFWO to zero.

Table 10 Functional watchdog response definition

QUESTION	RESP3	RESP2	RESP1	RESP0
0	FF	0F	F0	00
1	B0	40	BF	4F
2	E9	19	E6	16
3	A6	56	A9	59
4	75	85	7A	8A
5	3A	CA	35	C5
6	63	93	6C	9C
7	2C	DC	23	D3
8	D2	22	DD	2D
9	9D	6D	92	62
A	C4	34	CB	3B
B	8B	7B	84	74
C	58	A8	57	A7
D	17	E7	18	E8
E	4E	BE	41	B1
F	01	F1	0E	FE

Functional watchdog output FWO

The functional watchdog output FWO is an internal signal: It is connected to the FWD failure counter. The value of the functional watchdog FWO output is either “Valid FWD triggering” or “Invalid FWD Triggering”.

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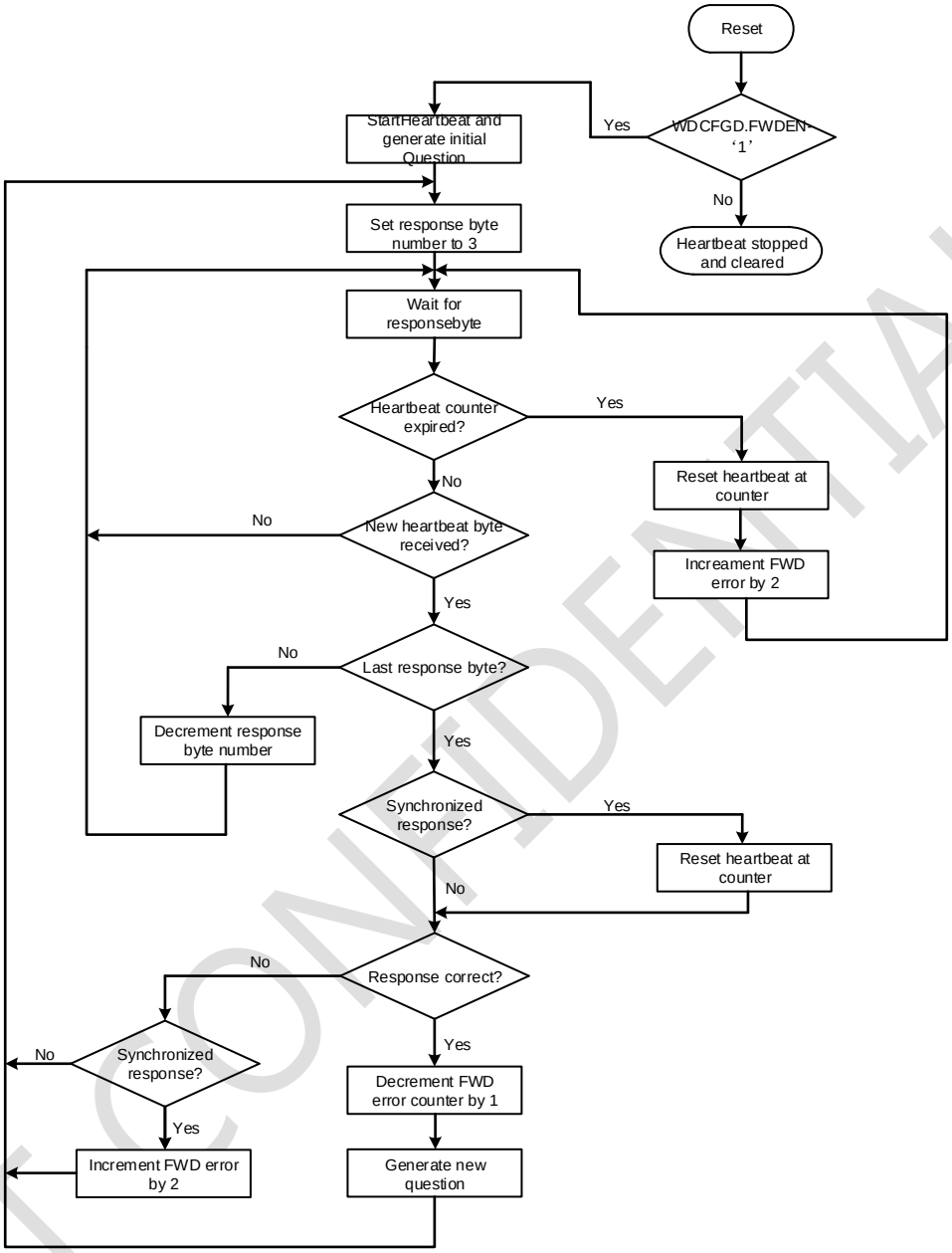


Figure 65. Functional watchdog flowchart diagram

11.3.2 Timing Diagrams

Correct triggering

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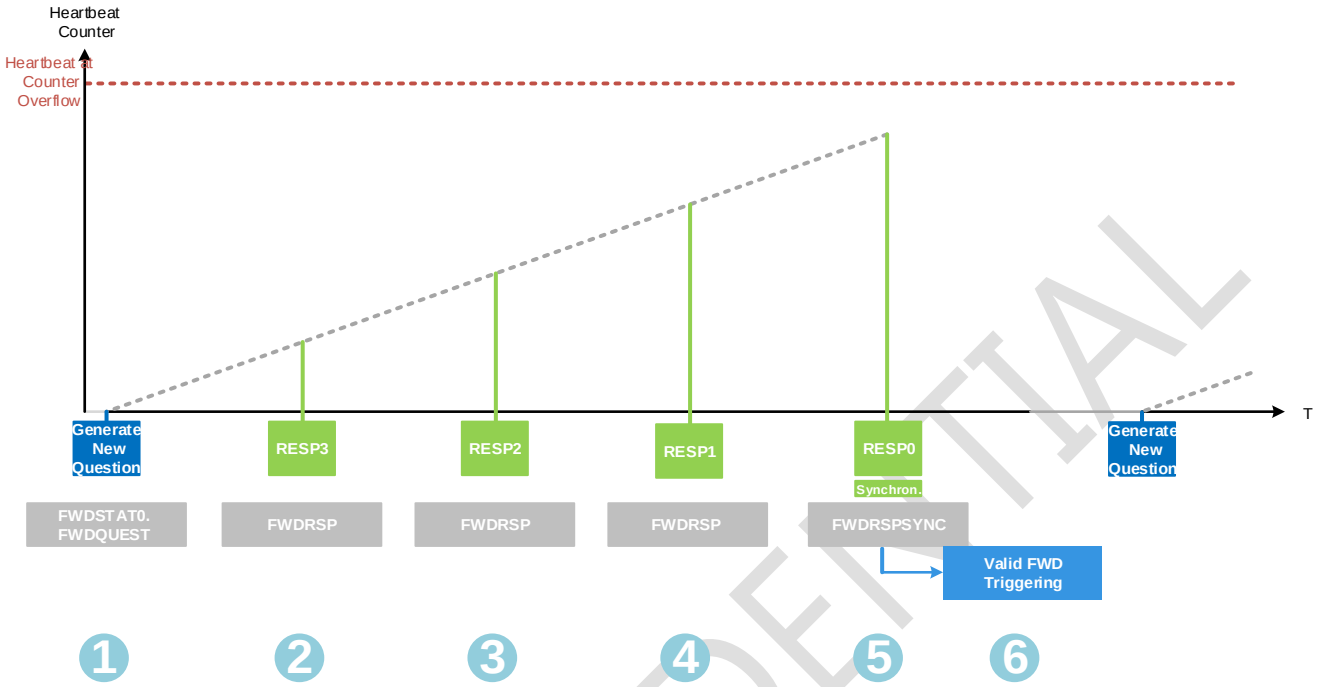


Figure 66. Normal operation: Correct triggering

1. A new question is generated, in parallel the heartbeat counter starts counting up (It is assumed, that a “Valid FWD triggering” has happened before).
2. A correct response is received (RESP3)
3. A correct response is received (RESP2)
4. A correct response is received (RESP1)
5. A correct synchronized response is received (RESP0). All responses are correct, the sequence of responses is correct and the last synchronized response was received before the heartbeat counter overflowed. The heartbeat counter will be reset (set to zero). This is regarded as “Valid FWD triggering”, the functional watchdog error counter ΣFWO is decremented by 1 (if the functional watchdog error counter value is higher than zero).
6. A new question is generated, in parallel the heartbeat counter starts counting up

Incorrect triggering: Synchronization is missing

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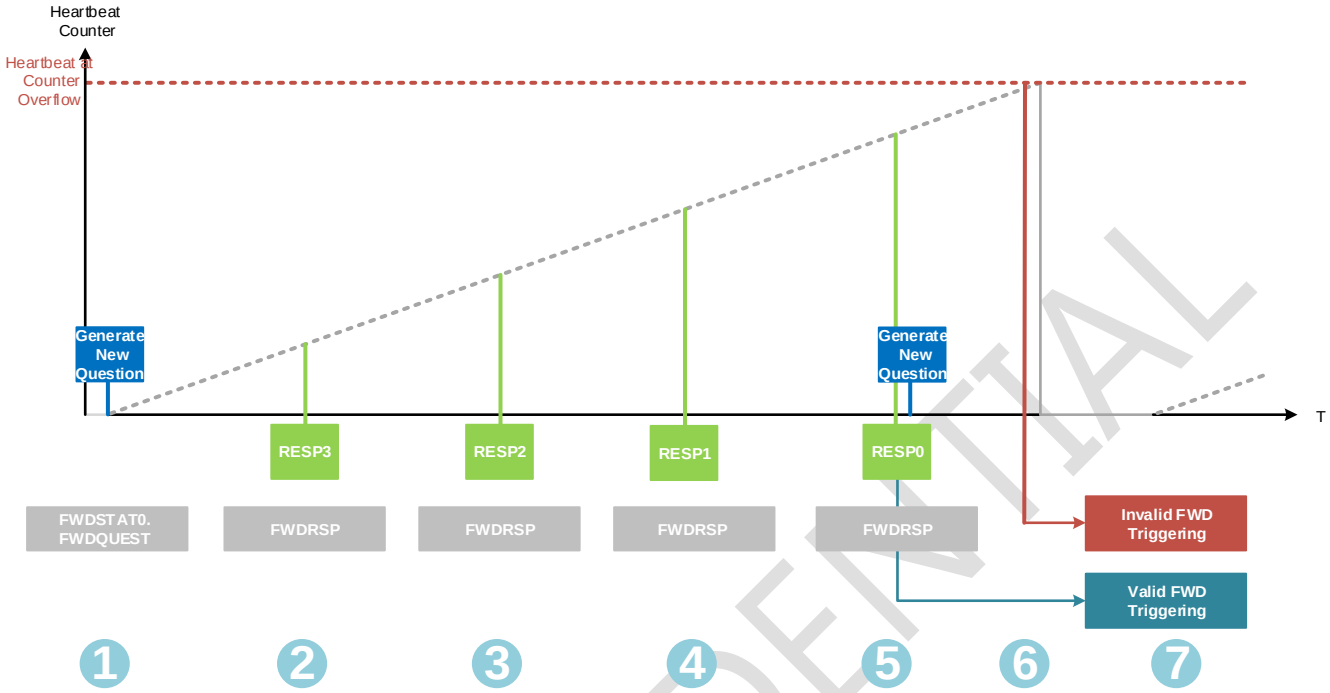


Figure 67. Fault operation: Synchronization is missing

1. A new question is generated, in parallel the heartbeat counter starts counting up (It is assumed, that a “Valid FWD triggering” has happened before).
2. A correct response is received (RESP3)
3. A correct response is received (RESP2)
4. A correct response is received (RESP1)
5. A correct response is received (RESP0), but not synchronized (written in wrong register). So far, all responses are correct, the sequence of responses is correct and the last not synchronized response was received before the heartbeat counter overflow occurred. The heartbeat counter will not be reset and continue to count. This is regarded as “Valid FWD triggering”, the functional watchdog error counter ∑FWO is decremented by 1 (if the functional watchdog error counter value is higher than zero). A new question is generated.
6. The heartbeat counter is still counting up, waiting for the answer on the new question. Later in time the heartbeat counter will expire and an overflow occurs. This is regarded as “Invalid FWD triggering”. The functional watchdog error counter ∑FWO is incremented by 2. The heartbeat counter is reset.
7. The heartbeat counter starts counting up. No new question is generated.

Incorrect triggering: Answer is wrong

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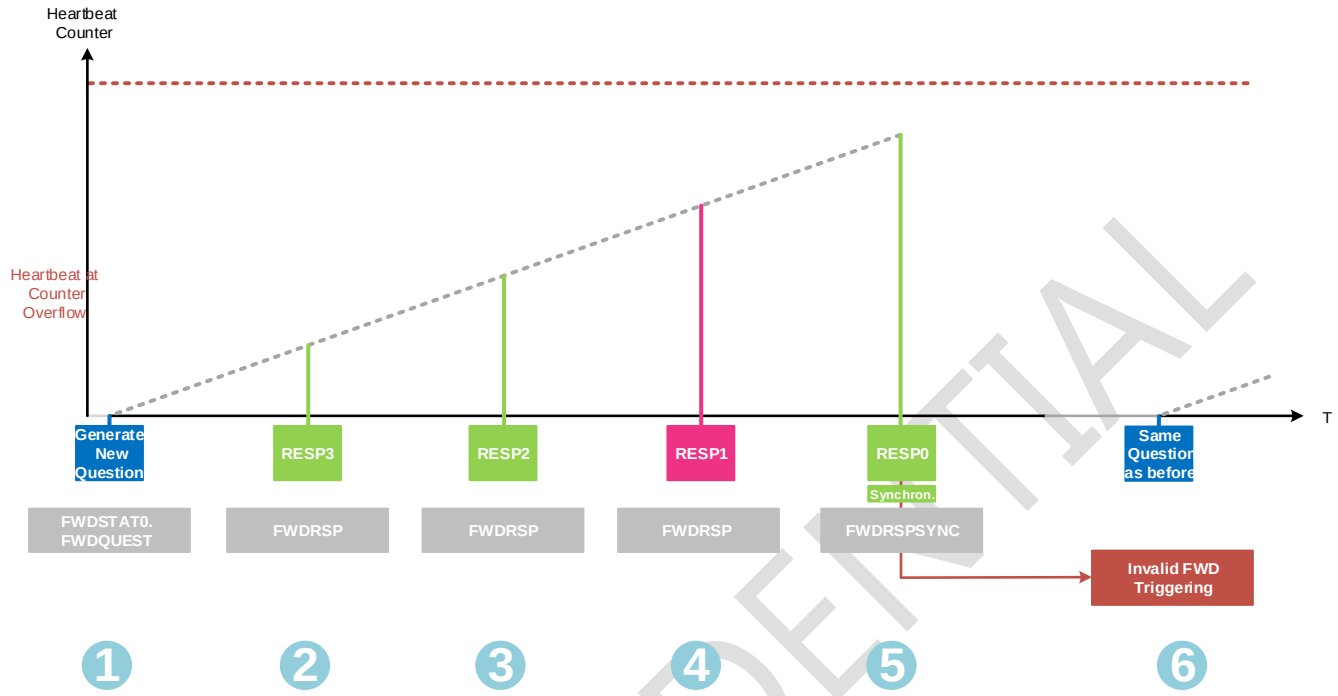


Figure 68. Fault operation: Answer is wrong

1. A new question is generated, in parallel the heartbeat counter starts counting up (It is assumed, that a “Valid FWD triggering” has happened before)
2. A correct response is received (RESP3)
3. A correct response is received (RESP2)
4. An incorrect response is received (RESP1)
5. A correct response is received (RESP0). The heartbeat counter will be reset (set to zero). The complete answer is not correct. This is regarded as “Invalid FWD triggering”. The functional watchdog error counter ΣFWO is incremented by 2. The heartbeat counter is reset.
6. No new question is generated, but the heartbeat counter starts counting up.

Note: If i.e. RESP2 and RESP1 would be mixed, than both responses would be regarded as incorrect – the responses have to be sent in correct order.

Incorrect triggering: Missing response

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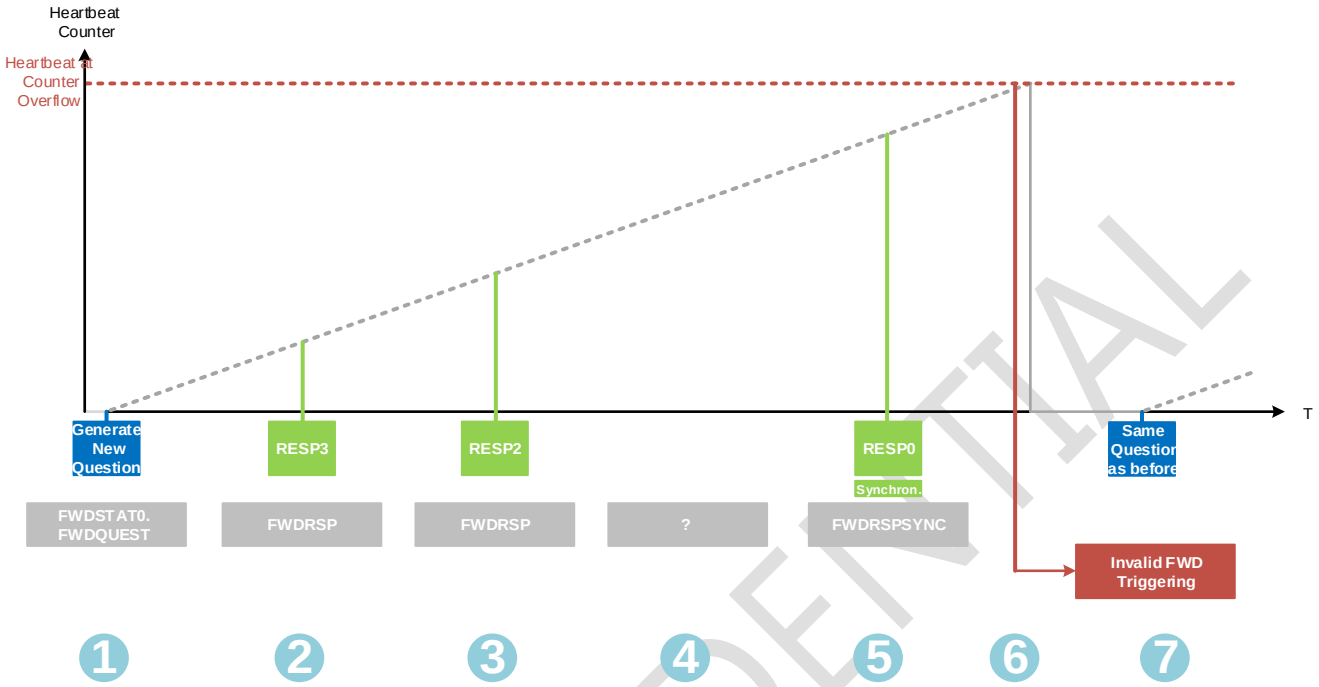


Figure 69. Fault operation: Answer is not complete

1. A new question is generated, in parallel the heartbeat counter starts counting up (It is assumed, that a “Valid FWD triggering” has happened before).
2. A correct response is received (RESP3)
3. A correct response is received (RESP2)
4. A response is missing (RESP1)
5. A correct response is received (RESP0). Therefore, the last response is not the last response but the second last due to the missing response (in this example RESP1). The functional watchdog will wait for all four responses to be written, while the heartbeat counter keeps on counting. There is no fixed time for all four responses, but they must be sent in correct order before the heartbeat counter expires.
6. The complete answer is not correct due to missing response RESP1. Although the last response is synchronized, the heartbeat counter will not be reset and continue counting up until an overflow occurs. This is regarded as “Invalid FWD triggering”. The functional watchdog error counter ΣFWO is incremented by 2. The heartbeat counter is reset.
7. No new question is generated and the heartbeat counter starts counting up.

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12 Typical Application

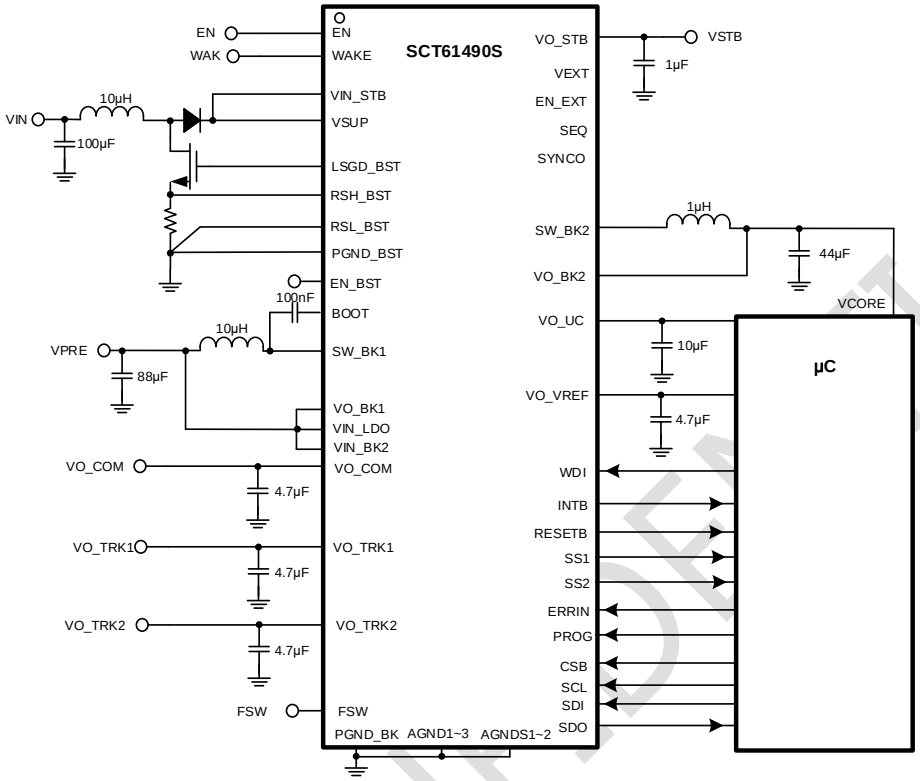


Figure 70. Application Schematics, 3V to 40V Input

Design Parameters	Example Value
Input Voltage	12V Nominal 3V to 40V
Output Voltage	VO_BK1: 5.8V VO_BK2: 1.2V VO_UC: 5V VO_STB: 5V VO_COM: 5V VO_VREF: 5V VO_TRK1/2: 5V
Maximum Output Current	VO_BK1: 4A VO_BK2: 5A VO_UC: 800mA VO_STB: 20mA VO_COM: 600mA VO_VREF: 200mA VO_TRK1/2: 200mA
Switching Frequency	400kHz/2.2MHz (selectable)

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The SCT61490S is featured with minimized external components and any feedback divider or configuration resistor could be saved. For typical application, the recommended inductance and capacitance for each power rail are listed in Table 11. Higher inductance and capacitance for lower output ripple are also acceptable.

Table 11. Recommended BOM for Typical Application

Power Rail	Switching Frequency	Inductor	Output Capacitor
VO_BK1: 5.8V	400kHz	10~22μH	68~100μF
VO_BK1: 5.8V	2.2MHz	4.7~10μH	10~47μF
VO_BK2: 1.2V	2.2MHz	1μH	44μF
VO_UC: 5V	-	-	2.2~47μF
VO_STB: 5V	-	-	1~10μF
VO_COM: 5V	-	-	1~47μF
VO_VREF: 5V	-	-	1~10μF
VO_TRK1/2: 5V	-	-	1~10μF

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12.1 Application Waveforms

V_{IN} = 12V, V_{BK1} = 5.8V, V_{BK2} = 1.2V, V_{UC} = 5V, V_{STB} = 5V, V_{COM} = 5V, V_{VREF} = 5V, V_{TRK12} = 5V, L1 = 10μH, L2 = 1μH, T_A = 25°C, unless otherwise noted.

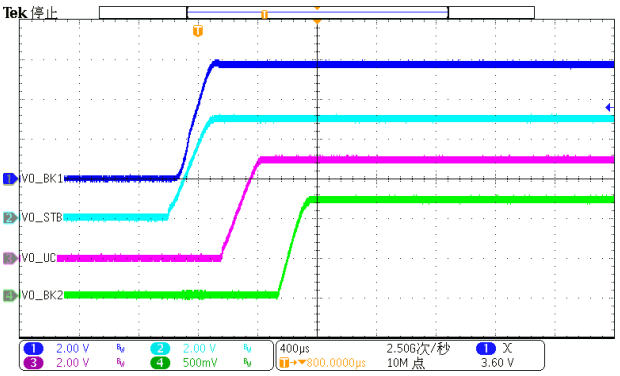


Figure 71. Power On Sequence I

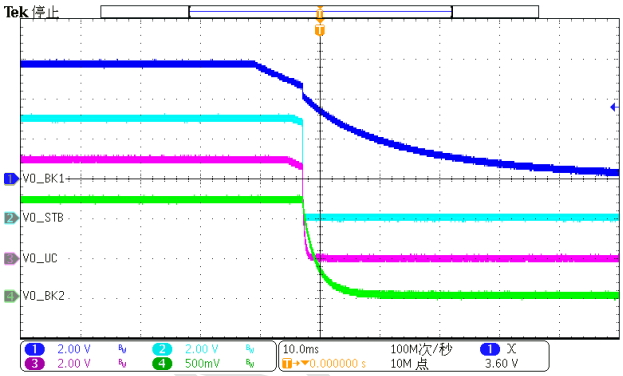


Figure 72. Power Off Sequence I

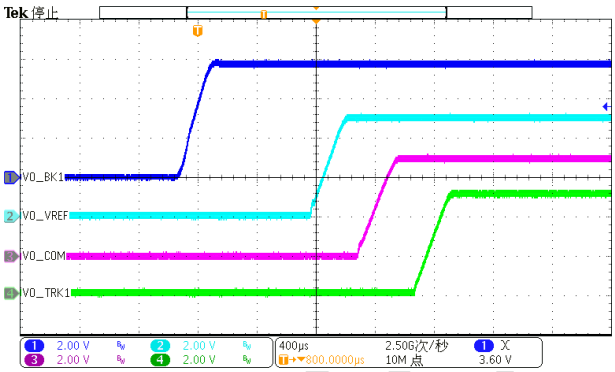


Figure 73. Power On Sequence II

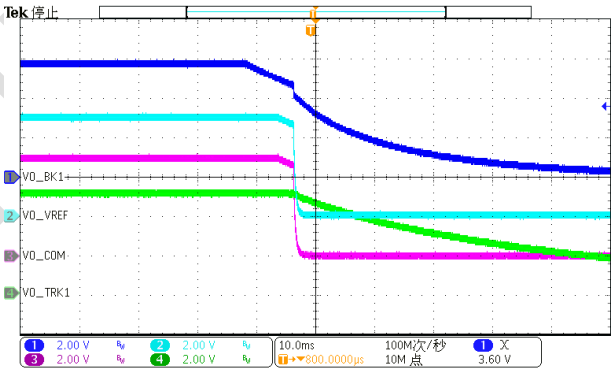


Figure 74. Power Off Sequence II

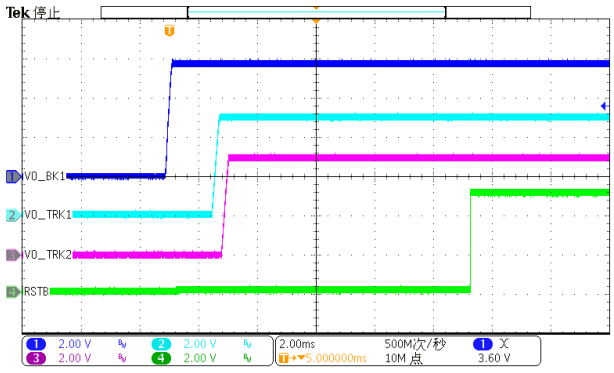


Figure 75. Power On Sequence III

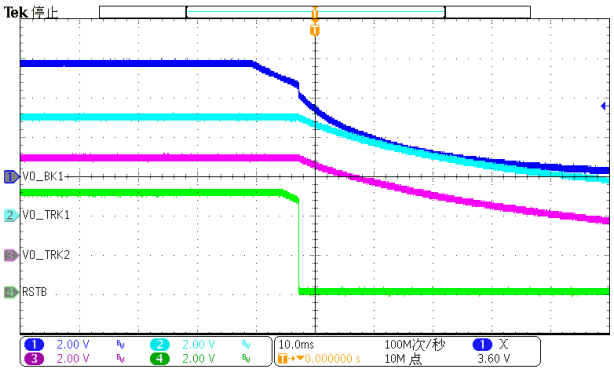


Figure 76. Power Off Sequence III

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Application Waveforms (continued)

V_{IN} = 12V, V_{BK1} = 5.8V, V_{BK2} = 1.2V, V_{UC} = 5V, V_{STB} = 5V, V_{COM} = 5V, V_{VREF} = 5V, V_{TRK12} = 5V, L1 = 10μH, L2 = 1μH, T_A = 25°C, unless otherwise noted.

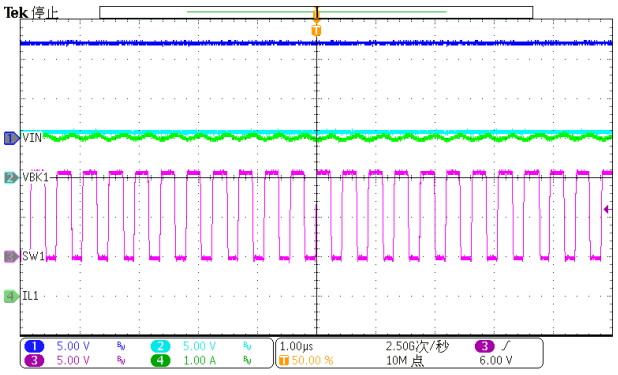


Figure 77. Buck1 Steady State, Load=4A

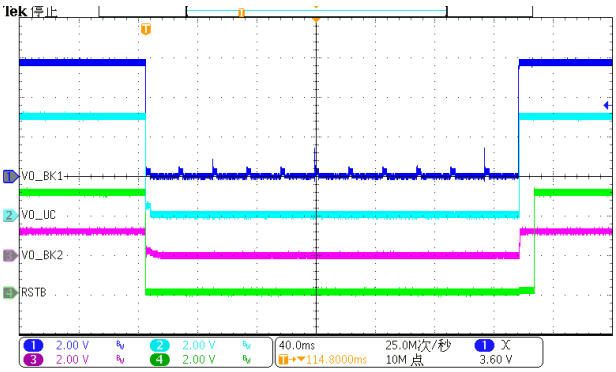


Figure 78. Buck1 Short-circuit and Recovery

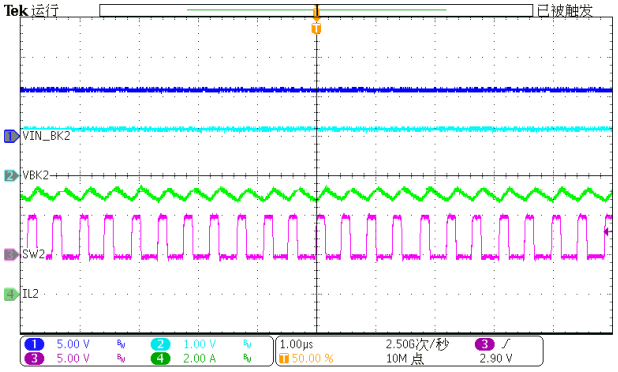


Figure 79. Buck2 Steady State, Load=5A

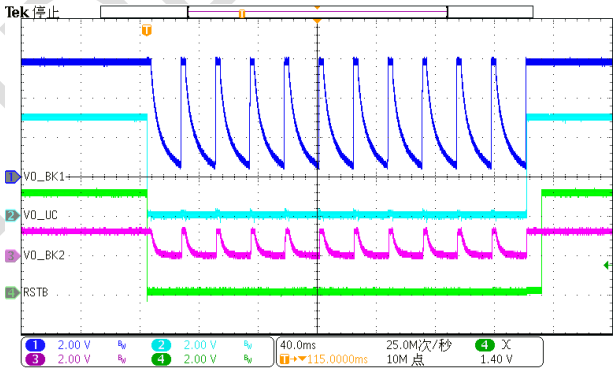


Figure 80. VO_UC Short-circuit and Recovery

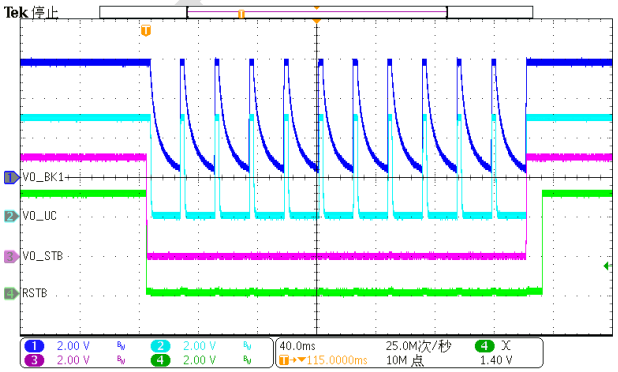


Figure 81. VO_ STB Short-circuit and Recovery

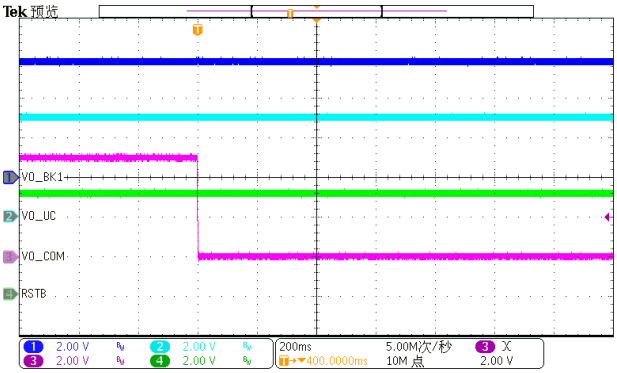


Figure 82. VO_COM Short-circuit

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12.2 Layout Guideline

Proper PCB layout is a critical for device's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The rule of thumb is to make ground trace lowest impedance and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over-heat area.
2. Place a low ESR ceramic capacitor as close to VIN, VIN_BK2 and VIN_LDO pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impedance of grounding.
4. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias.
5. Output inductor should be placed close to the SW pin. The switching area of the PCB conductor minimized to prevent excessive capacitive coupling.
6. Connect AGND to PGND plane at a single point.

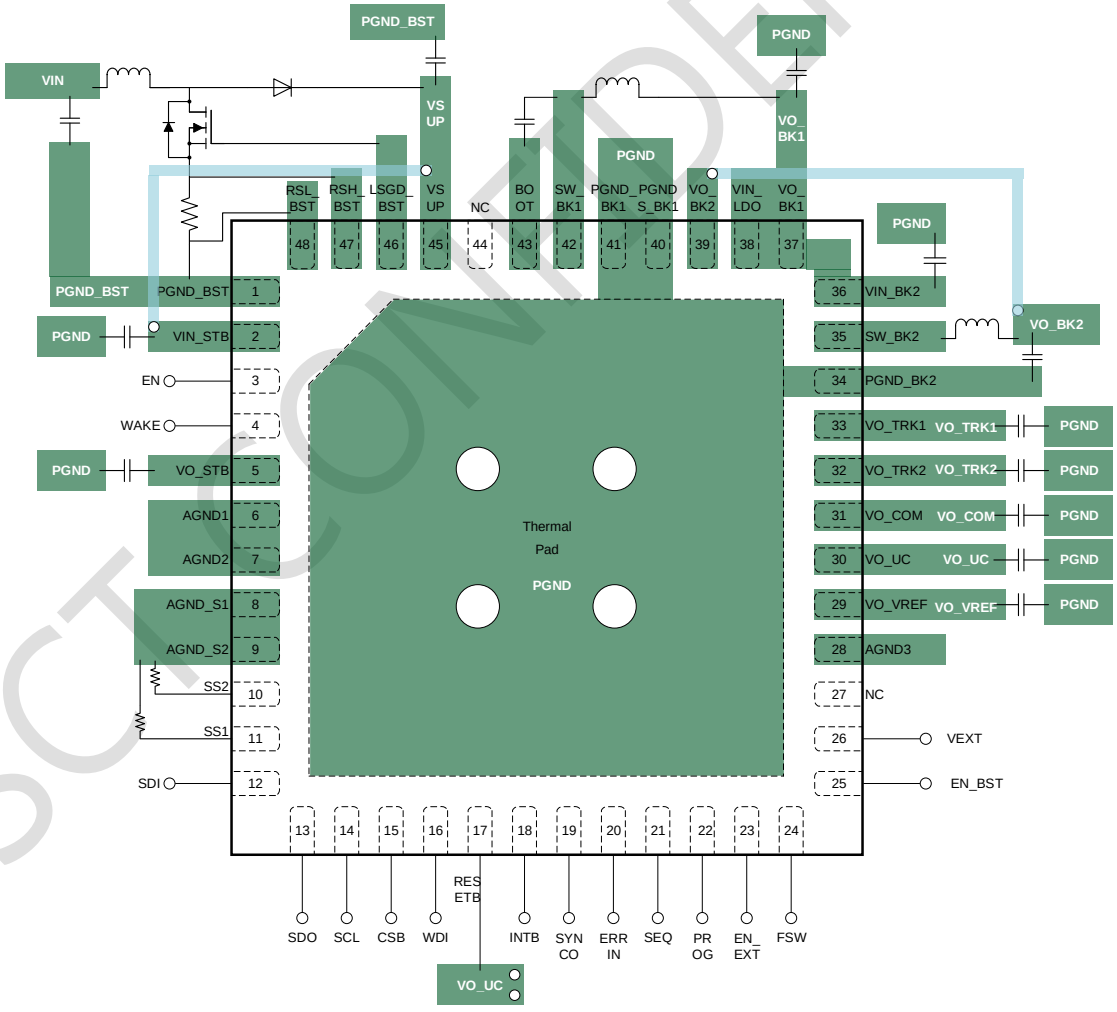


Figure 83. PCB Layout Example

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13 Register Description

13.1 Register Type Abbreviations

Abbreviations	Description
R0	Reset type 0. Registers that are being reset only in case of a POR.
R1	Reset type 1. Registers that are being reset only in case of STANDBY and a POR.
R2	Reset type 2. Registers that are being reset only in case of FAILSAFE, STANDBY and a POR.
R3	Reset type 3. Registers that are being reset in case of “Move to INIT” event, FAILSAFE, STANDBY and a POR.
R	Bits that are readable only (read)
RW	Bits that are readable and writable (read-write)
RWP	Bits that are readable and writable but protected by register PROTCFG (read-write-protected)
RW1C	Bits that are readable and to clear the bit you have to write a 1 to it. (read-write-1-to-clear). Flag-bits are updated based on the occurred condition.
RWHC	Bits that are readable and writable after writing the operation is triggered, once this is done successfully the bit is cleared by hardware. (read-write-hardware-cleared)
RWHU	Bits that are readable and writable, after the operation the bit is updated by hardware. (read-write- hardware-updated)

13.2 Register Mapping

ADDRESS	REGISTER	DEFAULT VALUE	RESET TYPE
0x00	DEVCFG0	08h	R2
0x01	DEVCFG1	06h	R0
0x02	DEVCFG2	00h	R2
0x03	PROTCFG	00h	R2
0x04	SYSPCFG0	01h	R1
0x05	SYSPCFG1	08h	R2
0x06	WDCFG0	9Bh	R2
0x07	WDCFG1	09h	R2
0x08	FWDCFG	0Bh	R2

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0x09	WWDCFG0	06h	R2
0x0A	WWDCFG1	0Bh	R2
0x0B	RSYSPCFG0	01h	R0
0x0C	RSYSPCFG1	00h	[7:5]: R1 [4:0]: R3
0x0D	RWDCFG0	9Bh	R3
0x0E	RWDCFG1	09h	R3
0x0F	RFWDCFG	0Bh	R3
0x10	RWWDCFG0	06h	R3
0x11	RWWDCFG1	09h	R3
0x12	WKTIMCFG0	00h	R2
0x13	WKTIMCFG1	00h	R2
0x14	WKTIMCFG2	00h	R2
0x15	DEVCTRL	00h	R2
0x16	DEVCTRLN	00h	R2
0x17	WWDSCMD	00h	R2
0x18	FWDRSP	00h	R2
0x19	FWDRSPSYNC	00h	R2
0x1A	SYSFAIL	00h	R1
0x1B	INITERR	00h	R2
0x1C	IF	00h	R2
0x1D	SYSSF	00h	R2
0x1E	WKSF	00h	R2
0x1F	SPISF	00h	R2
0x20	MONSF0	00h	R1
0x21	MONSF1	00h	R1
0x22	MONSF2	00h	R2
0x23	MONSF3	00h	R1
0x24	OTFAIL	00h	R1
0x25	OTWRNSF	00h	R2

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0x26	VMONSTAT	00h	R2
0x27	DEVSTAT	00h	R2
0x28	PROTSTAT	01h	R1
0x29	WWDSTAT	00h	R3
0x2A	FWDSTAT0	30h	R3
0x2B	FWDSTAT1	00h	R3
0x2C	ABIST_CTRL0	00h	[7:4]: R1 [3:0]: R2
0x2D	ABIST_CTRL1	00h	R2
0x2E	ABIST_SELECT0	00h	R2
0x2F	ABIST_SELECT1	00h	R2
0x30	ABIST_SELECT2	00h	R2
0x31	BCK_FREQ_CHANGE	00h	R2
0x32	BCK_FRE_SPREAD	00h	R2
0x33	BCK_MAIN_CTRL	00h	R2
0x34	BK2DVS	-	R0
0x35	BK2DVSN	-	R0
0x3A	FWD_KEY	00h	R2
0x3B	MONSF4	00h	R2
0x3C	MCSMON	00h	R2
0x3D	CHIPCODE	-	R0

13.3 Detailed Description

DEVCFG0 [7:0]				
ADDRESS: 0x00				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	WKTIMEN	RW	Wake timer enable	0 = Wake timer disabled 1 = Wake timer enabled in SLEEP or STANDBY state
[6]	WKTIMCYC	RW	Wake timer cycle period	when select short config: 0 = 8us 1 = 8.192ms when select long config: 0 = 1ms

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				1 = 1s
[5]	WKTIMCYC_SEL	RW	Wake timer cycle period pre-scaler Wake timer cycle period selection for long timer	0 = Short config 1 = Long config
[4]	RSV	R	Reserved	
[3:0]	TRDEL	RW	Transition delay into low power states. For STANDBY and SLEEP transition. Defined as a step of 100 µs.	0000 = 100µs; 0001 = 200µs; 0010 = 300µs; 0011 = 400µs; 0100 = 500µs; 0101 = 600µs; 0110 = 700µs; 0111 = 800µs; 1000 = 900µs; 1001 = 1000µs; 1010 = 1100µs; 1011 = 1200µs; 1100 = 1300µs; 1101 = 1400µs; 1110 = 1500µs; 1111 = 1600µs

DEVCFG1 [7:0]

ADDRESS: 0x01

BITS	FIELD	TYPE	DESCRIPTION	DECODE
[7:4]	RSV	R	Reserved	
[3:0]	RESDEL	RW	Reset release delay time	0000 = 200µs; 0001 = 400µs; 0010 = 800µs; 0011 = 1ms; 0100 = 2ms; 0101 = 4ms; 0110 = 10ms; 0111 = 15ms; 1000 = 30ms; 1001 = 60ms; 1010 = 100ms; others = 10ms.

DEVCFG2 [7:0]

ADDRESS: 0x02

BITS	FIELD	TYPE	DESCRIPTION	DECODE
[7]	EVCEN	R	External core supply enable status	0 = External core supply disabled 1 = External core supply enabled
[6]	EN_BST	R	Step-up converter enable status	0 = Disabled 1 = Enabled
[5]	FRE	R	Step-down converter frequency selection status	0 = Step-down converter runs on low frequency range 1 = Step-down converter runs on high frequency range
[4]	CMONEN	RW	LDO_UC current monitor enable for transition to a low power state For STANDBY and SLEEP transition. The setting is overwritten in SLEEP as current monitoring is always enabled.	0 = Disabled 1 = Enabled
[3:2]	CTHR	RW	LDO_UC current monitoring threshold value	00 = 10mA; 01 = 30mA; 10 = 60mA; 11 = 100mA
[1]	ESYNPHA	RW	External synchronization output phase	0 = No phase shift 1 = 180 phase shift
[0]	ESYNEN	RW	Synchronization output for external switchmode regulator enable	0 = Disabled 1 = Enabled

PROTCFG [7:0]

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ADDRESS: 0x03				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:0]	CTHR	RW	Protection key Protection key register to request write access to protected registers. Unlock: write 32-bit sequence of 4 consecutive bytes (1: 0xAB 2:0xEF 3:0x56 4:0x12) to unlock access to protected registers. Lock: write 32-bit sequence of 4 consecutive bytes (1: 0xDF 2:0x34 3:0xBE 4:0xCA) to lock access to protected registers. All configured values are applied to SSC and WD module after the lock.	ABh = Key 1 to unlock protected registers. EFh = Key 2 to unlock protected registers. 56h = Key 3 to unlock protected registers. 12h = Key 4 to unlock protected registers. DFh = Key 1 to lock protected registers. 34h = Key 2 to lock protected registers. BEh = Key 3 to lock protected registers. CAh = Key 4 to lock protected registers.

SYSPCFG0 [7:0]				
ADDRESS: 0x04				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:1]	RSV	R	Reserved, not used bits shall be written as 0 and will always return 1 upon read	
[0]	STBYEN	RW	Request standby regulator VO_STB enable	0 = Disabled 1 = Enabled

SYSPCFG1 [7:0]				
ADDRESS: 0x05				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:5]	SS2DEL	RWP	Request safe state 2 delay Applied for transitions from NORMAL to INIT, WAKE and SLEEP state.	000 = no delay; 001 = 10ms; 010 = 50ms; 011 = 100ms; 100 = 250ms; 101 = 1250ms; 110 = 2500ms
[4]	ERRSLPEN	RWP	Request ERR pin monitor functionality enable while the system is in SLEEP	0 = ERRIN pin monitor is disabled in SLEEP 1 = ERRIN pin monitor can be active in SLEEP depending on ERREN bit value.
[3]	ERREN	RWP	Request ERRIN pin monitor enable	0 = Disabled 1 = Enabled
[2]	ERRRECEN	RWP	Request ERRIN pin monitor recovery enable	0 = Disabled 1 = Enabled
[1:0]	ERRREC	RWP	Request ERRIN pin monitor recovery time	00 = 1ms; 01 = 2.5ms; 10 = 5ms; 11 = 10ms

WDCFG0 [7:0]				
ADDRESS: 0x06				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:4]	WWDETHR	RWP	Request window watchdog error threshold WWD error threshold to generate reset and enter into INIT state.	WWD error thrshold = WWDETHR[3:0] * 1 times

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[3]	WWDE	RWP	Request window watchdog enable	0 = Disabled 1 = Enabled
[2]	FWDEN	RWP	Request functional watchdog enable	0 = Disabled 1 = Enabled
[1]	WWDTSEL	RWP	Request window watchdog trigger selection This is ignored when window watchdog is disabled.	0 = External WDI input used as a WWD trigger 1 = WWD is triggered by SPI write to WWDSCMD register
[0]	WDCYC	RWP	Request watchdog cycle time	0 = 0.1 ms tick period 1 = 1 ms tick period

WDCFG1 [7:0]				
ADDRESS: 0x07				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	RSV	R	Reserved, not used bits shall be written as 0 and will always return 1 upon read	
[6]	WDCYCDIV	RWP	Request enable of additional divider by 10 for watchdog cycle time (WDCYC) configuration, Data bits are sent inverted to SPI upon read access.	0 = Disabled 1 = Enabled, additional divider by 10 for watchdog cycle time (WDCYC) configuration is enabled
[5]	RSV	R	Reserved, not used bits shall be written as 0 and will always return 1 upon read	
[4]	WDSLPEN	RWP	Request watchdog functionality enable while the device is in SLEEP	0 = Disabled 1 = Enabled, the WD will work based on individual configuration (WWDEN & FWDEN) settings while the system is in SLEEP mode
[3:0]	FWDETHR	RWP	Request functional watchdog error threshold FWD error threshold to generate reset and enter into INIT state.	FWD error thrshold = FWDETHR[3:0] * 1 times

FWDCFG [7:0]				
ADDRESS: 0x08				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:5]	RSV	R	Reserved, not used bits shall be written as 0 and will always return 1 upon read	
[4:0]	WDHBTP	RWP	Request functional watchdog heartbeat timer period Defined as a multiple of 50 watchdog cycles (RWDCFG0.WDCYC).	Heartbeat timer period = (WDHBTP[4:0]+1)* 50 WD cycles

WWDCFG0 [7:0]				
ADDRESS: 0x09				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**

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[7:5]	RSV	R	Reserved, not used bits shall be written as 0 and will always return 1 upon read	
[4:0]	CW	RWP	Request window watchdog closed window time Defined as a multiple of 50 watchdog cycles (RWDCFG0.WDCYC).	WWD close window= (CW[4:0]+1)* 50 WD cycles

WWDCFG1 [7:0]				
ADDRESS: 0x0A				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:5]	RSV	R	Reserved, not used bits shall be written as 0 and will always return 1 upon read	
[4:0]	OW	RWP	Request window watchdog open window time Defined as a multiple of 50 watchdog cycles (RWDCFG0.WDCYC).	WWD open window= (OW[4:0]+1)* 50 WD cycles

RSYSPCFG0 [7:0]				
ADDRESS: 0x0B				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:1]	RSV	R	Reserved	
[0]	STBYEN	R	Standby regulator VO_STB enable status Current configuration of standby regulator VO_STB enable.	0 = Disabled 1 = Enabled

RSYSPCFG1 [7:0]				
ADDRESS: 0x0C				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:5]	SS2DEL	R	Safe state 2 delay status Current configuration of safe state 2 delay applied for transitions from NORMAL to INIT, WAKE and SLEEP state. Bits have different reset class than whole register. The Bits are reset according to R1)	000 = no delay; 001 = 10ms; 010 = 50ms; 011 = 100ms; 100 = 250ms; 101 = 1250ms; 110 = 2500ms
[4]	ERRSLPEN	R	ERRIN pin monitor functionality enable status while the device is in SLEEP	0 = ERRIN pin monitor is disabled in SLEEP Disabled 1 = ERRIN pin monitor can be active in SLEEP depending on ERREN bit value
[3]	ERREN	R	ERRIN pin monitor enable status Current configuration of ERR pin monitor enable.	0 = Disabled 1 = Enabled
[2]	ERRRECEN	R	ERRIN pin monitor recovery enable status Current configuration of ERR pin monitor recovery enable.	0 = Disabled 1 = Enabled

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[1:0]	ERRREC	R	Request watchdog cycle time	00 = 1ms; 01 = 2.5ms; 10 = 5ms; 11 = 10ms

RWDCFG0 [7:0]				
ADDRESS: 0x0D				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:4]	WWDETHR	R	Window watchdog error threshold status Current configuration of WWD error threshold to generate reset and enter into INIT state	WWD error thrshold = WWDETHR[3:0] * 1 times
[3]	WWDEN	R	Window watchdog enable status Current configuration of WWD enable.	0 = Disabled 1 = Enabled
[2]	FWDEN	R	ERRIN pin monitor enable status Current configuration of ERR pin monitor enable.	0 = Disabled 1 = Enabled
[1]	WWDTSEL	R	Window watchdog trigger selection status Current configuration of WWD trigger selection. This is ignored when window watchdog is disabled.	0 = External WDI input used as a WWD trigger 1 = WWD is triggered by SPI write to WWDSCMD register
[0]	WDCYC	R	Request watchdog cycle time	0 = 0.1 ms tick period 1 = 1 ms tick period

RWDCFG1 [7:0]				
ADDRESS: 0x0E				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	RSV	R	Reserved, not used bits shall be written as 0 and will always return 1 upon read	
[6]	WDCYCDIV	R	Request enable of additional divider by 10 for watchdog cycle time (WDCYC) configuration, Data bits are sent inverted to SPI upon read access.	0 = Disabled 1 = Enabled, additional divider by 10 for watchdog cycle time (WDCYC) configuration is enabled
[5]	RSV	R	Reserved, not used bits shall be written as 0 and will always return 1 upon read	
[4]	WDSLPEN	R	Request watchdog functionality enable while the device is in SLEEP	0 = Disabled 1 = Enabled, the WD will work based on individual configuration (WWDEN & FWDEN) settings while the system is in SLEEP mode
[3:0]	FWDETHR	R	Request functional watchdog error threshold FWD error threshold to generate reset and enter into INIT state.	FWD error thrshold = FWDETHR[3:0] * 1 times

RFWDCFG [7:0]
ADDRESS: 0x0F

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BITS	FIELD	TYPE	DESCRIPTION	DECODE
[7:5]	RSV	R	Reserved, not used bits shall be written as 0 and will always return 1 upon read	
[4:0]	WDHBTP	R	Request functional watchdog heartbeat timer period Defined as a multiple of 50 watchdog cycles (RWDCFG0.WDCYC).	Heartbeat timer period = (WDHBTP[4:0]+1)* 50 WD cycles

RWWDCFG0 [7:0]				
ADDRESS: 0x10				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:5]	RSV	R	Reserved, not used bits shall be written as 0 and will always return 1 upon read	
[4:0]	CW	R	Request window watchdog closed window time Defined as a multiple of 50 watchdog cycles (RWDCFG0.WDCYC).	WWD close window= (CW[4:0]+1)* 50 WD cycles

RWWDCFG1 [7:0]				
ADDRESS: 0x11				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:5]	RSV	R	Reserved, not used bits shall be written as 0 and will always return 1 upon read	
[4:0]	OW	RWP	Request window watchdog open window time Defined as a multiple of 50 watchdog cycles (RWDCFG0.WDCYC).	WWD open window= (OW[4:0]+1)* 50 WD cycles

WKTIMCFG0 [7:0]				
ADDRESS: 0x12				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:0]	TIMVALL	RW	Wake timer value lower bits Bits (7:0) of wake time defined as a multiple of wake timer cycles (DEVCFG0.WKTIMCYC).	

WKTIMCFG1 [7:0]				
ADDRESS: 0x13				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:0]	TIMVALM	RW	Wake timer value middle bits Bits (15:8) of wake time defined as a multiple of wake timer cycles (DEVCFG0.WKTIMCYC).	
WKTIMCFG2 [7:0]				
ADDRESS: 0x14				

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BITS	FIELD	TYPE	DESCRIPTION	DECODE
[7:0]	TIMVALH	RW	Wake timer value higher bits Bits (23:16) of wake time defined as a multiple of wake timer cycles (DEVCFG0.WKTIMCYC).	

DEVCTRL [7:0]				
ADDRESS: 0x15				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	TRK2EN	RW	Request LDO tracker2 enable	0 = TRK2 will be disabled after valid request 1 = TRK2 will be enabled after valid request
[6]	TRK1EN	RW	Request LDO tracker1 enable	0 = TRK1 will be disabled after valid request 1 = TRK1 will be enabled after valid request
[5]	COMEN	RW	Request communication LDO_COM enable	0 = LDO_COM will be disabled after valid request 1 = LDO_COM will be enabled after valid request
[4]	BK2_EN	RW	Request LV Buck 2 enable	0 = LV Buck 2 will be disabled after valid request 1 = LV Buck 2 will be enabled after valid request
[3]	VREFEN	RW	Request voltage reference LDO_VRF enable	0 = LDO_VRF will be disabled after valid request 1 = LDO_VRF will be enabled after valid request
[2:0]	STATEREQ	RWHC	Request for device state transition Cleared to 000 by the HW after the request is processed. After writing a new state value a user should not change the value before it's cleared by HW.	000 = NONE; 001 = INIT; 010 = NORMAL; 011 = SLEEP; 100 = STANDBY; 101 = WAKE; 110 = RESERVED; 111 = RESERVED

DEVCTRLN [7:0]				
ADDRESS: 0x16				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	TRK2EN	RW	Request LDO tracker2 enable	1 = TRK2 will be disabled after valid request 0 = TRK2 will be enabled after valid request
[6]	TRK1EN	RW	Request LDO tracker1 enable	1 = TRK1 will be disabled after valid request 0 = TRK1 will be enabled after valid request
[5]	COMEN	RW	Request communication LDO_COM enable	1 = LDO_COM will be disabled after valid request 0 = LDO_COM will be enabled after valid request

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[4]	BK2_EN	RW	Request LV Buck 2 enable	1 = LV Buck 2 will be disabled after valid request 0 = LV Buck 2 will be enabled after valid request
[3]	VREFEN	RW	Request voltage reference LDO_VRF enable	1 = LDO_VRF will be disabled after valid request 0 = LDO_VRF will be enabled after valid request
[2:0]	STATEREQ	RWHC	Request for device state transition Cleared to 000 by the HW after the request is processed. After writing a new state value a user should not change the value before it's cleared by HW.	000 = RESERVED; 001 = RESERVED; 010 = WAKE; 011 = STANDBY; 100 = SLEEP; 101 = NORMAL; 110 = INIT; 111 = NONE

WWDSCMD [7:0]

ADDRESS: 0x17

BITS	FIELD	TYPE	DESCRIPTION	DECODE
[7]	TRIG_STATUS	R	Last SPI trigger received	
[6:1]	RSV	R	Reserved	
[0]	TRIG	RW	Window watchdog SPI trigger command Read TRIG_STATUS bit first and write inverted value to TRIG bit.	

FWDRSP [7:0]

ADDRESS: 0x18

BITS	FIELD	TYPE	DESCRIPTION	DECODE
[7:0]	FWDRSP	RW	Functional watchdog response Write functional watchdog response bytes to this field.	

FWDRSPSYNC [7:0]

ADDRESS: 0x19

BITS	FIELD	TYPE	DESCRIPTION	DECODE
[7:0]	FWDRSPS	RW	Functional watchdog heartbeat synchronization response Write the last functional watchdog response byte to this field to synchronize/restart the heartbeat.	

SYSFAIL [7:0]

ADDRESS: 0x1A

BITS	FIELD	TYPE	DESCRIPTION	DECODE
[7]	INITF	RW1C	INIT failure flag INIT failure due to the third INIT failure in row. i.e. The device restarts INIT phase from FAILSAFE.	0 = No fault, write 0 - no action 1 = Fault occurred, write 1 to clear the flags
[6]	ABISTERR	RW1C	ABIST operation interrupted flag	0 = No fault, write 0 - no action

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			ABIST interrupted by any fault/event which is not part of ABIST.	1 = Fault occurred, write 1 to clear the flags
[5:4]	RSV	R	Reserved	
[3]	RSTB_MON_ERR	RW1C	RESETB monitor failure flag	0 = No fault, write 0 - no action 1 = Fault occurred, write 1 to clear the flags
[2]	VMONF	RW1C	Voltage monitor failure flag Voltage monitor failure occured which lead to FAILSAFE.	0 = No fault, write 0 - no action 1 = Fault occurred, write 1 to clear the flags, read MONSF0, MONSF1 and MONSF3 for details
[1]	OTF	RW1C	Over temperature failure flag	0 = No fault, write 0 - no action 1 = Fault occurred, write 1 to clear the flags, read OTFAIL for details
[0]	VOLTSELER R	RW1C	Double Bit error on voltage selection flag Device entered FAILSAFE state due to internal voltage selection failure.	0 = No fault, write 0 - no action 1 = Fault occurred, write 1 to clear the flags

INITERR [7:0]

ADDRESS: 0x1B

BITS	FIELD	TYPE	DESCRIPTION	DECODE
[7]	HARDRES	RW1C	Hard reset flag Hard reset has been generated due to the second INIT failure in row. i.e. The device restarts INIT phase for the 3rd time.	0 = No fault, write 0 - no action 1 = Fault occurred, write 1 to clear the flags
[6]	SOFTRES	RW1C	Soft reset flag Soft reset has been generated due to the first INIT failure. i.e. The device restarts INIT phase for the 2nd time.	0 = No fault, write 0 - no action 1 = Fault occurred, write 1 to clear the flags
[5]	ERRF	RW1C	MCU error monitor failure flag	0 = No fault, write 0 - no action 1 = Fault occurred, write 1 to clear the flags
[4]	FWDF	RW1C	Functional watchdog error counter overflow failure flag	0 = No fault, write 0 - no action 1 = Fault occurred, write 1 to clear the flags
[3]	WWDF	RW1C	Window watchdog error counter overflow failure flag	0 = No fault, write 0 - no action 1 = Fault occurred, write 1 to clear the flags
[2]	VMONF	RW1C	Voltage monitor failure flag Voltage monitor failure occured which lead to FAILSAFE.	0 = No fault, write 0 - no action 1 = Fault occurred, write 1 to clear the flags, read MONSF2 for details
[1]	CRG_ERR	RW1C	clock monitor or reset monitor failure flag.	0 = No fault, write 0 - no action 1 = Fault occurred, write 1 to clear the flags
[0]	RSV	RW1C	Reserved	

IF [7:0]

ADDRESS: 0x1C

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BITS	FIELD	TYPE	DESCRIPTION	DECODE
[7]	INTMISS	R	Interrupt not serviced in time flag Interrupt has not been serviced within tINT,TO time	0 = No interrupt timeout happened 1 = Interrupt timeout happened, cleared by hardware when all other flags in IF are cleared.
[6]	ABIST	RW1C	Requested ABIST operation performed flag	0 = No interrupt, write 0 - no action 1 = Interrupt flag active, write 1 to clear the flag
[5]	OTF	RW1C	Over temperature failure interrupt flag	0 = No interrupt, write 0 - no action 1 = Interrupt flag active, write 1 to clear the flag, read OTFAIL for details
[4]	OTW	RW1C	Over temperature warning interrupt flag	0 = No interrupt, write 0 - no action 1 = Interrupt flag active, write 1 to clear the flag, read OTWRNSF for details
[3]	MON	RW1C	Monitor interrupt flag	0 = No interrupt, write 0 - no action 1 = Interrupt flag active, write 1 to clear the flag, read MONSF0, MONSF1, MONSF2 and MONSF3 for details
[2]	SPI	RW1C	SPI interrupt flag	0 = No interrupt, write 0 - no action 1 = Interrupt flag active, write 1 to clear the flag, read SPISF for details
[1]	WK	RW1C	Wake interrupt flag Only set if device generates an interrupt when leaving SLEEP state.	0 = No interrupt, write 0 - no action 1 = Interrupt flag active, write 1 to clear the flag, read WKSF for details
[0]	SYS	RW1C	System interrupt flag	0 = No interrupt, write 0 - no action 1 = Interrupt flag active, write 1 to clear the flag, read SYSSF for details

SYSSF [7:0]				
ADDRESS: 0x1D				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	RSV	R	Reserved	
[5]	NO_OP	RW1C	State transition request failure flag Requested state transition via DEVCTRL & DEVCTRLN could not be performed because of wrong protocol.	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[4]	TRFAIL	RW1C	Transition to low power failed flag Transition to low power failed either due to the LDO_UC current monitor, WAK high level or a rising edge on EN PIN during TRDEL time.	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[3]	ERRMISS	RW1C	MCU error miss status flag Set only when SYSPCFG1.ERRRECEN='1'	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[2]	FWDE	RW1C	Functional watchdog error interrupt flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[1]	WWDE	RW1C	Window watchdog error interrupt flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[0]	CFGE	RW1C	Protected configuration double bit error flag	0 = Write 0 - no action

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			Double bit error occurred on protected configuration register. Status registers shall be read in order to determine which configuration has changed.	1 = Event detected, write 1 to clear the flag

WKSF [7:0]				
ADDRESS: 0x1E				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	WAKST	R	WAKE input status	0 = Voltage at pin WAKE is in low level signal range 1 = Voltage at pin WAKE is in high level signal range
[6]	ENST	R	EN input status	0 = Voltage at pin EN is in low level signal range 1 = Voltage at pin EN is in high level signal range
[5]	RSV	R	Reserved	
[4]	WKSPI	RW1C	Wakeup from SLEEP by SPI flag (GoToWAKE)	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[3]	WKTIM	RW1C	Wake timer wakeup flag Bit will also be set if STANDBY state left because of wake timer expired.	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[2]	CMON	RW1C	LDO_UC current monitor threshold wakeup flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[1]	EN	RW1C	EN signal wakeup flag Bit will also be set if FAILSAFE or STANDBY state left because of EN.	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[0]	WAKE	RW1C	WAKE signal wakeup flag Bit will also be set if FAILSAFE or STANDBY state left because of WAK.	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag

SPISF [7:0]				
ADDRESS: 0x1F				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:5]	RSV	R	Reserved	
[4]	LOCK	RW1C	LOCK or UNLOCK procedure error flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[3]	DURE	RW1C	SPI frame duration error flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[2]	ADDRE	RW1C	SPI address invalid flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[1]	LENE	RW1C	SPI frame length invalid flag Number of detected SPI clock cycles different than 16.	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag

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[0]	PARE	RW1C	SPI frame parity error flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag

MONSF0 [7:0]				
ADDRESS: 0x20				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	TRK2SG	RW1C	Tracker2 short to ground status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[6]	TRK1SG	RW1C	Tracker1 short to ground status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[5]	VREFSG	RW1C	Voltage reference short to ground status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[4]	COMSG	RW1C	Communication LDO short to ground status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[3]	VEXTSG	RW1C	External voltage short to ground status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[2]	STBYSG	RW1C	Standby LDO short to ground status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[1]	UCSG	RW1C	uC LDO short to ground status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[0]	BK1SG	RW1C	Pre-Buck1 voltage short to ground status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag

MONSF1 [7:0]				
ADDRESS: 0x21				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	TRK2OV	RW1C	Tracker2 over voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[6]	TRK1OV	RW1C	Tracker1 over voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[5]	VREFOV	RW1C	Voltage reference over voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[4]	COMOV	RW1C	Communication LDO over voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[3]	VEXTOV	RW1C	External voltage over voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag

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[2]	STBYOV	RW1C	Standby LDO over voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[1]	UCOV	RW1C	uC LDO over voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[0]	BK1OV	RW1C	Pre-Buck1 voltage over voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag

MONSF2 [7:0]				
ADDRESS: 0x22				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	TRK2UV	RW1C	Tracker2 under voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[6]	TRK1UV	RW1C	Tracker1 under voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[5]	VREFUV	RW1C	Voltage reference under voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[4]	COMUV	RW1C	Communication LDO under voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[3]	VEXTUV	RW1C	External voltage under voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[2]	STBYUV	RW1C	Standby LDO under voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[1]	UCUV	RW1C	uC LDO under voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[0]	BK1UV	RW1C	Pre-Buck1 voltage under voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag

MONSF3 [7:0]				
ADDRESS: 0x23				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	BIASHI	RW1C	Bias current too high flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[6]	BIASLOW	RW1C	Bias current too low flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[5]	BG12OV	RW1C	Bandgap comparator over voltage condition flag (VBG1 ⩾ VBG2 + 4%)	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag

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[4]	BG12UV	RW1C	Bandgap comparator under voltage condition flag (VBG1 ⩽ VBG2 - 4%)	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[3]	BK2SG	RW1C	LV Buck2 short to ground status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[2]	BK2OV	RW1C	LV Buck2 over voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[1]	BK2UV	RW1C	LV Buck2 under voltage status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[0]	VBATOV	RW1C	Supply voltage VSUP over voltage flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag

OTFAIL [7:0]				
ADDRESS: 0x24				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	MON	RW1C	Monitoring over temperature flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[6:5]	RSV	R	Reserved	
[4]	COM	RW1C	Communication LDO over temperature flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[3]	BK2	RW1C	LV Buck2 over temperature flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[2]	RSV	R	Reserved	
[1]	UC	RW1C	uC LDO over temperature flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[0]	BK1	RW1C	Pre-Buck1 over temperature flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag

OTWRNSF [7:0]				
ADDRESS: 0x25				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	RSV	R	Reserved	
[5]	VREF	RW1C	Voltage reference over load flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[4]	COM	RW1C	Communication LDO over temperature warning flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[3]	BK2	RW1C	LV Buck2 over temperature warning flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[2]	STDBY	RW1C	Standby LDO over load flag	0 = Write 0 - no action

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			(over current for more than 1ms)	1 = Event detected, write 1 to clear the flag
[1]	UC	RW1C	uC LDO over temperature warning flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[0]	PREG	RW1C	Pre-regulator over temperature warning flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag

VMONSTAT [7:0]				
ADDRESS: 0x26				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	TRK2ST	R	Tracker2 voltage ready status	0 = Voltage is out of range or not enabled 1 = Voltage is OK
[6]	TRK1ST	R	Tracker1 voltage ready status	0 = Voltage is out of range or not enabled 1 = Voltage is OK
[5]	VREFST	R	Voltage reference voltage ready status	0 = Voltage is out of range or not enabled 1 = Voltage is OK
[4]	COMST	R	Communication LDO voltage ready status	0 = Voltage is out of range or not enabled 1 = Voltage is OK
[3]	VEXTST	R	External voltage ready status	0 = Voltage is out of range or not enabled 1 = Voltage is OK
[2]	STBYST	R	Standby LDO voltage ready status	0 = Voltage is out of range or not enabled 1 = Voltage is OK
[1]	BK2ST	R	Internal Post Buck voltage ready status	0 = Voltage is out of range or not enabled 1 = Voltage is OK
[0]	BK1ST	R	Pre-regulator voltage ready status	0 = Voltage is out of range or not enabled 1 = Voltage is OK

DEVSTAT [7:0]				
ADDRESS: 0x27				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	TRK2EN	R	Tracker2 voltage enable status	0 = Voltage is disabled 1 = Voltage is enabled
[6]	TRK1EN	R	Tracker1 voltage enable status	0 = Voltage is disabled 1 = Voltage is enabled
[5]	COMEN	R	Communication LDO enable status	0 = Voltage is disabled 1 = Voltage is enabled
[4]	STBYEN	R	Standby LDO enable status	0 = Voltage is disabled 1 = Voltage is enabled
[3]	VREFEN	R	Reference voltage enable status	0 = Voltage is disabled 1 = Voltage is enabled
[2:0]	STATE	R	Device state	000 = NONE; 001 = INIT;

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				010 = NORMAL; 011 = SLEEP; 100 = STANDBY; 101 = WAKE; 110 = RESERVED; 111 = RESERVED

PROSTAT [7:0]				
ADDRESS: 0x28				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	KEY4OK	R	Key4 ok status Information about validity of the 4th received protection key byte	0 = Key not valid 1 = Key valid
[6]	KEY3OK	R	Key3 ok status Information about validity of the 3rd received protection key byte	0 = Key not valid 1 = Key valid
[5]	KEY2OK	R	Key2 ok status Information about validity of the 2nd received protection key byte	0 = Key not valid 1 = Key valid
[4]	KEY1OK	R	Key1 ok status Information about validity of the 1st received protection key byte	0 = Key not valid 1 = Key valid
[3:1]	RSV	R	Reserved	
[0]	LOCK	R	Protected register lock status	0 = Access is unlocked 1 = Access is locked

WWDSTAT [7:0]				
ADDRESS: 0x29				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:4]	RSV	R	Reserved	
[3:0]	WWDECNT	R	Window watchdog error counter status	WWD error counter = WWDECNT[3:0]*1 times

FWDSTAT0 [7:0]				
ADDRESS: 0x2A				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	RSV	R	Reserved	
[6]	FWDRSPOK	R	Functional watchdog response check error status	0 = Response message is wrong 1 = All received bytes in response message are correct
[5:4]	FWDRSPC	R	Functional watchdog response counter value	
[3:0]	FWDQUEST	R	Functional watchdog question	
FWDSTAT1 [7:0]				
ADDRESS: 0x2B				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:4]	RSV	R	Reserved	
[3:0]	FWDECNT	R	Functional watchdog error counter value	FWD error counter = FWDECNT[3:0]*1 times

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ABIST_CTRL0 [7:0]				
ADDRESS: 0x2C				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:4]	STATUS	R	ABIST global error status ABIST status information after requested operation has been performed, information shall only be considered valid, once START bit is cleared. Bits have different reset class than whole register. The Bits are reset according to *R1).	5 = Selected ABIST operation performed with no errors 10 = Selected ABIST operation performed with errors, check respective SELECT registers
[3]	INT	RW	Safety path selection Select whether safe state or interrupt related comparator shall be tested.	0 = safe state related comparators shall be tested 1 = interrupt related comparators shall be tested
[2]	SINGLE	RW	ABIST Sequence selection Select whether a single comparator shall be tested or all comparators in predefined sequence	0 = Predefined sequence 1 = Single comparator test
[1]	PATH	RW	Full path test selection Select the path which should be covered by ABIST operation	0 = Comparator only 1 = Comparator and corresponding deglitching logic, shall be selected in case contribution to respective safety measure needs to be tested
[0]	START	RWHC	Start ABIST operation The ABIST operation itself will be started. This bit is cleared after ABIST operation has been performed	0 = Operation done 1 = Start operation

ABIST_CTRL1 [7:0]				
ADDRESS: 0x2D				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:2]	RSV	R	Reserved	
[1]	ABIST_CLK_EN	RW	ABIST clock check enable Select ABIST clock to check its functionality	0 = Disable 1 = Enable
[0]	OV_TRIG	RW	Overvoltage trigger for secondary internal monitor enable	0 = Disable 1 = Enable

ABIST_SELECT0 [7:0]				
ADDRESS: 0x2E				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	TRK2OV	RWHU	Select TRK2 OV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator

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[6]	TRK1OV	RWHU	Select TRK1 OV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[5]	VREFOV	RWHU	Select VREF OV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[4]	COMOV	RWHU	Select COM OV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[3]	VEXTOV	RWHU	Select External voltage OV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[2]	STBYOV	RWHU	Select Standby LDO OV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[1]	UCOV	RWHU	Select uC LDO OV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[0]	PREGOV	RWHU	Select Pre-regulator OV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator

ABIST_SELECT1 [7:0]				
ADDRESS: 0x2F				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	TRK2UV	RWHU	Select TRK2 UV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[6]	TRK1UV	RWHU	Select TRK1 UV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[5]	VREFUV	RWHU	Select VREF UV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on

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				comparator, bit will be set in case of ABIST fail for this comparator
[4]	COMUV	RWHU	Select COM UV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[3]	VEXTUV	RWHU	Select External voltage UV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[2]	STBYUV	RWHU	Select Standby LDO UV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[1]	UCUV	RWHU	Select uC LDO UV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[0]	PREGUV	RWHU	Select Pre-regulator UV comparator for ABIST operation	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator

ABIST_SELECT2 [7:0]				
ADDRESS: 0x30				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	BIASHI	RWHU	Bias current too high flag	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[6]	BIASLOW	RWHU	Bias current too low flag	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[5]	BG12OV	RWHU	Bandgap comparator over voltage condition flag (VBG1 ⩾ VBG2 + 4%)	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[4]	BG12UV	RWHU	Bandgap comparator under voltage condition flag (VBG1 ⩽ VBG2 - 4%)	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[3]	INTOV	RWHU	Select internal supply OV condition	0 = Not selected 1 = Selected, bit will be cleared upon

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				successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[2]	BK2OV	RWHU	Select internal LV Buck2 OV condition	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[1]	BK2UV	RWHU	Select internal LV Buck2 UV condition	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator
[0]	VBATOV	RWHU	Supply voltage VSUP over voltage flag	0 = Not selected 1 = Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator

BCK_FREQ_CHANGE [7:0]				
ADDRESS: 0x31				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	FSS_MODE	RW	Frequency Spread Spectrum Mode. Refer to FRE_SP_THR	1 = Pseudorandom Modulation 0 = Triangle Modulation
[6]	FSS_PERIOD	RW	Frequency Spread Period. Refer to FRE_SP_THR	0 = 9KHz 1 = 4.5KHz
[5:3]	RSV	R	Reserved	
[2:0]	BCK_FREQ_SEL	RW	BUCK switching frequency change For high and low switching mode. New value needs to be validated via data_valid procedure	000 = No change; 001 = Change buck frequency by approx. +1.5% from $f_{OSC,step\text{-}down}$; 010 = Change buck frequency by approx. +3% from $f_{OSC,step\text{-}down}$; 011 = Change buck frequency by approx. +4.5% from $f_{OSC,step\text{-}down}$; 100 = No change; 101 = Change buck frequency by approx. -1.5% from $f_{OSC,step\text{-}down}$; 110 = Change buck frequency by approx. -3% from $f_{OSC,step\text{-}down}$; 111 = Change buck frequency by approx. -4.5% from $f_{OSC,step\text{-}down}$

BCK_FRE_SPREAD [7:0]				
ADDRESS: 0x32				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:0]	FRE_SP_THR	RW	Spread spectrum Select the percentage of frequency spread(+/-). The mean frequency is reduced by the percentage as well keeping the maximum frequency at	00h = No change; 2Bh = ±1% 55h = ±2% 80h = ±3% AAh = ±4%

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			the nominal frequency selected by FRE.	D5h = ±5% FFh = ±6% C4h = ±10% others = No change

BK1_CTRL [7:0]				
ADDRESS: 0x33				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	BUSY	R	DATA_VALID parameter update ready status	0 = update done 1 = update ongoing
[6]	DATA_VALID	RW	Enable buck update Update Command to load new parameter for stepdown regulator (after configuration write 1 to update and write 0 after BUSY flag is cleared to proceed operation)	0 = No action 1 = Load new parameters
[5:1]	RSV	R	Reserved	
[0]	BK2DVS_UNLOCK	RW	BK2DVS and BK2DVSN unlock bit	0 = lock 1 = unlock

BK2DVS [7:0]				
ADDRESS: 0x34				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	BK2_OV_SEL	RW	Interal Post Buck OV monitor threshold Register	00 = OV rising threshold is VSET*106%, falling thrshold is VSET*105%; 01 = OV rising threshold is VSET*104%, falling thrshold is VSET*103%; 10 = OV rising threshold is VSET*108%, falling thrshold is VSET*107%; 11 = OV rising threshold is VSET*110%, falling thrshold is VSET*109%.
[6:0]	BK2DVS	RW	Internal Post Buck Output Voltage Program Request Register	VOUT2=LVDVS[6:0]*10mV+600mV, 600mV~1870mV (720mV~1800mV) 0000000 = 0.60V; 0000001 = 0.61V; 0000010 = 0.62V; 0000011 = 0.63V; … 1111100 = 1.84V; 1111101 = 1.85V;1111110 = 1.86V; 1111111 = 1.87V.

BK2DVSN [7:0]				
ADDRESS: 0x35				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**

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[7]	BK2_UV_SEL	RW	Interal Post Buck UV monitor threshold Register	01 = UV rising threshold is VSET*94%, falling thrshold is VSET*95%; 00 = UV rising threshold is VSET*96%, falling thrshold is VSET*97%; 10 = UV rising threshold is VSET*92%, falling thrshold is VSET*93%; 11 = UV rising threshold is VSET*90%, falling thrshold is VSET*91%.
[6:0]	BK2DVSN	RW	Internal Post Buck Output Voltage Program Request Inverter Register	VOUT2=LVDVSN[6:0]*10mV+600mV, 600mV~1870mV (720mV~1800mV) 1111111 = 0.60V; 1111110 = 0.61V;1111101 = 0.62V; 1111100 = 0.63V; … 00000011 = 1.84V; 00000010 = 1.85V;00000001 = 1.86V; 00000000 = 1.87V.

FWD_KEY [7:0]

ADDRESS: 0x3A

BITS	FIELD	TYPE	DESCRIPTION	DECODE
[7:0]	FWD_KEY	R	Function watchdog's respone	

MONFS4 [7:0]

ADDRESS: 0x3B

BITS	FIELD	TYPE	DESCRIPTION	DECODE
[7:6]	RSV	R	Reserved	N/A
[5]	BOOST_OC	RW1C	Boost over current status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[4]	GNDLOSS	RW1C	GND loss status flag	0 = Write 0 - no action 1 = Event detected, write 1 to clear the flag
[3:0]	RSV	R	Reserved	

MCSMON [7:0]

ADDRESS: 0x3C

BITS	FIELD	TYPE	DESCRIPTION	DECODE
[7]	PROG	RW	MCU programming support enable(OR combination with PROG pin)	0 = Disabled via SPI(unless enabled by PROG pin high) 1 = Enabled via SPI(independent of PROG pin)
[6]	MPSIN	R	MCU programming support enable(OR combination with PROG bitfield)	0 = Disabled via pin PROG(unless enabled by PROG bitfield being set) 1 = Enabled via pin

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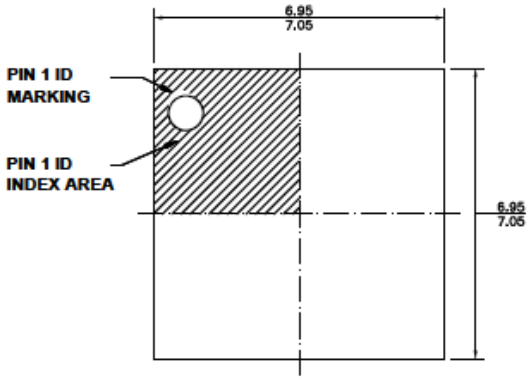
				PROG(independent of PROG bitfield)
[5:0]	CYCMON	R	Watchdog cycle timer monitor	0D 0 wd cycles passed 1D 1 wd cycles passed 2D 2 wd cycles passed ... 50D 50 wd cycles passed 51D not used ... 63D not used

CHIP_CODE [7:0]				
ADDRESS: 0x3D				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:0]	CHIP_CODE	RW	Chip Suffix Code	Chip Suffix Code, refer to Rev Note.

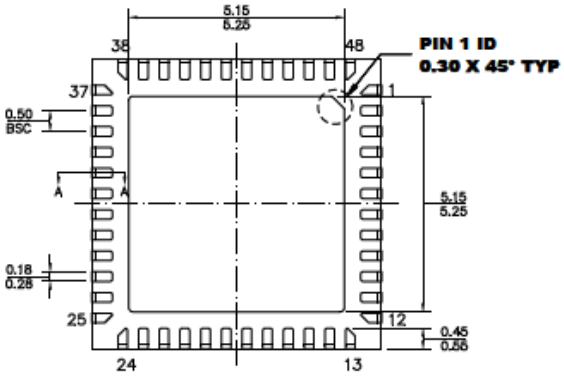
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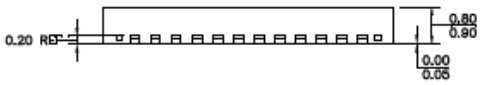
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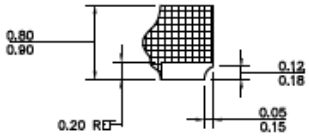
TOP VIEW



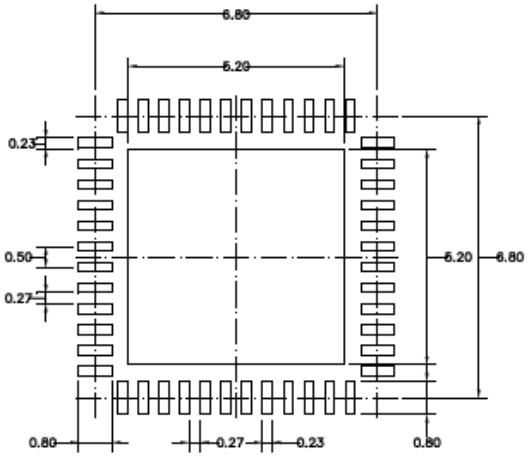
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) DRAWING CONFIRMS TO JEDEC MO-220.
6) DRAWING IS NOT TO SCALE.

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