2.7V-6V Vin 4A Synchronous Step Down Convertor

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1
    Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- Input Voltage Range: 2.7V-6V
- Up to 4A Continuous Output Current
- 43μA Quiescent Current
- 0.6V±1% Feedback Reference Voltage
- Integrated 14mΩ High-Side and 9mΩ Low-Side Power MOSFETs
- Adjustable1.2MHz~4MHz Switching Frequencies
- Integrated Frequency Dither for EMI Mitigation
- Selectable PFM or FCCM Operation
- Active output discharge
- Programmable Soft Start Time
- Power Good Indicator
- Integrated Protection Feature
  - Cycle-by-cycle current limit
  - Under-voltage Lockout
  - HICCUP Over Current Protection
  - Thermal Shutdown Protection:170°C
- QFN-9L 2mm*3mm Package
- Available in a Wettable Flank Package

APPLICATIONS

- Automotive Infotainment
- Advanced Driver Assistance System(ADAS)
- Solid state driver

DESCRIPTION

The SCT2140Q is a monolithic, step-down switch-mode converter with built-in internal 14mΩ High-Side and 9mΩ Low-Side Power MOSFETs. The device achieves 4A of continuous output current from a 2.7V to 6V input voltage range, with excellent load and line regulation. The output voltage can be regulated to as low as 0.6V.

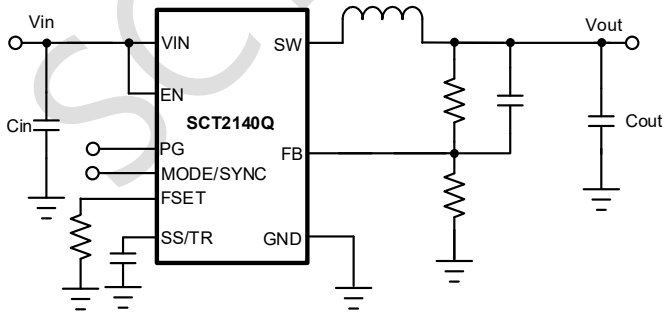
The SCT2140Q, adopting the constant-on time (COT) mode control provides fast transient response and eases loop stabilization, greatly simplifies the converter off-chip configuration. The switching clock frequency can be programmed from 1.2MHz to 4MHz for optimization of the filter size and output voltage ripple.

The SCT2140Q features programmable soft-start time to avoid large inrush current and output voltage overshoot during startup. The SCT2140Q has MODE pin to select Pulse Frequency Modulation (PFM) operation mode to achieve the light load power save or Forced Continuous Conduction Mode (FCCM) to achieve low light load ripple.

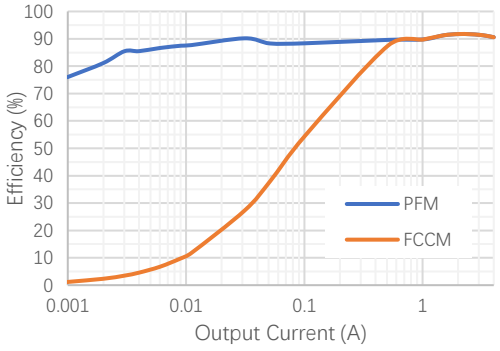
It includes full protection features, such as cycle-by-cycle current limit and hiccup over current protection, output under-voltage protection, input under-voltage lockout, and thermal shutdown.

The SCT2140Q requires a minimal number of external components and is available in a space-saving QFN-9L 2mm*3mm package with Wettable Flank.

TYPICAL APPLICATION



2.7V-6V, Synchronous Buck Converter



Efficiency, Vin=5V, Vout=1.8V

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 0.8: Customer sample.

DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL
SCT2140QFSAR	Tape & Reel	5000	2140Q	9	FCTQFN2X3-9L	1

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted (1)

DESCRIPTION	MIN	MAX	UNIT
VIN, EN, PG, SW, FSET, MODE/SYNC	-0.3	6.5	V
SW(<10ns)	-2.5	VIN+1	V
SS/TR, FB	-0.3	5.5	V
Operating junction temperature T_J(2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

PIN CONFIGURATION

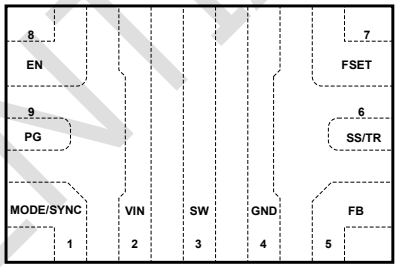


Figure1: Top View FCTQFN2X3-9L

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
MODE/SYNC	1	Mode selection and synchronization input. Connect to logic high for FCCM mode. Connect to logic low or ground for PFM mode. Do not leave this pin floating. The switching frequency can be synchronized by this pin using an external clock.
VIN	2	Power supply input pin.
SW	3	Switch output. SW is driven up to VIN through the high-side power MOSFET during on-time. The inductor current drives SW to negative voltage through low-side power MOSFET during off-time.
GND	4	Ground pin.
FB	5	Inverting input of the error amplifier. Connect a voltage divider from the output to this pin to set output voltage.
SS/TR	6	Soft-start time programming pin. An external capacitor and an internal current source set the ramp rate of the internal error amplifier reference during soft start. The pin can also be used as an input for tracking and sequencing.
FSET	7	Switching frequency set input. A resistor from this pin to GND defines the switching frequency if not externally synchronized.
EN	8	Enable logic input. Connect to logic low or floating to disable the device. Pull high to enable the device.
PG	9	Power-good indicator. An open-drain output which goes low if FB is below or above threshold voltage. Connect a pull up resistor to the system voltage rail. This pin can be floating when not using this function.

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RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	2.7	6	V
V_{OUT}	Output voltage range	0.6	Max duty*Vin	V
T_J	Operating junction temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per AEC-Q100-002, all pins (1)	-3	+3	kV
	Charged Device Model (CDM), per AEC-Q100-011, all pins (1)	-1	+1	kV

(1) HBM and CDM stressing are done in accordance with the AEC-Q100 specification.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	FCTQFN2X3-9L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	55.3	°C/W
$R_{\theta JC(top)}$	Junction to case (top) thermal parameter(1)	70.8	
$R_{\theta JB}$	Junction-to-board thermal resistance(1)	6.2	
Ψ_{JT}	Junction-to-top characterization parameter (1)	3.5	
Ψ_{JB}	Junction-to-board characterization parameter (1)	6	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2140Q is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT2140Q. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

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ELECTRICAL CHARACTERISTICS

V_{IN}=5V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		2.7		6	V
V_{IN_UVLO}	Input UVLO	V_{IN} rising	2.5	2.6	2.68	V
	Hysteresis			100		mV
I_{SD}	Shutdown current			300		nA
I_Q	Quiescent current from VIN	no load, no switching		43		uA
		Vo=1.8V, L=0.33uH, no load and switching, PFM mode(1)		70		uA
V_{FB}	Reference voltage of FB	Tj=25°C	0.594	0.6	0.606	V
		Tj=-40°C~150°C	0.591	0.6	0.609	V
I_{FB}	FB pin leakage current				100	nA
V_{UVP}	Undervoltage protection of FB reference voltage			420		mV
Power switch						
R_{HS}	High-side switch on resistance			14		mΩ
R_{LS}	Low-side switch on resistance			9		mΩ
$ILIM_{HS}$	High-side peak current limit			7.5		A
$ILIM_{LS}$	Low-side valley current limit			5.5		A
I_{LSZC}	LS zero cross current threshold	PFM mode		100		mA
$ILIM_{LSROC}$	LS reverse current limit	FCCM mode		-3		A
Switching Frequency						
F_{SW}	Switching frequency	RSET= 150kΩ		1.2		MHz
		RSET= 81.8kΩ		2.2		MHz
		RSET= 45kΩ		4		MHz
F_{SS_PERIOD}	Frequency spread spectrum period			6		kHz
F_{SS_RANGE}	Frequency spread spectrum in percentage of Fsw			±5		%
t_{ON_MIN}	Minimum on-time			50		ns
t_{OFF_MIN}	Minimum off-time			60		ns
Mode and Soft Start						
V_{MODE_FCCM}	MODE pin rising threshold	FCCM mode	1.2			V
V_{MODE_PFM}	MODE pin falling threshold	PFM mode			0.4	V
I_{SS}	Soft-start Current			8.5		uA
Rss	SS pull down resistance			300		Ω
EN & PG						
V_{ENH}	High-level Threshold voltage			1.1		V
V_{ENL}	Low- level Threshold voltage			1		V
R_{EN}	EN Pull down resistance			1		MΩ
R_{DIS}	Output Discharge resistance			50		Ω
V_{PGTL}	Power Good Lower Threshold voltage	FB rinsing (Reference to V_{FB})		95		%
		FB falling (Reference to V_{FB})		90		%
V_{PGTH}		FB rinsing (Reference to V_{FB})		110		%

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SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
	Power Good Upper Threshold voltage	FB falling (Reference to V_{FB})		105		%
V_{PG}	Power Good Logic Low Level Voltage	I_{PG}=-1mA			0.4	V
T_{PGD}	Power Good Delay			40		uS
Protection						
T_{SD}	Thermal shutdown threshold			170		°C
	Hysteresis			20		°C

Notes:
1) Guaranteed by sample characterization. Not tested in production.

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TYPICAL CHARACTERISTICS

V_{IN}=5V, V_{OUT}=1.8V, F_{SW}=2.2MHz, T_A=25°C, unless otherwise noted.

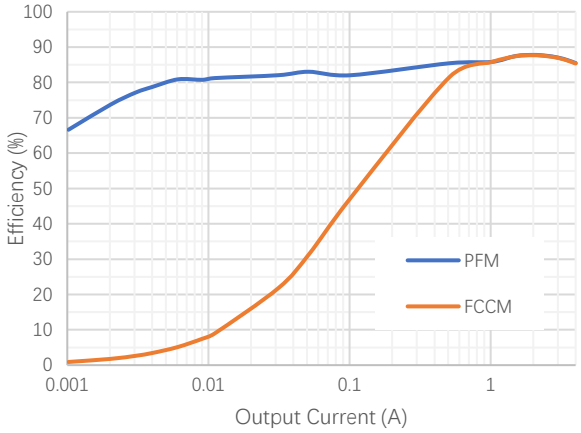


Figure 2. Efficiency vs Load Current, Vin=5V, Vout=1V

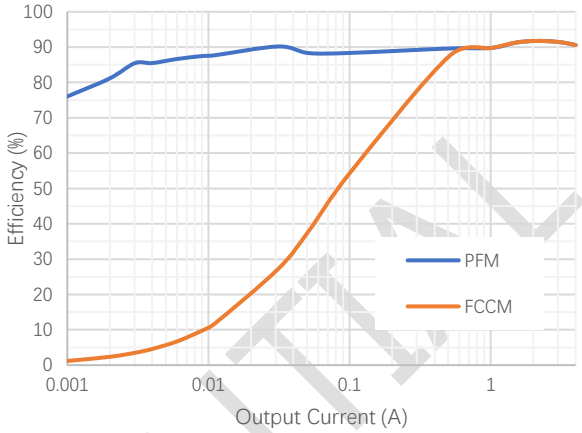


Figure 3. Efficiency vs Load Current, Vin=5V, Vout=1.8V

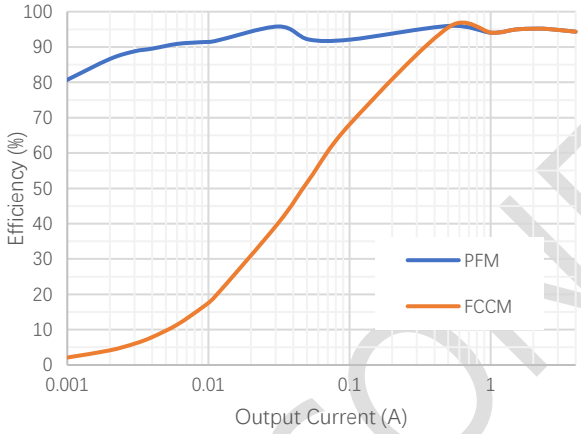


Figure 4. Efficiency vs Load Current, Vin=5V, Vout=3.3V

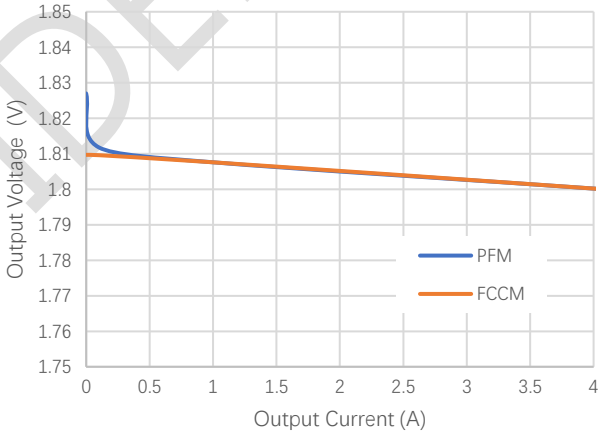


Figure 5. Load Regulation, Vin=5V, Vo=1.8V

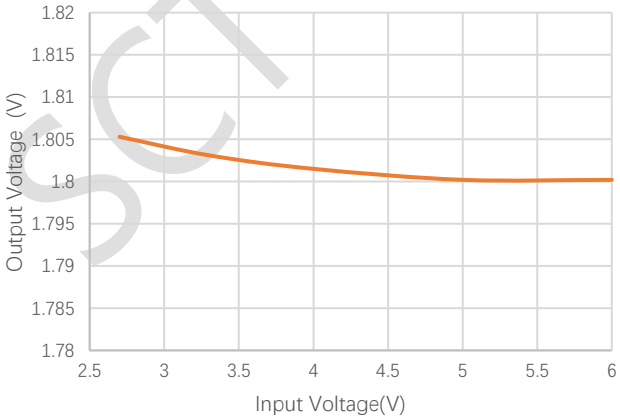


Figure 6. Line Regulation, Vo=1.8V, Io=2A

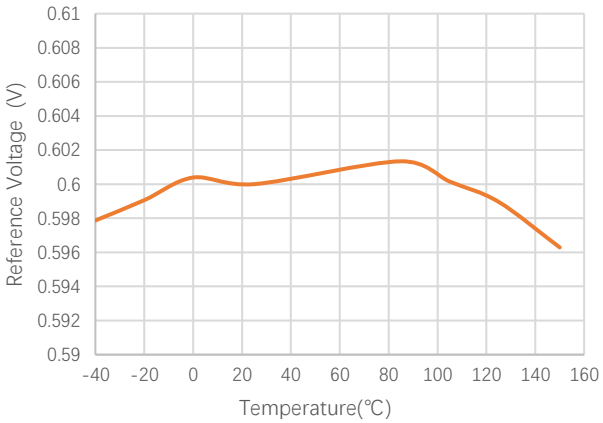


Figure 7. V_{FB} vs Temperature

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FUNCTIONAL BLOCK DIAGRAM

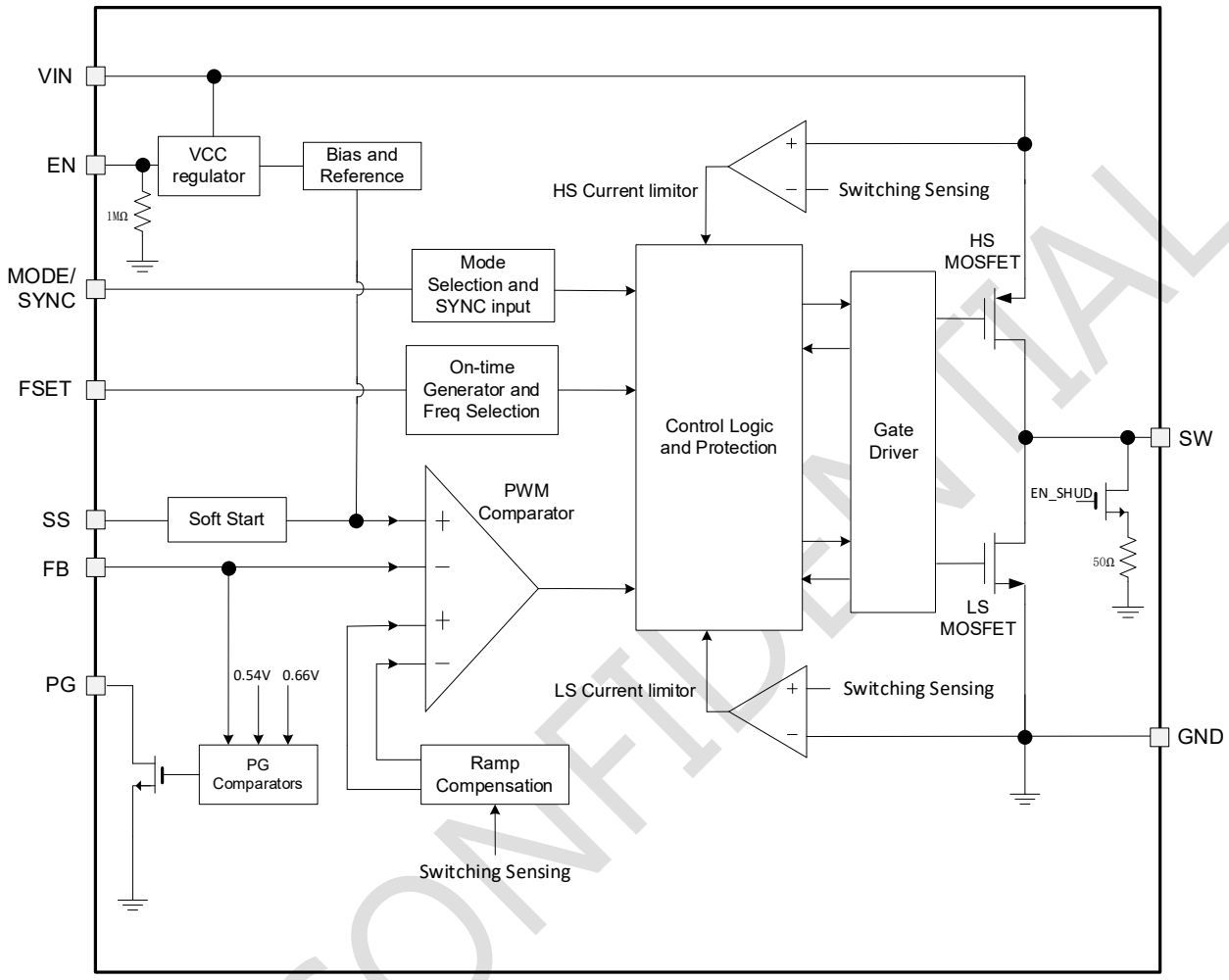


Figure 8. Functional Block Diagram

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OPERATION

Overview

The SCT2140Q is a 2.7V-6V input, 4A output, synchronous buck converter with built-in 14mΩ Rdson high-side and 9mΩ Rdson low-side power MOSFETs. It implements Constant on-time (COT) mode control to regulate output voltage, providing excellent line and load transient response and simplifying the external frequency compensation design.

The switching frequency can be set from 1.2MHz~4MHz by setting different FSET resistors, to optimize either the power efficiency or the external components' sizes. The device features two different operation modes at light loading: Pulse Frequency Modulation (PFM) mode and Forced Continuous Conduction Mode (FCCM). The quiescent current is typically 43uA under no load and PFM mode condition to achieve high efficiency at light load.

The SCT2140Q full protection features include the input under-voltage lockout, over-current protection with cycle-by-cycle current limiting and hiccup mode, output hard short protection and thermal shutdown protection.

Constant On-time Control

The SCT2140Q employs Constant on-time (COT) mode control providing fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET is turned on a fixed on-time period. The one on-time is calculated by the converter's input voltage (VIN) and the output voltage (VOUT) cycle-by-cycle based to maintain a pseudo-fixed frequency over the input voltage range. SCT2140Q turns off high-side MOSFET after the fixed on-time and turns on the low-side MOSFET. SCT2140Q turns off the low-side MOSFET once the output voltage dropped below the output regulation, the one-shot timer then reset and the high-side MOSFET is turned on again. The on-time is inversely proportional to the input voltage and proportional to the output voltage. It can be calculated using the following Equation 1:

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_S} \quad (1)$$

Where:

- VOUT is the output voltage.
- VIN is the input voltage.
- fs is the switching frequency.

After an on-time period, the regulator goes into the off-time period. The off-time period length depends on VFB in most cases. It will end when the FB voltage decreases below 0.6V, at which point the on-time period is triggered. If the off-time period is less than the minimum off time, the minimum off time will be applied, which is around 60ns typical.

Switching Frequency

The switching frequency can be programmed by FSET pin resistor from equation 2. The typical setting information is shown in following table1. The frequency setting is latched in at each power up and cannot be modified during operation. Cycling the input power or the EN pin can reselect the switching frequency.

$$fsw(\text{kHz}) = \frac{180000}{R_{SET}(\text{k}\Omega)} \quad (2)$$

Table 2. FSET Pin Set-up for typical Switching Frequency Selection

FSEL Set-up	RSET=150kΩ	RSET=81.8kΩ	RSET=45kΩ
Switching Frequency	1.2MHz	2.2MHz	4MHz

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Frequency Spread Spectrum

The SCT2140Q implements Frequency Spread Spectrum (FSS) function. The FSS circuitry shifts the switching frequency within ±5% window at a 6kHz modulation frequency as figure 9. The emission power of the fundamental switching frequency and its harmonics is distributed into smaller pieces. Thus, the peak EMI noise is reduced significantly.

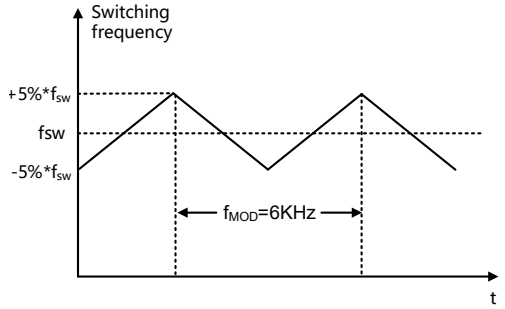


Figure 9. Frequency Spread Spectrum

MODE/SYNC

The MODE_SYNC pin combines operate mode control and frequency synchronization. The SCT2140Q works in PFM mode in light load when MODE/SYNC pin is set low and operates in forced PWM mode when the MODE_SYNC pin is set high. If an external clock frequency is applied on the MODE_SYNC pin, the switching frequency will be synchronized to the external clock frequency, and the device will operate in forced PWM mode. The external frequency must be selected in the frequency range as below table 1, and it must meet the specifications for the minimum on-time (50ns typical) and minimum off-time (60ns typical).

Table 1. Synchronization clock frequency range

	SYNC range	FSET Fsw	MIN	NOM	MAX	UNIT
F_{SYNC}	Synchronization clock frequency range (MODE/SYNC)	Nominal f_{SW} = 1.2 MHz	0.8		1.5	MHz
F_{SYNC}	Synchronization clock frequency range (MODE/SYNC)	Nominal f_{SW} = 2.2 MHz	1.8		2.7	MHz
F_{SYNC}	Synchronization clock frequency range (MODE/SYNC)	Nominal f_{SW} = 4 MHz	2.6		4.5	MHz

Pulse Frequency Modulation (PFM) Mode

Grounding the MODE/SYNC pin makes the SCT2140Q works at Pulse Frequency Modulation (PFM) mode to improve the power efficiency in light load. As the output current decreases from heavy load condition, the inductor current is also reduced. If the output current is reduced, the valley of the inductor current reaches the zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The low-side MOSFET is turned off when a zero inductor current is detected. As the load current further decreases the converter runs into discontinuous conduction mode. The on-time is kept the same as it is in continuous conduction mode. The off-time increases as it takes more time to discharge the output with a smaller load current.

Forced Continuous Conduction Mode (FCCM)

Connecting MODE/SYNC pin to VIN, the SCT2140Q forces the device operating at Forced Continuous Conduction Mode (FCCM) with pseudo-fixed switching frequency regardless loading current. Operating in FCCM mode can achieve smaller output voltage ripple compared with PFM at light load. When the load current approaches zero, the low-side MOSFET current crosses zero and sinks current from output to maintain the constant output. Hence power efficiency in light load is much lower than heavy load.

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Enable (EN) and output discharge

EN is a digital control pin that can turn the regulator on and off. When EN is pulled below the falling threshold voltage (1V), the chip shuts down. Force EN above its rising threshold voltage (1.1V) to turn the part on. Leave EN floating or pull it down to ground to disable the SCT2140Q. There is an internal 1MΩ resistor connected from the EN pin to ground.

When the device is disabled, the part automatically goes into output discharge mode, and its internal discharge MOSFET in SW pin provides a discharge path for the output capacitor.

Output Voltage

The SCT2140Q regulates the internal reference voltage at 0.6V. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$R_{FB_TOP} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_{FB_BOT} \quad (3)$$

Where:

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Soft Start/Tracking (SS/TR)

The SCT2140Q has an external soft start/tracking (SS/TR) pin that ramps up the output voltage at a controlled slew rate to avoid overshoot at startup. The SS pin's charge current is typically 8.5μA. The soft-start time (tss) is determined by the SS capacitor. tss can be calculated with Equation 4:

$$t_{ss}(ms) = \frac{C_{SS}(nF) * 0.6(V)}{Iss(uA)} \quad (4)$$

Where:

- Css is the external SS capacitor.
- Iss is the internal 8.5μA SS charge current.

The minimum SS capacitor is recommended to be 10nF.

The SS/TR pin can also be used as an input for tracking and sequencing. A voltage applied at SS/TR can be used to track a master voltage. The output voltage follows this voltage in both directions up and down in FCCM mode. In PFM mode, the output voltage decreases based on the load current. This requires the voltage applied at SS/TR to be below the feedback voltage (0.6V). If the voltage on SS/TR is above the feedback voltage, the internal reference is clamped to 0.6V and the output voltage no longer varies with SS/TR pin voltage.

Under Voltage Lockout UVLO

The SCT2140Q Under Voltage Lock Out (UVLO) default startup threshold is typical 2.6V with VIN rising and shutdown threshold is 2.5V with VIN falling.

Over Current Protection (OCP) and Hiccup Mode

In each switching cycle, the inductor current is sensed by monitoring the high-side MOSFET during the ON period and the low-side MOSFET during the OFF period. When the inductor current (IL) reaches the high-side MOSFET

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peak current limit (typically 7.5A) during the ON period, the high-side MOSFET is forced off immediately to prevent the current from rising further. Then the low-side MOSFET turns on, and stays on until IL drops below the low-side MOSFET valley current limit (typically 5.5A). If output loading continues to increase, output will drop below the V_{UVP}, and SS pin is discharged such that output is 0V. The device re-starts after a hiccup time of 10ms. When overload or hard short condition is removed, the device automatically recovers to enters normal regulating operation.

Power Good Indicator

The SCT2140Q has one power good (PG) output to indicate normal operation after the soft-start time. PG is the open drain of an internal MOSFET, which has a maximum RDS(ON) below 200Ω. PG can be connected to VIN or an external voltage source through an external a resistor (e.g., 100kΩ). After the input voltage is applied, the MOSFET turns on, and PG is pulled to GND before soft start is ready. After V_{FB} reaches 95% of V_{REF}, PG is pulled high by the external voltage source with 40us delay. When V_{FB} drops to 90% or rises to 110% of V_{REF}, the PG voltage is pulled to GND to indicate an output failure. If VIN and EN are not available, and PG is pulled up by an external power supply, PG will self-bias and assert. If a 100kΩ pull-up resistor is used, the voltage on the pin is below 0.6V.

Thermal Shutdown

Once the junction temperature in the SCT2140Q exceeds 170°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 150°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

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APPLICATION INFORMATION

Typical Application

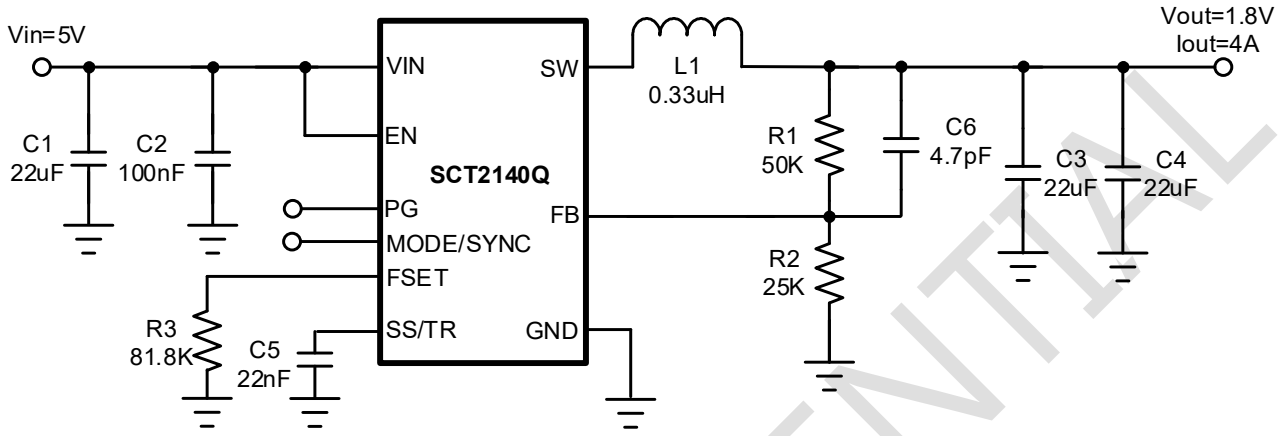


Figure 10. SCT2140Q Design Example, 1.8V Output

Design Parameters

Design Parameters	Example Value
Input Voltage	5V Normal 2.8V to 6V
Output Voltage	1.8V
Maximum Output Current	4A
Switching Frequency	2.2MHz
Output voltage ripple (peak to peak)	10mV
Transient Response 0A to 4A load step	ΔVout =100mV

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Output Voltage

The output voltage is set by an external resistor divider R1 and R2 in typical application schematic. Recommended R2 resistance is 25KΩ to reduce VOUT leakage current. Use Equation 5 to calculate R1.

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_2 \quad (5)$$

where:

- V_{REF} is the feedback reference voltage, typical 0.6V.

Table 2. R_1, R_2Value for Common Output Voltage (Room Temperature)

V_{OUT}	R_1	R_2
1 V	16.5KΩ	25KΩ
1.8 V	50KΩ	25KΩ
3.3 V	112.5KΩ	25KΩ

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance (DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 10%~40% of the maximum output current.

The peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 6.

$$I_{LPP} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{V_{IN} * L * f_{SW}} \quad (6)$$

Where:

- I_{LPP} is the inductor peak-to-peak current.
- L is the inductance of inductor.
- f_{SW} is the switching frequency.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 7 to calculate the inductance value.

$$L_{MIN} = \frac{V_{OUT}}{f_{SW} * LIR * I_{OUT(max)}} * (1 - \frac{V_{OUT}}{V_{IN(max)}}) \quad (7)$$

Where:

- L_{MIN} is the minimum inductance required.
- f_{sw} is the switching frequency.
- V_{OUT} is the output voltage.
- $V_{IN(max)}$ is the maximum input voltage.
- $I_{OUT(max)}$ is the maximum DC load current.
- LIR is coefficient of I_{LPP} to I_{OUT}.

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in Equation 8 and Equation 9.

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$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2} \quad (8)$$

$$I_{LRMS} = \sqrt{(I_{OUT})^2 + \frac{1}{12} * (I_{LPP})^2} \quad (9)$$

Where:

- I_{LPEAK} is the inductor peak current.
- I_{OUT} is the DC load current.
- I_{LPP} is the inductor peak-to-peak current.
- I_{LRMS} is the inductor RMS current.

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 7.5A. The most conservative approach is to choose an inductor with a saturation current rating greater than 7.5A. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the SCT2140Q can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a lower maximum output current.

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g. 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 10.

$$I_{CINRMS} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})} \quad (10)$$

The worst case condition occurs at $V_{IN}=2*V_{OUT}$, where:

$$I_{CINRMS} = 0.5 * I_{OUT} \quad (11)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 12 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} * C_{IN}} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}}) \quad (12)$$

For this example, 22μF, X7R ceramic capacitors rated for 10 V in parallel are used. And a 0.1μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

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Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 13 desired.

$$\Delta V_{OUT} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{8 * f_{SW}{}^2 * L * C_{OUT} * V_{IN}} \quad (13)$$

Where:

- ΔV_{OUT} is the output voltage ripple.
- f_{SW} is the switching frequency.
- L is the inductance of inductor.
- C_{OUT} is the output capacitance.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, two 1206 22μF ceramic output capacitors work for most applications.

Table 3: Component List with Typical Output Voltage BOM list

Fsw (MHz)	Vout (V)	L (uH)	R1 (kΩ)	R2 (kΩ)	Cf (pF)
1.2	1	0.47	16.5	25	4.7
	1.8	0.56	50	25	4.7
	3.3	0.68	112.5	25	4.7
2.2	1	0.33	16.5	25	4.7
	1.8	0.47	50	25	4.7
	3.3	0.56	112.5	25	4.7
4	1	0.22	16.5	25	4.7
	1.8	0.33	50	25	4.7
	3.3	0.47	112.5	25	4.7

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Application Waveforms

V_{IN}=5V, V_{OUT}=1.8V, F_{SW}=2.2MHz, T_A=25°C, unless otherwise noted.

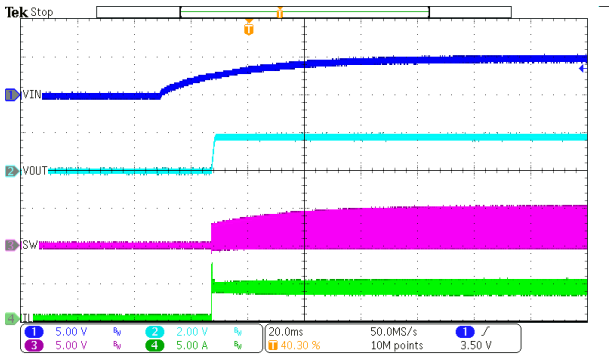


Figure 11. Power up (I_{LOAD}=4A)

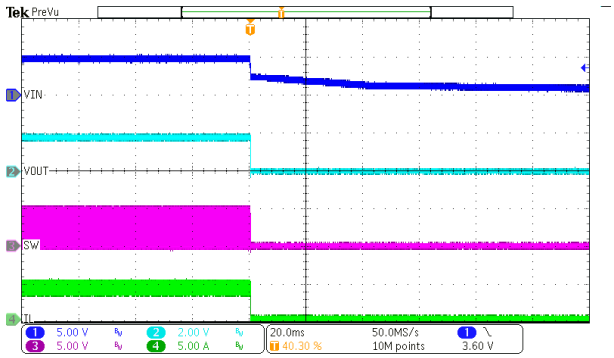


Figure 12. Power down (I_{LOAD}=4A)

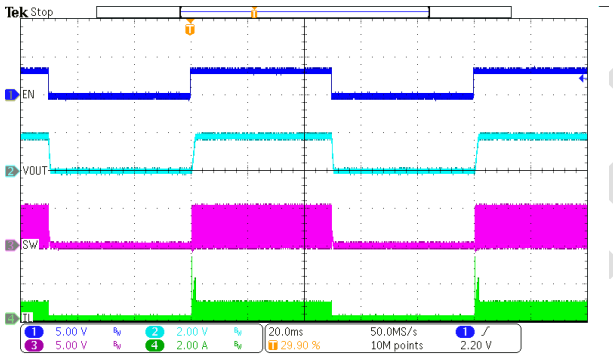


Figure 13. EN toggle (I_{LOAD}=0.1A)

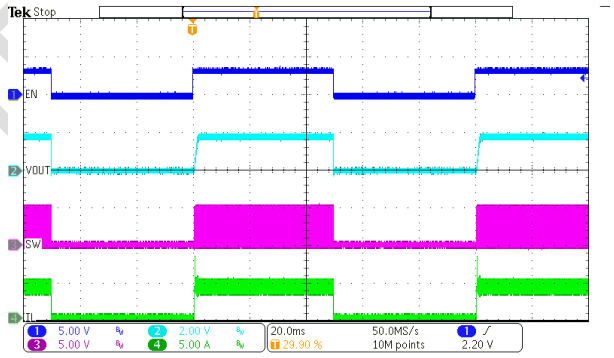


Figure 14. EN toggle (I_{LOAD}=4A)

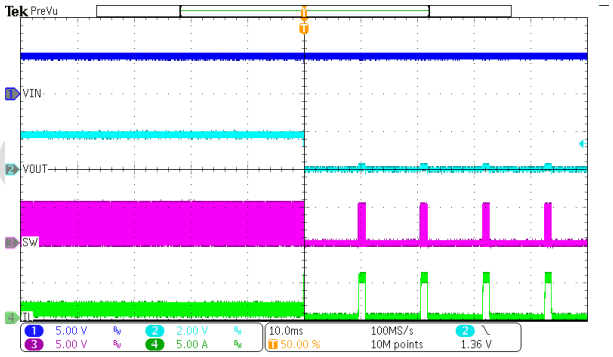


Figure 15. Over Current Protection (1A to hard short)

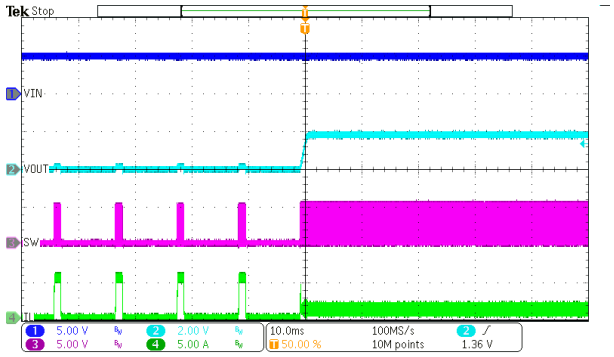


Figure 16. Over Current Release (hard short to 1A)

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Application Waveforms

V_{IN}=5V, V_{OUT}=1.8V, F_{SW}=2.2MHz, T_A=25°C, unless otherwise noted.

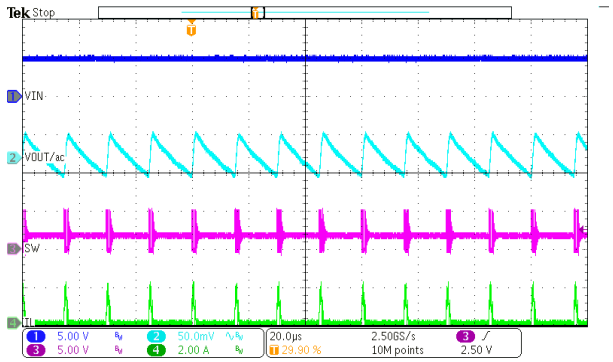


Figure 17. Output Ripple (I_{LOAD}=100mA, PFM mode)

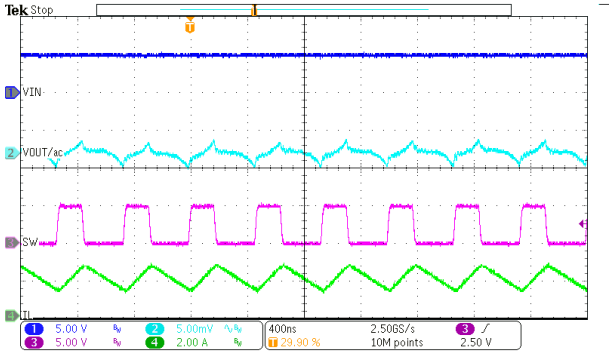


Figure 18. Output Ripple (I_{LOAD}=2A) Load

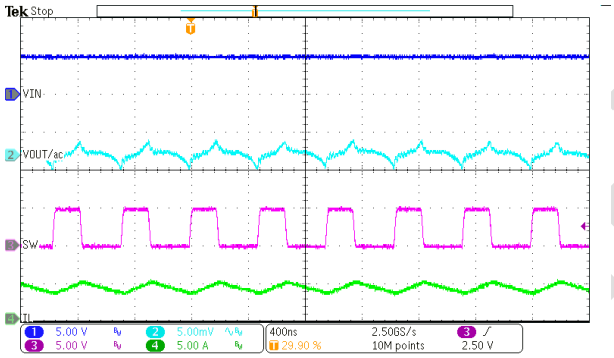


Figure 19. Output Ripple (I_{LOAD}=4A)

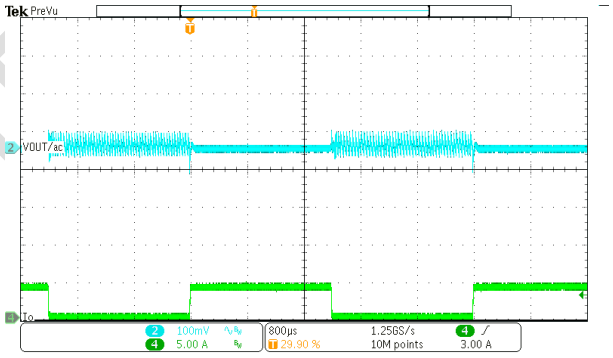


Figure 20. Transient (0A-4A, 1.6A/us, PFM mode)

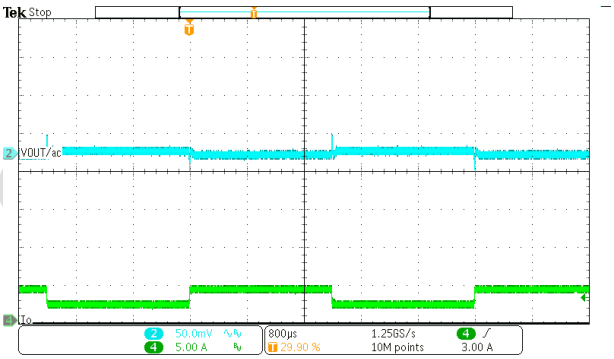


Figure 21. Load Transient (2A-4A, 1.6A/us)

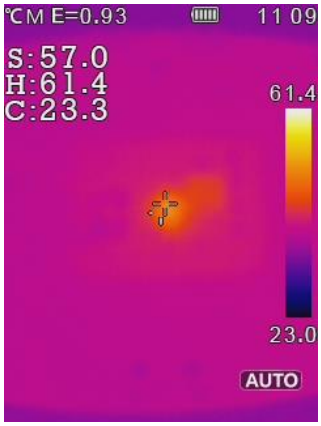


Figure 22. Thermal, V_{IN}=5V, V_{OUT}=1.8V, I_{LOAD}=4A

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Layout Guideline

Proper PCB layout is a critical for SCT2140Q's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.
4. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias directly under the IC. The center thermal pad should always be soldered to the board for mechanical strength and reliability, using multiple thermal vias underneath the thermal pad. Improper soldering thermal pad to ground plate on PCB will cause SW higher ringing and overshoot besides downgrading thermal performance. It is recommended 8mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss thru the vias is of concern, plugging or tenting can be used to achieve a repeatable process.
5. Output inductor should be placed close to the SW pin. The area of the PCB conductor minimized to prevent excessive capacitive coupling.

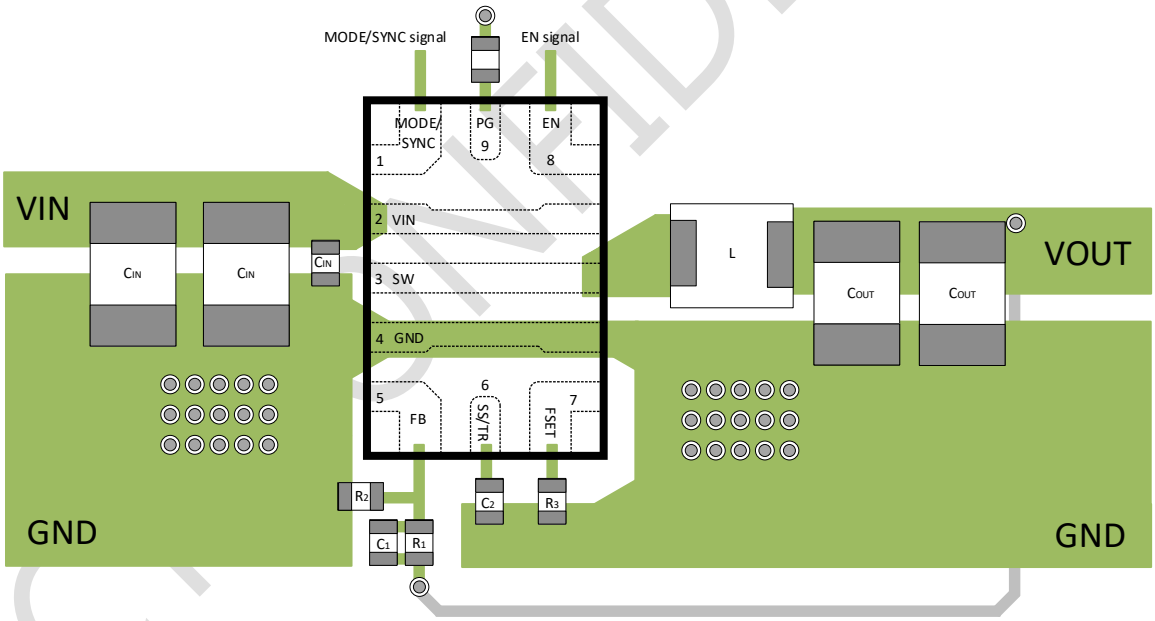
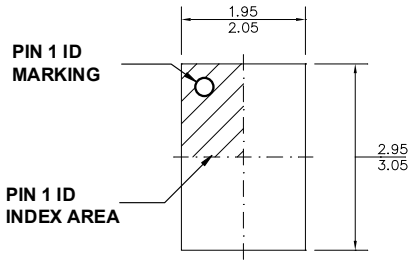


Figure 23. PCB Layout Example

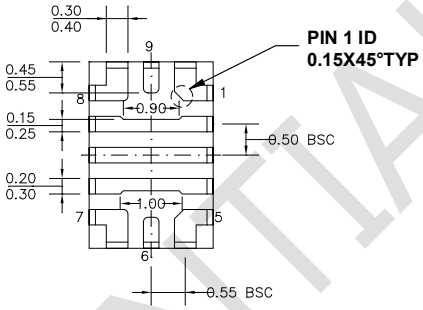
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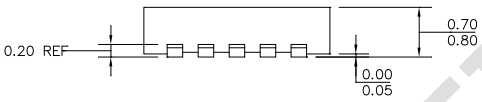
PACKAGE INFORMATION



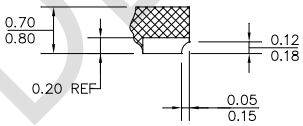
TOP VIEW



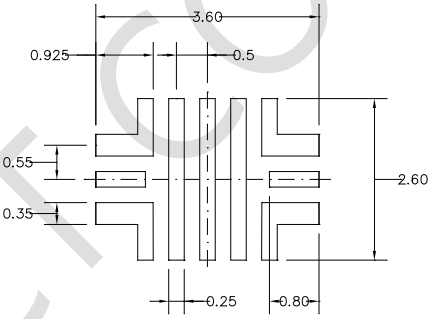
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

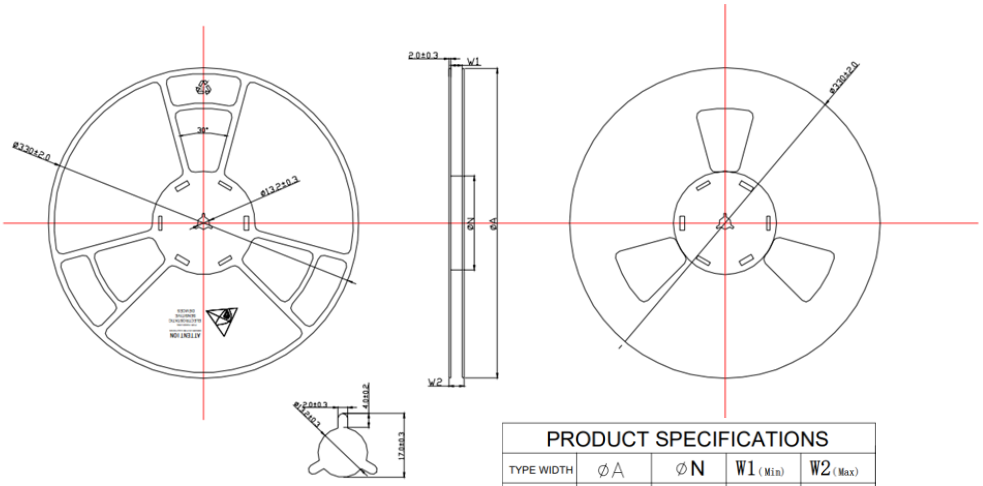
NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) DRAWING CONFIRMS TO JEDEC MO-220.
6) DRAWING IS NOT TO SCALE.

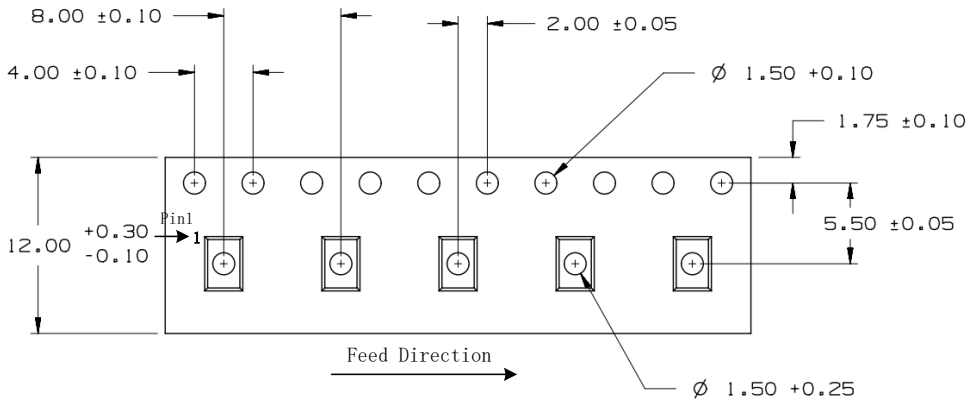
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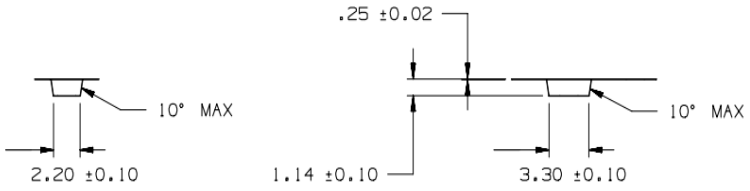
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TAPE AND REEL INFORMATION



PRODUCT SPECIFICATIONS				
TYPE WIDTH	ØA	ØN	W1 (Min)	W2 (Max)
12MM	330±2.0	100±1.0	12.4	19.4
16mm	330±2.0	100±1.0	16.4	23.4
24MM	330±2.0	100±1.0	24.4	31.4
32MM	330±2.0	100±1.0	32.4	39.4
44MM	330±2.0	100±1.0	44.4	51.4





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