2.7V-6V Vin 15A Synchronous Step Down Convertor

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
- Input Voltage Range: 2.7V-6V
- Up to 15A Continuous Output Current
- Four Output Voltage Ranges:
  – 0.4V to 0.71875V in 1.25mV steps
  – 0.4V to 1.0375V in 2.5mV steps
  – 0.4V to 1.675V in 5mV steps
  – 0.8V to 3.35V in 10mV steps
- Output Voltage Accuracy ±1%
- Integrated 6mΩ High-Side and 3mΩ Low-Side Power MOSFETs
- Resistor-selectable Start-up Output Voltage
- Resistor-selectable Switching Frequency
- Selectable PFM or FCCM Operation
- Programmed Soft-start/Soft-stop Time
- Differential Remote Voltage Sensing
- Active Output Discharge
- Power Good Indicator
- Integrated Frequency Dither for EMI Mitigation
- Factory-Configurable Multi-Page One-Time Programmable (OTP) Memory
- Integrated Protection Feature
  - Cycle-by-cycle current limit
  - Under-voltage Lockout
  - Input over-voltage Protection
  - LIMIT or HICCUP Over Current Protection
  - Thermal Warning and Thermal Shutdown Protection
- FCLGA-16L 2.55mm*3.55mm Package
- Available in a Wettable Flank Package

APPLICATIONS

- Infotainment and cluster
- Advanced Driver Assistance Systems (ADAS)
- FPGA, ASIC, and digital core supply

DESCRIPTION

The SCT21F0Q is a monolithic, step-down switch-mode converter with built-in internal 6mΩ High-Side and 3mΩ Low-Side Power MOSFETs. The device achieves 15A of continuous output current from a 2.7V to 6V input voltage range, with excellent load and line regulation. The output voltage can be regulated to as low as 0.4V.

The SCT21F0Q, adopting the constant-on time (COT) mode control provides fast transient response and eases loop stabilization, greatly simplifies the converter off-chip configuration. The switching clock frequency can be selected from 1.1MHz, 2.2MHz, 2.5MHz and 3MHz for optimization of the filter size and output voltage ripple. The frequency dither option minimizes radiated electromagnetic emission.

The SCT21F0Q has a MODE/SYNC pin to select Pulse Frequency Modulation (PFM) operation mode to achieve the light load power save or Forced Continuous Conduction Mode (FCCM) to achieve low light load ripple.

The SCT21F0Q has an optional remote sensing feature that maximizes voltage regulation at the point-of-load, and the device achieves better than ±1% output voltage accuracy under all operating conditions. The I^2C interface supports dynamic voltage adjustment with programmable slew rates to balance performance and power consumption.

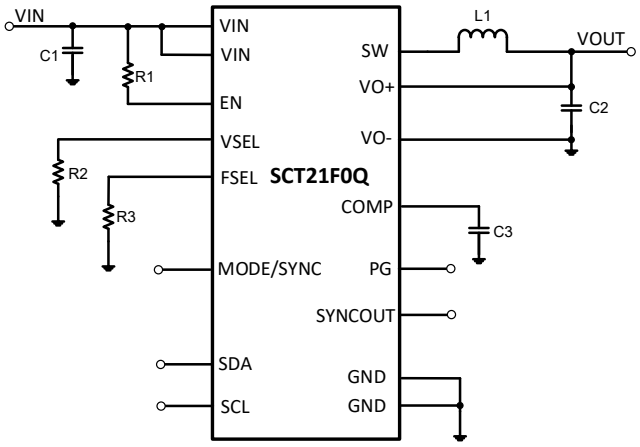
It includes full protection features, such as cycle-by-cycle current limit and hiccup over current protection, output under-voltage protection, input under-voltage lockout and over-voltage protection, and thermal shutdown.

The SCT21F0Q requires a minimal number of external components and is available in a space-saving FCLGA-16L 2.55mm*3.55mm package with Wettable Flank.

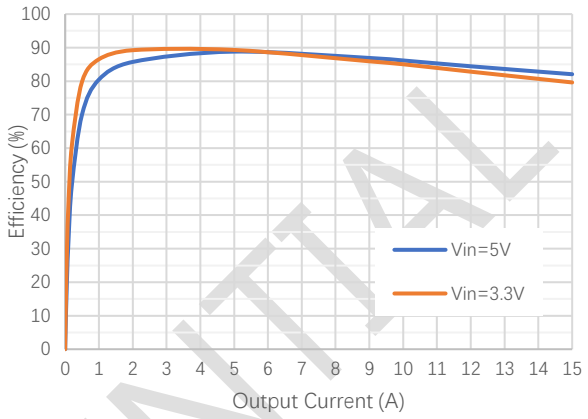
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TYPICAL APPLICATION



2.7V-6V, Synchronous Buck Converter



Efficiency, Vout=0.875V, Fsw=2.2MHz, FCCM mode

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 0.8: Customer sample.

DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL
SCT21F0QLLDR	Tape & Reel	3000	21F0Q	16	FCLGA2.55X3.55-16L	3

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted (1)

DESCRIPTION	MIN	MAX	UNIT
VIN	-0.3	6.5	V
SW	-0.3	VIN+0.3	V
SW (Pulse<10ns)	-3	10	V
VO+	-0.3	3.8	V
VO-	-0.3	0.3	V
SCL, SDA	-0.3	5	V
FSEL, VSEL, EN, MODE/SYNC, SYNCOUT, COMP, PG	-0.3	6.5	V
Operating junction temperature T_J(2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

PIN CONFIGURATION

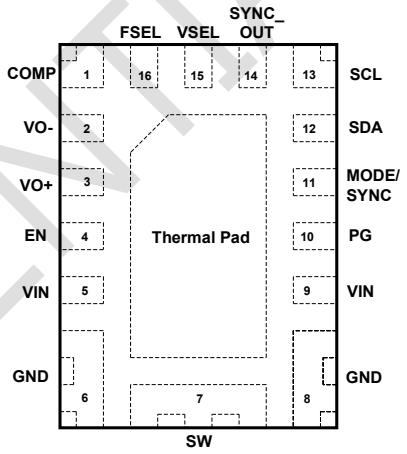


Figure 1:Top View FCLGA2.55X3.55-16L

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
COMP	1	Device compensation input pin. A capacitor from this pin to GND defines the compensation of the control loop. It recommends to add 2.2nF between these two pins.
VO-	2	Output ground sense pin. (differential output ground sensing)
VO+	3	Output voltage sense pin. (differential output voltage sensing)
EN	4	Enable logic input. Logic low disables the device, logic high enables the device. The user must connect to this pin using a series resistor of at least 20kΩ. Do not leave this pin unconnected.
VIN	5, 9	Power supply input pin. Decouple the input rail with at least 0.1uF input ceramic capacitor. Place the capacitor as close as to VIN and GND pins as possible.
GND	6, 8	Ground pin.
SW	7	Switching node pin. SW is driven up to VIN through the high-side power MOSFET during on-time. The inductor current drives SW to negative voltage through low-side power MOSFET during off-time. Use wide and short PCB traces to make the connection. Keep the SW pattern area minimized.

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PG	10	Power-good indicator pin. An open-drain output which goes low if VOUT is below or above threshold voltage. Connect a pull up resistor to the system voltage rail. This pin can be left open when not used.
MODE/SYNC	11	PFM and FCCM mode selected pin. Connect the pin high to force the device in Forced Continuous Conduction Mode (FCCM) operation mode. Connected the pin low to operate the device in Pulse Frequency Modulation (PFM) mode. The mode pin can also be used to synchronize the device to an external clock.
SDA	12	Serial data line pin. Open-Drain I/O, connect this pin to high level with a pull-up resistor.
SCL	13	Serial clock line pin. Connect this pin to high level with a pull-up resistor.
SYNC_OUT	14	Internal clock output pin for synchronization. Leave this pin floating when not used. SYNCOUT outputs a 140° out-of-phase clock to the other devices.
VSEL	15	Start-up output voltage and I^2C address select pin. A resistor or short circuit to GND or VIN defines the startup output voltage and I2C address.
FSEL	16	Frequency selects pin. A resistor or a short circuit to GND or VIN determines the free-running switching frequency.
Exposed Thermal Pad		The thermal pad must be soldered to GND to achieve an appropriate thermal resistance and for mechanical stability.

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RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	2.7	6	V
V_{OUT}	Output voltage range	0.4	3.35	V
T_J	Operating junction temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per AEC-Q100-002, all pins(1)	-2	+2	kV
	Charged Device Model (CDM), per AEC-Q100-011, all pins (1)	-1	+1	kV

(1) HBM and CDM stressing are done in accordance with the AEC-Q100 specification.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	FCLGA2.55X3.55-16L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	TBD	°C/W
$R_{\theta JC(top)}$	Junction to case (top) thermal parameter(1)	TBD	
$R_{\theta JB}$	Junction-to-board thermal resistance(1)	TBD	
Ψ_{JT}	Junction-to-top characterization parameter (1)	TBD	
Ψ_{JB}	Junction-to-board characterization parameter (1)	TBD	
$R_{\theta JC(bot)}$	Junction to case (bot) thermal parameter(1)	TBD	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT21F0Q is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT21F0Q. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

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ELECTRICAL CHARACTERISTICS

V_{IN}=5V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		2.7		6	V
V_{IN_UVLO}	Input UVLO	V_{IN} rising		2.6		V
	Hysteresis			100		mV
I_{SD}	Shutdown current	EN=0V		30		uA
I_Q	Quiescent current from VIN	EN=high, no load, no switching		1.6		mA
		EN=high, Vo=0.875V,L=0.16uH, no load, switching, PFM mode(1)		2		mA
V_{OUT}	Output accuracy	V_{IN}≥V_{OUT}+1.4V	-1		1	%
I_{IB_VO-}	Input bias current (VO-)	VO- = –100mV to 100mV	-6			uA
I_{IB_VO+}	Input bias current (VO+)	VO+ = 3.3V, VIN =6V			6	uA
V_{ICR}	Input common-mode range (VO-)		-60		100	mV
I_{DIS}	Output discharge current in constant current mode	VO+=2V		100		mA
R_{DIS}	Output discharge resistance in resistive discharge mode	VO+≤0.5V			6	Ω
V_{OVP}	Input overvoltage threshold			6.3		V
	Hysteresis			100		mV
EN & Interface						
V_{ENH}	High-level Threshold voltage			1		V
V_{ENL}	Low- level Threshold voltage			0.9		V
I_{ENH}	High-level input current	V_{EN}=5V			200	nA
I_{ENL}	Low-level input current	V_{EN}=0V	-200			nA
V_H	High-level input voltage (SDA, SCL, MODE/SYNC, VSEL, FSEL, SYNC_OUT)		0.8			V
V_L	Low-level input voltage (SDA, SCL, MODE/SYNC, VSEL, FSEL, SYNC_OUT)				0.4	V
V_{L_SDA}	Low-level output voltage (SDA)	I_{OL}=3mA			0.4	V
I_{OH}	High-level output current (SDA, SCL)	V_{OH}=3.3V			200	nA
$I_{IL_MODE/SYNC}$	Low-level input current (MODE/SYNC)	V_{IL}=0V	-150		150	nA
$I_{IH_MODE/SYNC}$	High-level input current (MODE/SYNC)	V_{IH}=V_{IN}			3	uA
$I_{IL_SYNC_OUT}$	Low-level input current (SYNC_OUT)	V_{IL}=0V	-250			nA
$I_{IH_SYNC_OUT}$	High-level input current (SYNC_OUT)	V_{IH}=2V			150	nA
t_{EN_delay1}	Enable delay time when EN connects to VIN	Measured from when EN goes high to when device starts switching		270	500	us
t_{EN_delay2}	Enable delay time when EN supply external signal	Measured from when EN goes high to when device starts switching			200	us
t_{ss}	Output voltage soft-start time		0.35	0.5	0.65	ms

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SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
		Measured from when device starts switching to rising edge of PG	0.7	1	1.3	ms
			1.4	2	2.4	ms
			2.8	4	5.2	ms
R_{up}	Internal pullup resistance (VSEL, FSEL)		5.5		9	kΩ
R_{down}	Internal pulldown resistance (VSEL, FSEL)		1.3		2.2	kΩ
V_{PGTL}	Power Good Lower Threshold voltage	Vo rinsing(Reference to VSET)	94	96	98	%
		Vo falling(Reference to VSET)	92	94	96	%
V_{PGTH}	Power Good Upper Threshold voltage	Vo rinsing(Reference to VSET)	104	106	108	%
		Vo falling(Reference to VSET)	102	104	106	%
V_{OL_PG}	Low-level output voltage (PG)	I_{OL}=1mA			0.3	V
I_{OH_PG}	High-level output current (PG)	V_{OH} =3.3V			200	nA
t_{d_PG}	Deglitch time (PG)	High-to-low or low-to-high transition on the PG pin	40	50	60	us
Power switch						
R_{HS}	High-side switch on resistance	V_{IN}=3.3V		6		mΩ
R_{LS}	Low-side switch on resistance	V_{IN}=3.3V		3		mΩ
$I_{SW\ off_HS}$	High-side FET off-state current	VIN=6V,V_{SW}=0V, Tj=25°C	-1			uA
$I_{SW\ off_LS}$	Low-side FET off-state current	VIN=6V,V_{SW}=6V, Tj=25°C			100	uA
$ILIM_{HS}$	High-side peak current limit			24		A
$ILIM_{LS}$	Low-side valley current limit			20		A
$I_{_LSZC}$	LS zero cross current threshold, PFM mode			100		mA
$ILIM_{_LSNOC}$	LSD negative current limit	From drain to source		10		A
Switching Frequency						
F_{SW}	Switching frequency	FSEL pin short to GND		1.1		MHz
		FSEL pin connect 6.2kΩ to GND		2.2		MHz
		FSEL pin connect 47kΩ to VIN		2.5		MHz
		FSEL pin short to VIN		3		MHz
F_{SS_PERIOD}	Frequency spread spectrum period			Fsw/ 2048		kHz
F_{SS_RANGE}	Frequency spread spectrum in percentage of Fsw			±10		%
t_{ON_MIN}	Minimum on-time			40		ns
t_{OFF_MIN}	Minimum off-time			80		ns
Protection						
T_W	Thermal warning threshold			150		°C
	Hysteresis			20		°C
T_{SD}	Thermal shutdown threshold			170		°C
	Hysteresis			20		°C
I²C Interface						
V_{IH}	High-level input voltage		1.2			V
V_{IL}	Low-level input voltage				0.4	V
V_{OL}	Low-level output voltage	I_{SINK}=4mA			0.4	V
F_{SCL}	SCL clock frequency				1	MHz

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SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
T_{LOW}	Low period of the SCL clock		500			ns
T_{HIGH}	High period of the SCL clock		260			ns
T_{HD_STA}	Hold time (repeated) START condition		260			ns
T_{SU_STA}	Set-up time (repeated) START condition		260			ns
T_{HD_DAT}	Data hold time		0			ns
T_{SU_DAT}	Data set-up time		50			ns
T_R	Rise time of both SCL and SDA signals				120	ns
T_F	Fall time of both SCL and SDA signals				120	ns
T_{SU_STO}	Set-up time for STOP condition		260			ns
C_B	Capacitive load for each bus line				550	pF

Notes:
1) Guaranteed by sample characterization. Not tested in production.

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TYPICAL CHARACTERISTICS

V_{IN}=5V, L=0.16uH, fsw=2.2MHz, V_{OUT}=0.875V, FCCM mode, unless otherwise noted.

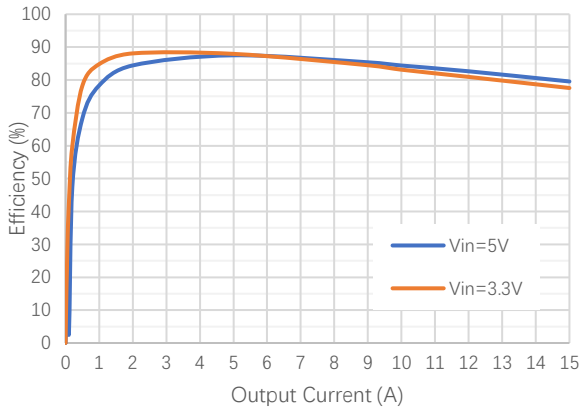


Figure 2. Efficiency vs Load Current, Vout=0.75V

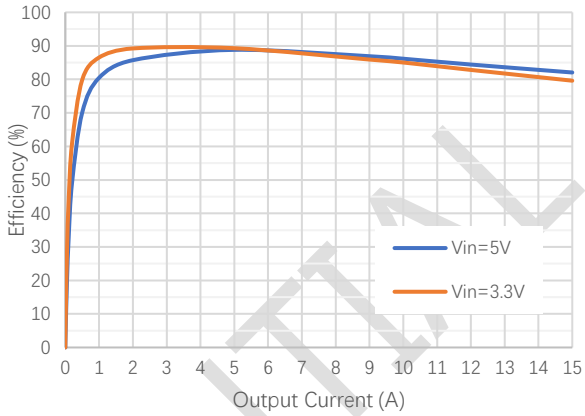


Figure 3. Efficiency vs Load Current, Vout=0.875V

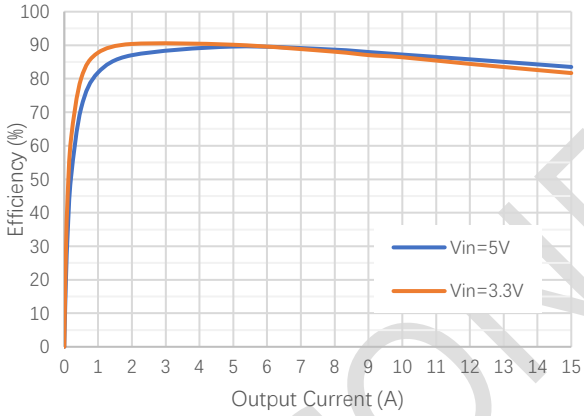


Figure 4. Efficiency vs Load Current, Vout=1V

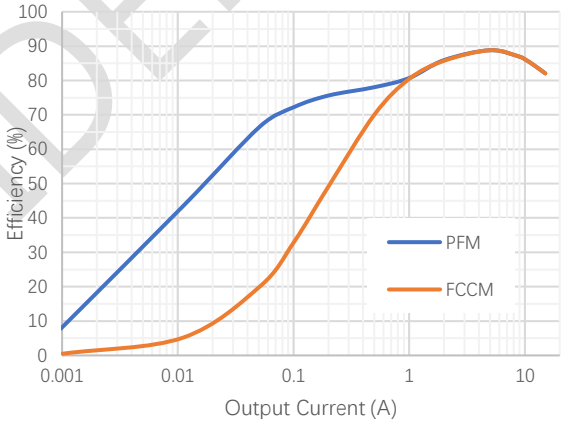


Figure 5. Efficiency vs Mode, Vin=5V, Vout=0.875V

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FUNCTIONAL BLOCK DIAGRAM

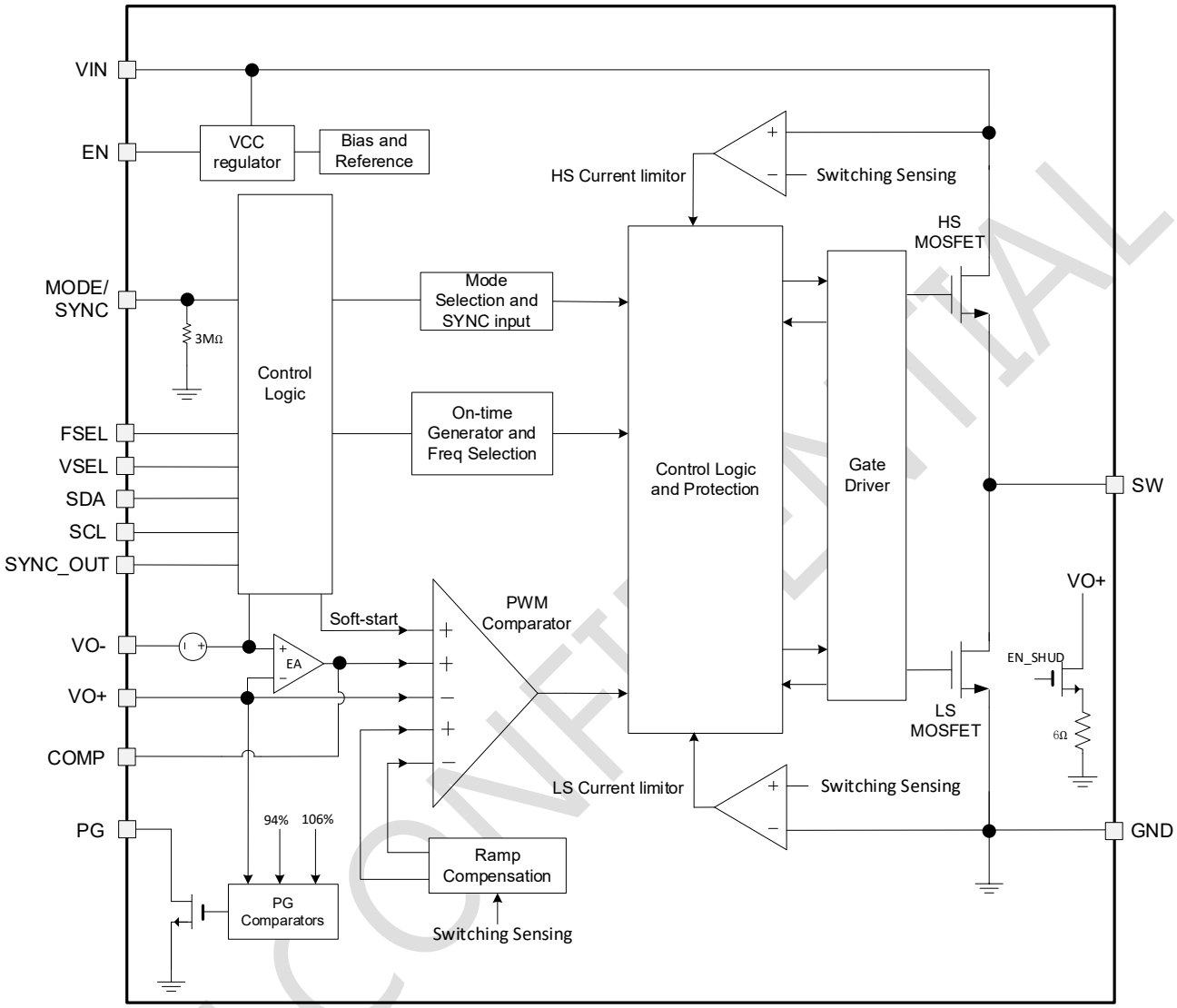


Figure 8. Functional Block Diagram

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OPERATION

Overview

The SCT21F0Q is a 2.7V-6V input, 15A output, synchronous buck converter with built-in 6mΩ Rdson high-side and 3mΩ Rdson low-side power MOSFETs. It implements Constant on-time (COT) mode control to regulate output voltage, providing excellent line and load transient response and simplifying the external frequency compensation design.

The switching frequency is selectable, 1.1MHz, 2.2MHz, 2.5MHz and 3MHz, by setting different FSEL status, to optimizes either the power efficiency or the external components' sizes. The device features two different operation modes at light loading: Pulse Frequency Modulation (PFM) mode and Forced Continuous Conduction Mode (FCCM) . The quiescent current is typically 1.6mA under no load and PFM mode condition to achieve high efficiency at light load.

The SCT21F0Q full protection features include the input under-voltage lockout, input over-voltage, over current protection with current limit and hiccup mode, output hard short protection and thermal shutdown protection.

Constant On-time Control

The SCT21F0Q employs Constant on-time (COT) mode control providing fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET is turned on a fixed on-time period. The one on-time is calculated by the converter's input voltage (VIN) and the output voltage (VOUT) cycle-by-cycle based to maintain a pseudo-fixed frequency over the input voltage range. SCT21F0Q turns off high-side MOSFET after the fixed on-time and turns on the low-side MOSFET. SCT21F0Q turns off the low-side MOSFET once the output voltage dropped below the output regulation, the one-shot timer then reset and the high-side MOSFET is turned on again. The on-time is inversely proportional to the input voltage and proportional to the output voltage. It can be calculated using the following Equation 1:

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_S} \quad (1)$$

Where:

- VOUT is the output voltage.
- VIN is the input voltage.
- fs is the switching frequency.

After an on-time period, the regulator goes into the off-time period. The off-time period length depends on internal reference voltage in most cases. It will end when the VO+ pin voltage decreases below internal reference voltage, at which point the on-time period is triggered. If the off-time period is less than the minimum off time, the minimum off time will be applied, which is around 80ns typical.

MODE/SYNC

The MODE/SYNC pin combines operate mode control and frequency synchronization. The SCT21F0Q works in PFM mode in light load when set MODE/SYNC pin low and operates in forced continuous conduction mode when the MODE_SYNC pin is set high. If an external clock frequency is applied on the MODE/SYNC pin, the switching frequency will be synchronized to the external clock frequency and the device will operate in forced continuous current mode. The external frequency must be selected in the frequency range as below:

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			MIN	NOM	MAX	UNIT
F_{SYNC}	Synchronization clock frequency range (MODE/SYNC)	Nominal f_{SW} = 1.1 MHz	0.8		1.8	MHz
F_{SYNC}	Synchronization clock frequency range (MODE/SYNC)	Nominal f_{SW} = 2.2 MHz	1.7		2.7	MHz
F_{SYNC}	Synchronization clock frequency range (MODE/SYNC)	Nominal f_{SW} = 2.5 MHz	2		3	MHz
F_{SYNC}	Synchronization clock frequency range (MODE/SYNC)	Nominal f_{SW} = 3 MHz	2.5		3.3	MHz
D_{SYNC}	Synchronization clock duty cycle range (MODE/SYNC)		45		55	%

Pulse Frequency Modulation (PFM) Mode

Grounding the MODE/SYNC pin makes the SCT21F0Q work at Pulse Frequency Modulation (PFM) mode to improve the power efficiency in light load. As the output current decreases from heavy load condition, the inductor current is also reduced. If the output current is reduced, the valley of the inductor current reaches the zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The low-side MOSFET is turned off when a zero inductor current is detected. As the load current further decreases the converter runs into discontinuous conduction mode.

Forced Continuous Conduction Mode (FCCM)

Connecting MODE/SYNC pin to VIN, the SCT21F0Q forces the device operating at Forced Continuous Conduction Mode (FCCM) with pseudo-fixed switching frequency regardless of loading current. Operating in FCCM mode can achieve smaller output voltage ripple compared with PFM at light load. When the load current approaches zero, the low-side MOSFET current crosses zero and sinks current from output to maintain the constant output. Hence power efficiency in light load is much lower than heavy load.

Table 1 shows the function table of the MODE/SYNC pin and the FCCM_EN bit in the CTL1 register, which control the operating mode of the device

Table 1. FCCM and PFM Selection

MODE/SYNC Pin	FCCM_EN Bit	Operating Mode
Low	0	PFM
	1	FCCM
High	X	FCCM
SYNC	X	FCCM

Switching Frequency Selection

The switching frequency of the SCT21F0Q is selectable to be one of three options: 1.1MHz, 2.2MHz, 2.5MHz and 3MHz. The switching frequency selection is programmed by FSEL pin. The selection information is shown in following table. The frequency setting is latched in at each power up and is not modified during operation. Cycling the input power or the EN pin can reselect the switching frequency.

Table 2. FSEL Pin Set-up for Switching Frequency Selection

FSEL Pin Set-up	FSEL pin short to GND	FSEL pin connects 6.2kΩ to GND	FSEL pin connects 47kΩ to VIN	FSEL pin short to VIN
Switching Frequency	1.1MHz	2.2MHz	2.5MHz	3MHz

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Enable (EN) Function

EN is a digital control pin that can turn the regulator on and off. When EN is pulled below the falling threshold voltage (0.9V), the chip shuts down. Force EN above its rising threshold voltage (1V) to turn the part on. Leave EN floating or pull it down to ground to disable the SCT21F0Q. When the EN pin pulls up to VIN, the device first loads the default register settings from nonvolatile memory and reads the state of the VSEL, FSEL pins and then start up. The t_{EN_delay1} time is from VIN higher than rising UVLO to soft start . The device also keeps shutdown when triggering such as thermal shutdown or overvoltage lockout occur during this delay time.

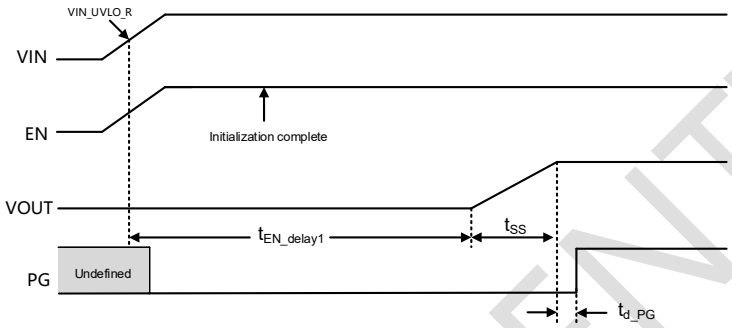


Figure 9. Start-Up with EN pin is Pulled Up to VIN

When power is first applied to the VIN pin and EN pin is supplied from external signal, the device has loaded the default register settings from nonvolatile memory and reads the state of the VSEL, FSEL pins after Vin UVLO. The t_{EN_delay2} time is from EN pin enables to soft start. The device also keeps shut down when triggering such as thermal shutdown or overvoltage lockout occur during this delay time.

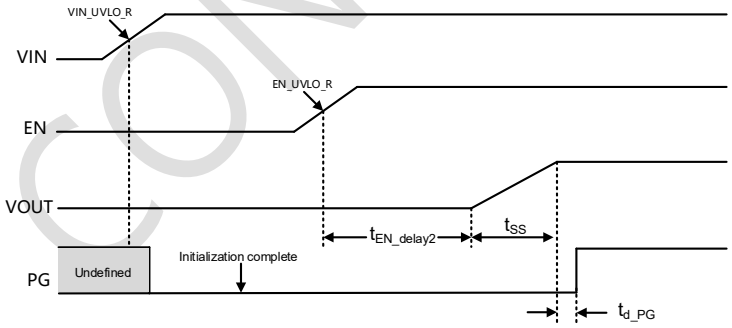


Figure 10. Start-Up with EN pin is Pulled Up to External Signal

Soft Start(SS)

The SCT21F0Q can be programmed the output voltage slew rate to avoid overshoot at startup by register CTL2[1:0] SS_TIME bits. The soft-start time (tss) have 4 options as below:

Table 3. Soft-start time Selection

CTL2[1:0] SS_TIME	SS time(ms)
00	0.5
01	1(default)

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10	2
11	4

The device ignores new values until the soft-start sequence is complete if the user programs the following when the device soft-start sequence has already started:

• A new output voltage setpoint (CTL0[7:0] VOUT_SET)

• An output voltage range (CTL2[3:2] VOUT_RANGE)

• Soft-start time (CTL2[1:0] SS_TIME) settings

If the user changes the value of CTL0[7:0] VOUT_SET during soft start, the device first ramps to the value that CTL0[7:0] VOUT_SET had when the soft-start sequence began. Then, when soft start is complete, the device ramps up or down to the new value.

The device can start up into a pre-bias output. In this case, only a portion of the internal voltage ramp is seen externally.

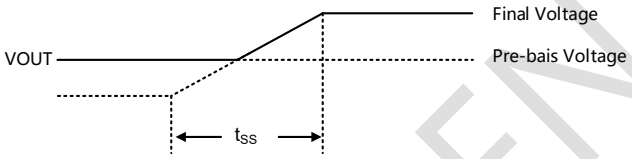


Figure 11. Start-Up with Vo pre-bias voltage

Output Discharge and Soft Stop

The SCT21F0Q also has an output discharge function that makes sure output voltage decreases to 0V when the device is shutdown. This function is enabled by default and can be controlled by the register CTL1[3] DISCH_EN bit. If this bit enables, the SCT21F0Q will discharge output as below conditions:

1) A low level is applied to the EN pin.

2) SW_EN = 0 in the CTL1 register.

3) A thermal shutdown event occurs.

4) A UVLO event occurs.

5) A OVLO event occurs.

The SCT21F0Q also has soft-stop function, this function is disabled by default and can be controlled by the register CTL2[4] SOFT-STOP_EN bit. The output voltage is ramped down at the same as programmed soft-start time when enable this bit. The SCT21F0Q operates in FCCM during the soft-stop period and only EN pin pulls low or SW_EN bit=0 can trigger soft-stop.

Output Voltage

The SCT21F0Q can be set up output voltage by register CTL0[7:0] VOUT_SET and CTL2[3:2] VOUT_RANGE. The device has 4 output range options as below:

Table 4. Output range option

CTL2[3:2] VOUT_RANGE	VOUT_RANGE
00	0.4V to 0.71875V in 1.25mV steps
01	0.4V to 1.0375V in 2.5mV steps
10	0.4V to 1.675V in 5mV steps(default)
11	0.8V to 3.3 V in 10mV steps

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Note:

1) Every change to the CTL2[3:2] VOUT_RANGE bits must be followed by a write to the CTL0[7:0] VOUT_SET register, even if the value of the CTL0[7:0]VOUT_SET bits does not change. This sequence is required for the device to start to use the new voltage range.

2) The 0.8V to 3.35V range uses a 0.8V reference and the other ranges use a 0.4V reference. Switching from the 0.8V to 3.35V range can therefore cause increased output voltage undershoot or overshoot while the device switches the internal reference.

After choosing the output voltage range by the register CTL2[3:2] VOUT_RANGE, the CTL0[7:0] VOUT_VSET register can configure the output voltage.

Table 5. Output Voltage setting

CTL2[3:2] VOUT_RANGE	Output voltage set
00	0.4V + VOUT_SET[7:0] × 1.25mV
01	0.4V + VOUT_SET[7:0] × 2.5mV
10	0.4V + VOUT_SET[7:0] × 5mV
11	0.8V + VOUT_SET[7:0] × 10mV

During initialization, the device reads the state of the VSEL pin and selects the default output voltage as below:

Table 6. VSEL Pin Set-up default output voltage and I²C address

VSEL Pin Set-up	VSEL pin short to GND	VSEL pin connect 6.2kΩ to GND	VSEL pin connect 47kΩ to VIN	VSEL pin short to VIN
Output voltage	0.8V	0.75V	0.875V	1V
I²C address	0x40	0x41	0x42	0x43

If the user programs new output voltage setpoint (CTL0[7:0] VOUT_SET), output voltage range (CTL2[3:2] VOUT_RANGE), or soft-start time (CTL2[1:0] SS_TIME) settings when the device has already begun the soft-start sequence, the device ignores the new values until the soft-start sequence is complete.

If the user changes the value of CTL0[7:0]VOUT_SET during soft start, the device first ramps to the value that CTL0[7:0] VOUT_SET had when the soft-start sequence began. Then, when soft start is complete, ramps up or down to the new value. If the user changes CTL0[7:0] VOUT_SET, CTL1[1:0]VOUT_SLEW RATE, or CTL2[1:0] SS_TIME while EN is low, the device uses the new values the next time the user enables the device.

Dynamic Voltage Scaling (DVS)

The SCT21F0Q has dynamic voltage scaling (DVS) to allow loads to margin their supply voltage. The device can set the VOUT slew rate when change from one voltage to the another by CTL1[1:0] VOUT_SLEW RATE as below:

Table 7. Dynamic Voltage Scaling Slew Rate

CTL1[1:0] VOUT_SLEW RATE	DVS Slew Rate
00	10mV/μs
01	5mV/μs
10	1.25mV/μs
11	0.5mV/μs

When ramping the output to a higher voltage requires additional output current, so that during DVS, the converter must generate a total output current given by:

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$$I_{OUT} = I_{OUT(DC)} + C_{OUT}\frac{dV_{OUT}}{dt} \quad (1)$$

Where:

- I_{OUT} is the total current the converter must generate while ramping to a higher voltage.
- $I_{OUT(DC)}$ is the DC load current.
- C_{OUT} is the total output capacitance.
- dV_{OUT}/dt is the slew rate of the output voltage (programmable by register VOUT_SLEW RATE).

Generally, make sure that the total output current during DVS does not exceed the current limit of the device.

Compensation (COMP)

The COMP pin is the connection point for an external compensation network to optimize the loop response for a wide range of operating conditions. A 2.2nF capacitor to GND pin is sufficient for typical applications.

Frequency Spread Spectrum (FSS)

The SCT21F0Q has Frequency Spread Spectrum (FSS) to minimize the peak emissions at a specific frequency. When the FSS function is enabled, the spread spectrum operation frequency span is ±10% nominal value and the frequency modulation have a fsw/2048 triangular wave as below:

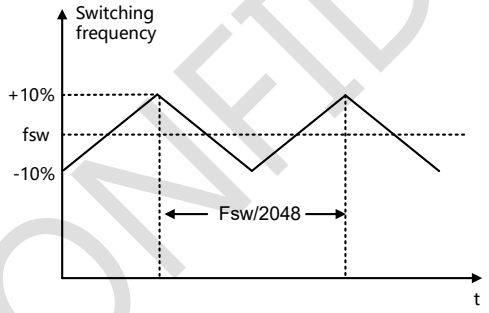


Figure 12. Frequency Spread Spectrum

Under Voltage Lockout UVLO

The SCT21F0Q Under Voltage Lock Out (UVLO) default startup threshold is typical 2.6V with VIN rising and shutdown threshold is 2.5V with VIN falling. If the supply voltage decreases below this value, the device stops switching and, if CTL1[2] DISCH_EN = 1, turns on the output discharge.

Over Voltage Lockout OVLO

The SCT21F0Q Over Voltage Lock Out (OVLO) functions to protect the device damage when supply voltage is too high. The OVLO rising threshold is typical 6.3V. If the supply voltage increases above this value, the device stops switching and, if CTL1[2] DISCH_EN = 1, turns on the output discharge.

The SCT21F0Q can automatically recover when supply voltage falls below 6.2V. The device will start switching again with a new soft-start sequence.

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Over Current Protection (OCP)

In each switching cycle, the inductor current is sensed by monitoring the high-side MOSFET during the ON period and the low-side MOSFET during the OFF period. When the inductor current (IL) reaches the high-side MOSFET peak current limit (typically 24A) during the ON period, the high-side MOSFET is forced off immediately to prevent the current from rising further. Then the low-side MOSFET turns on, and stays on until IL drops below the low-side MOSFET valley current limit (typically 20A).The high-side MOSFET switch again if the inductor current has decreased below the low-side MOSFET valley current limit threshold.

The SCT21F0Q has two OCP operation modes: HICCUP Mode and Current Limit Mode.

To enable Hiccup Mode operation, make sure that CTL1[2] HICCUP_EN=1. When the low-side switch current exceeds the current limit threshold on 32 consecutive switching cycles, the device will stop switching for 128us and then automatically starts switching again with a new soft-start sequence. PG pin will be pulled low and STATUS register HICCUP bit will be set 1. The device clears the HICCUP bit if the user reads the STATUS register and PG pin pull high again when the overload condition has been removed.

To enable Current Limit Mode operation, make sure that CTL1[2] HICCUP_EN=0. The device limits the low-side switch current cycle-by-cycle for as long as the overload condition exists. If the device limits the low-side switch current for four or more consecutive switching cycles, the device sets ILIM = 1 in the STATUS register. The device clears the ILIM bit if the user reads the STATUS register when the overload condition has been removed.

Power Good Indicator

The SCT21F0Q has one power good (PG) output to indicate normal operation after the soft-start time. PG is the open drain of an internal MOSFET, which has a maximum $R_{DS(ON)}$ below 200Ω. PG can be connected to VIN or an external voltage source through an external a resistor (e.g., 100kΩ). After the input voltage is applied, the MOSFET turns on, and PG is pulled to GND before soft start is ready.

The PG pin is open-drain output that indicates the status of the converter. When the output voltage is either less than 94% (typical) or greater than 106% (typical) of the nominal output voltage. The output of the window comparator will drive the open-drain PG pin to low (50us deglitch typical).

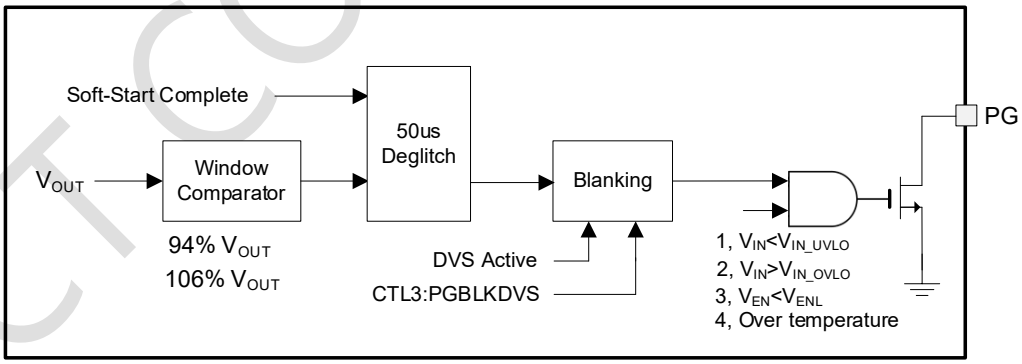


Figure 13. Power-Good Functional Block Diagram

During DVS activity, when the DC/DC converter transitions from one output voltage setting to another, the output voltage may shortly exceed the limits of the window comparator and pull the PG pin low. The device has a feature to disable this behavior when setting CTL3[0] PGBLKDVS to 1. The device ignores the output of the power-good window comparator during DVS.

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Remote Output Voltage Sensing

The remote output voltage sensing function is implemented to compensate for the voltage drop in the copper between the SCT21F0Q and the load caused by the large output current and the resistance in the transmission line as figure14. Remote sensing lets the converter sense the output voltage directly at the point-of-load and increases the accuracy of the output voltage regulation.

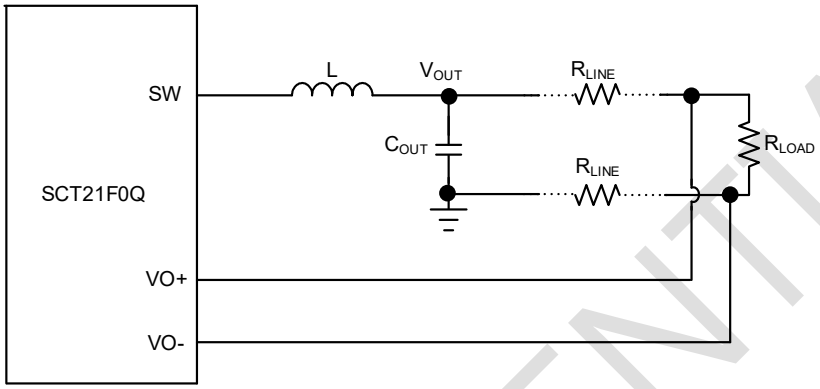


Figure 14. Remote Output Voltage Sensing Circuit

Adaptive Voltage Positioning(AVP)

The SCT21F0Q supports adaptive voltage positioning function. The output voltage stays constant when without AVP, and the output voltage droops linearly with load when AVP is enabled. This increases the headroom available for transient under and over shoots thereby resulting in a reduced output capacitor requirement. This function is disabled by default and can be controlled by the register CTL2[5] AVP_EN bit. When this bit sets to 1, the AVP slope is about 1mV/A from 0A to rated output current.

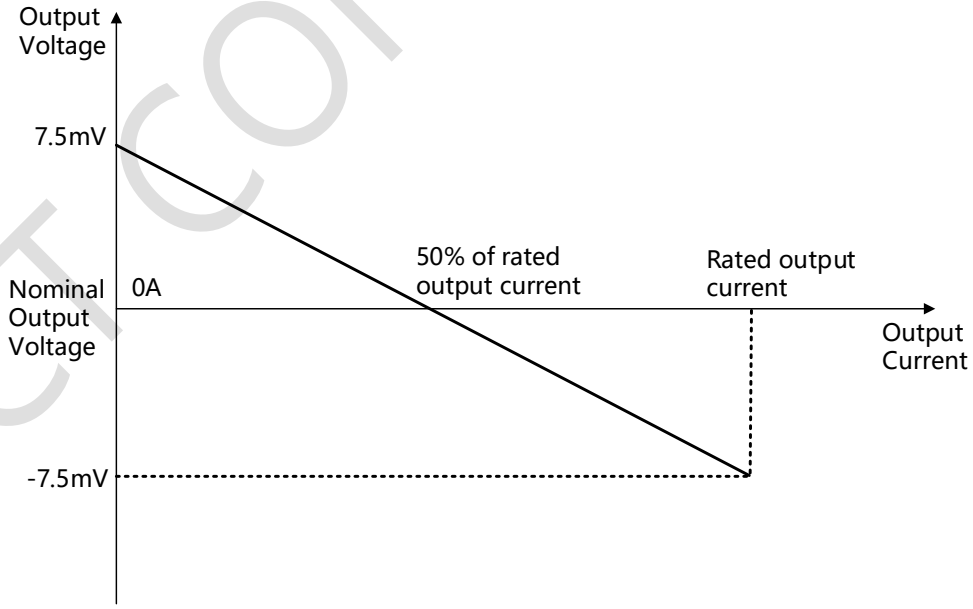


Figure 14. Adaptive Voltage Positioning

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Thermal Warning

Once the junction temperature in the SCT21F0Q exceeds 150°C, the device will set STATUS OT_WRAN bit to 1. This bit can be clear if the user reads the STATUS register when the junction temperature is below 130°C (typical).

Thermal Shutdown

Once the junction temperature in the SCT21F0Q exceeds 170°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 150°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

STATE MACHINE DESCRIPTION

The state machine of SCT21F0Q is shown in figure 15. There are six states in this device: IDEL, LOAD OTP, STANDBY, SOFT START, NORMAL, DVS, SOFT STOP. Each state is described in greater detail below.

IDLE State

The device enters IDLE state whenever VIN is lower than VIN UVLO threshold. All functional blocks are disabled and all registers are reset. The device will exit IDLE state and jump to LOAD OTP state when VIN reached its rising UVLO threshold.

LOAD OTP State

The device will load data from OTP to corresponding registers, then STANDBY state is entered.

STANDBY State

STANDBY state is where the device could be held on to check and wait for all conditions to meet power up. To exit STANDBY state, VIN shall be higher than VIN UVLO threshold, EN higher than UVLO threshold, OTP is done and no other critical fault like thermal shutdown is triggered. Once all conditions are ready, the SCT21F0Q automatically enters the soft start state.

SOFT START State

In SOFT START state, the SCT21F0Q will ramp to output voltage follow soft start time. Once the soft start is done, the SCT21F0Q will entry NORMAL state and PG pin will be pull high. If any disable or protection event occurs, the device will return to STANDBY State.

NORMAL State

NORMAL state is the normal operation state of the device with output regulator voltage is power good. The normal state is the standard operating state for the SCT21F0Q.

DVS State

In DVS state, dynamic voltage scaling (DVS) to allow loads to margin their supply voltage. The device can set the VOUT slew rate when changing from one voltage to the another by CTL1[1:0] VOUT_SLEW RATE.

SOFT STOP State

In SOFT STOP state, the SCT21F0Q will ramp down output voltage follow soft start time. Once the soft stop is done, the SCT21F0Q will entry STANDY state. SCT21F0Q works in SOFT STOP state need to set CTL2[4] SOFT-STOP_EN bit to 1 and this state is disabled default.

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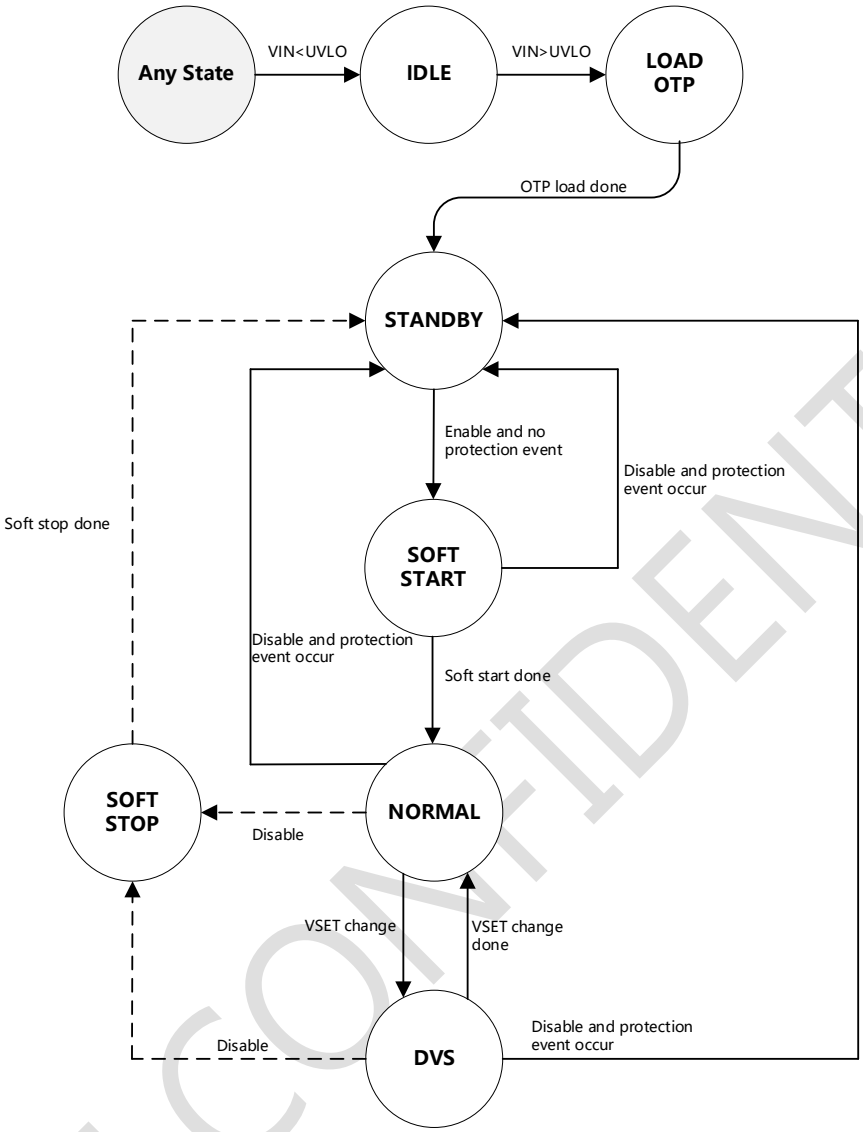


Figure 15. STATE MACHINE DESCRIPTION

I²C Interface

The SCT21F0Q integrates a two-wire serial interface for bidirectional communications between the device and the master through bus. The I²C protocol defines two bus lines, the serial data line (SDA) and the serial clock line (SCL). The SCT21F0Q is always assigned a unique chip address and operates as a slaver, the master drives the SCL line and transfer bidirectional data through SDA line. Both the SCL and SDA lines need a pull-up resistor connected to bus voltage since HIGH state is the default state when bus is idle. The SCT21F0Q supports Standard-mode (up to 100 kHz), Fast-mode (up to 400 kHz), Fast-mode Plus (up to 1 MHz). The internal filtering ignores spikes and noises on the bus line to preserve data integrity. The maximum capacitive load for each bus line is given in Electrical Characteristic thus the number of interfaces is limited.

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Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

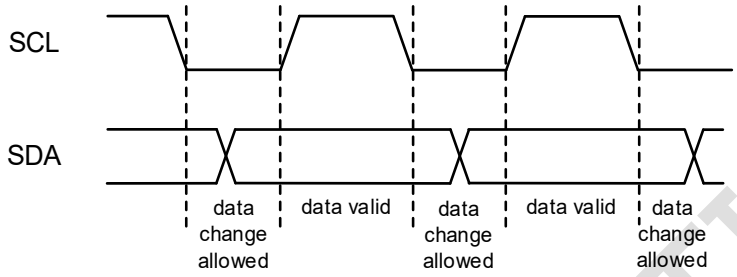


Figure 16. Data Validity Diagram

START and STOP Conditions

The data transfer always generates START and STOP conditions to announce the process. A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. Both the START and STOP conditions are generated by master on bus.

The bus is considered to be busy after START condition and released after STOP condition. A repeated START condition during transmission is also valid and will be regarded as a new START condition.

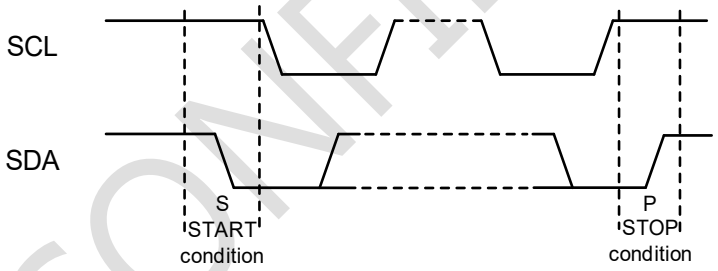


Figure 17. START and STOP Conditions Diagram

Data Transmission

The transferred byte consists of eight bits with the Most Significant Bit (MSB) first. After each byte is transferred, the master will release the SDA line and generate the ninth acknowledge clock pulse on SCL line. The SCT21F0Q will pull the SDA line LOW during this acknowledge clock, to announce a successful reception and the next byte may be sent. If the master is receiver and the last byte is received, it still generates the ninth acknowledge clock pulse but SDA line will not be pulled LOW. It's called not acknowledge signal and indicates the end of transmission. After the START condition, the master must send a slave address as the first addressing byte. The slave address is seven bits long followed by an eighth R/W bit. The R/W bit defines the data direction. Set the R/W bit to 0 to indicate write command, and a 1 indicates read command.

Write Data Format

A write to the device includes transmission of the following:

- START condition
- Slave address with the write bit set to 0
- 1 byte of data to register address

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- 1 byte of data to the command register
- STOP condition

Read Data Format

A read from the device includes the following:

- Transmission of a START condition
- Slave address with the write bit set to 0
- 1 byte of data to register address
- Restart condition
- Slave address with read bit set to 1
- 1 byte of data to the command register
- STOP condition

Figure 8 illustrates the proper format for one frame.

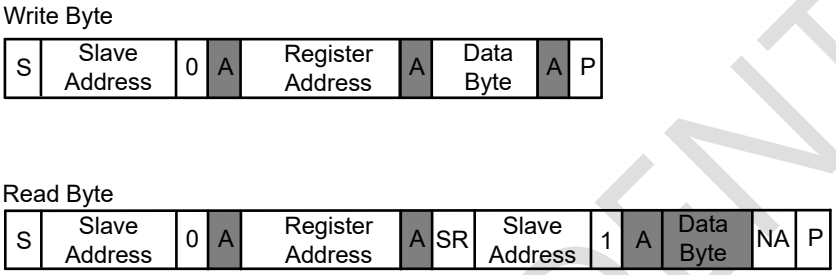


Figure 18. Transmission Data Format Diagram

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Register Map

ADD	NAME	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0x00	CTL0	R/W	VOUT_SET							
0x01	CTL1	R/W	RESET	FSS_EN	SW_EN	FCCM_EN	DISCH_EN	HICCUP _EN	VOUT_SLEW RATE	
0x02	CTL2	R/W	RESERVED		AVP_EN	SOFT-STOP_EN	VOUT_RANGE		SS_TIME	
0x03	CTL3	R/W	RESERVED							PGBLAK DVS
0x04	STATUS	R	VIN_OV	RESERVED	HICCUP	ILIM	OT_WARN	OT	PB_UV	PB_OV

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CTL0 [7:0]				
ADDRESS: 0x00				
BITS	**FIELD**	**TYPE**	**Default value**	**DESCRIPTION**
[7:0]	VOUT_SET	W/R	x	Output voltage setpoint. (See the VOUT_RANGE bits in the CTL2 register.) Range 1: Output voltage setpoint = 0.4V+VOUT_SET[7:0]×1.25mV Range 2: Output voltage setpoint = 0.4V+VOUT_SET[7:0]×2.5mV Range 3: Output voltage setpoint = 0.4V+VOUT_SET[7:0]×5mV Range 4: Output voltage setpoint = 0.8V+VOUT_SET[7:0]×10mV The state of the VSEL pin during power up determines the reset value.

CTL1 [7:0]				
ADDRESS: 0x01				
BITS	**FIELD**	**TYPE**	**Default value**	**DESCRIPTION**
[7]	RESET	W/R	0	Reset device. 0 = No effect 1 = Resets all registers to the default values and this bit auto clear to 0.
[6]	FSS_EN	W/R	0	Frequency spread spectrum clocking enable. 0 = FSS operation disabled 1 = FSS operation enabled
[5]	SW_EN	W/R	1	Software enable. 0 = Switching disabled (register values retained) 1 = Switching enabled (without the enable delay)
[4]	FCCM_EN	W/R	0	Forced continuous current operation mode enable. 0 = Power-save operation enabled 1 = Forced continuous current operation mode enable This bit is logically ORed with the MODE/SYNC pin. If a high level or a synchronization clock is applied to the MODE/SYNC pin, the device operates in FCCM, regardless of the state of this bit.
[3]	DISCH_EN	W/R	1	Output discharge enable. 0 = Output discharge disabled 1 = Output discharge enabled
[2]	HICCUPEN	W/R	0	Hiccup operation enable. 0 = Hiccup operation disabled 1 = Hiccup operation enabled.
[1:0]	VOUT_SLEW RATE	W/R	10	Output voltage slew rate when changing from one output voltage setting to another. 00 = 10 mV/μs 01 = 5 mV/μs 10 = 1.25 mV/μs 11 = 0.5 mV/μs

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CTL2 [7:0]				
ADDRESS: 0x02				
BITS	**FIELD**	**TYPE**	**Default value**	**DESCRIPTION**
[7:6]	RESERVED	R	00	/
[5]	AVP_EN	W/R	0	Output AVP enables. 0= disable AVP. 1= enable AVP, default AVP slope is about 1mV/A.
[4]	SOFT-STOP_EN	W/R	0	Output soft stop enables. The soft-stop time is same as soft start. 0= disable soft stop when IC shutdown. 1= enable soft stop when IC shutdown.
[3:2]	VOUT_RANGE	W/R	10	Output voltage range. 00 = 0.4 V to 0.71875 V in 1.25-mV steps 01 = 0.4 V to 1.0375 V in 2.5-mV steps 10 = 0.4 V to 1.675 V in 5-mV steps 11 = 0.8 V to 3.35 V in 10-mV steps
[1:0]	SS_TIME	W/R	01	Soft-start ramp time. 00 = 0.5 ms 01 = 1 ms 10 = 2 ms 11 = 4 ms

CTL3 [7:0]				
ADDRESS: 0x03				
BITS	**FIELD**	**TYPE**	**Default value**	**DESCRIPTION**
[7:1]	RESERVED	R	000000	/
[0]	PGBLNKDVS	W/R	0	Power-good blanking during DVS. 0b = PG pin reflects the output of the window comparator. 1b = PG pin is high impedance during DVS.

STATUS [7:0]				
ADDRESS: 0x04				
BITS	**FIELD**	**TYPE**	**Default value**	**DESCRIPTION**
[7]	VIN_OV	R	0	Vin OV, This bit reports whether a Vin over-voltage occurred since the last time the STATUS register was read. 0 = No Vin over-voltage event occurred 1 = A Vin over-voltage event occurred
[6]	RESERVED	R	0	/
[5]	HICCUP	R	0	Hiccup. This bit reports whether a hiccup event occurred since the last time the STATUS register was read. 0 = No hiccup event occurred 1 = A hiccup event occurred
[4]	ILIM	R	0	Current limit. This bit reports whether an current limit event occurred since the last time the STATUS register was read. 0 = No current limit event occurred 1 = An current limit event occurred

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[3]	OT_WARN	R	0	Thermal warning. This bit reports whether a thermal warning event occurred since the last time the STATUS register was read. 0 = No thermal warning event occurred 1 = A thermal warning event occurred
[2]	OT	R	0	Thermal shutdown. This bit reports whether a thermal shutdown event occurred since the last time the STATUS register was read. 0 = No thermal shutdown event occurred 1 = A thermal shutdown event occurred
[1]	PB_UV	R	1	Power-bad undervoltage. This bit reports whether a power-bad event (output voltage too low) occurred since the last time the STATUS register was read. 0 = No power-bad undervoltage event occurred 1 = A power-bad undervoltage event occurred
[0]	PB_OV	R	0	Power-bad overvoltage. This bit reports whether a power-bad event (output voltage too high) occurred since the last time the STATUS register was read. 0 = No power-bad overvoltage event occurred 1 = A power-bad overvoltage event occurred

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APPLICATION INFORMATION

Typical Application

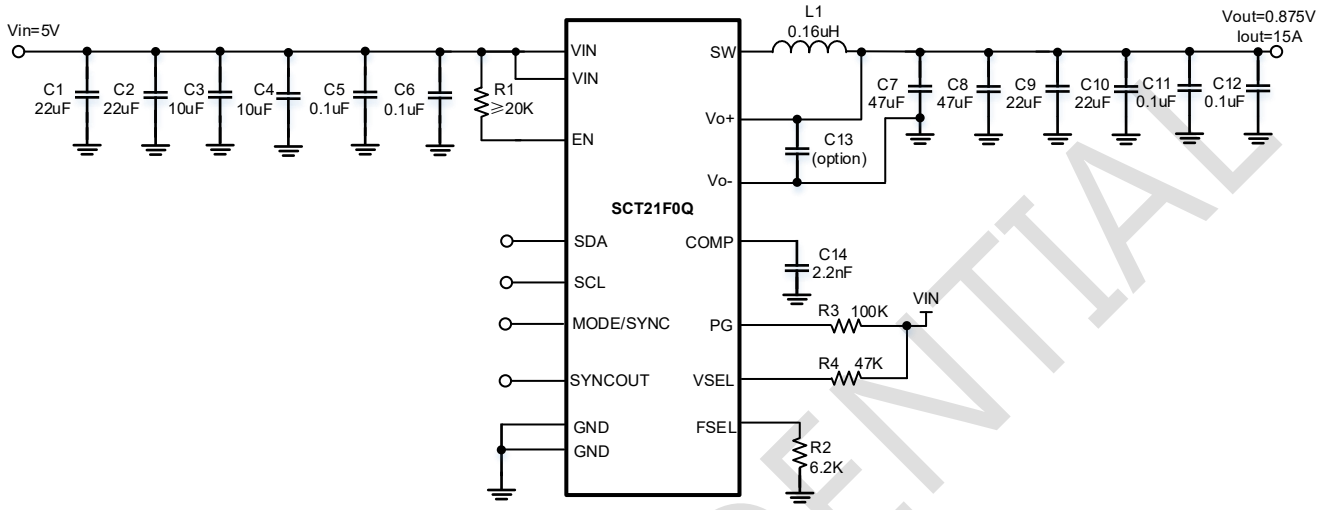


Figure 19. SCT21F0Q Design Example, 0.875V Output

Design Parameters

Design Parameters	Example Value
Input Voltage	5V Normal 2.7V to 6V
Output Voltage	0.875V
Maximum Output Current	15A
Switching Frequency	2.2MHz
Output voltage ripple (peak to peak)	5mV
Transient Response 1.5A to 13.5A load step	ΔVout =100mV

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Output Voltage

The SCT21F0Q can be set up output voltage by register CTL0[7:0] VOUT_SET and CTL2[3:2] VOUT_RANGE, VOUT c be calculated with Equation (2):

VOUT (mV) = (Reference Voltage + VOUT_SET x VOUT_RANGE-STEP) (2)

Where:

- Reference Voltage is chosen by CTL2[3:2] VOUT_RANGE: 400mV or 800mV.
- VOUT_SET range is from 0 to 255 decimal numbers, configured by CTL0[7:0] VOUT_SET.
- VOUT_RANGE-STEP is chosen by CTL2[3:2] VOUT_RANGE:1.25mV/steps, 2.5mV/steps, 5mV/steps or 10mV/steps.

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance (DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 10%~40% of the maximum output current.

The peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 3.

$$I_{LPP} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{V_{IN} * L * f_{SW}} \quad (3)$$

Where:

- I_{LPP} is the inductor peak-to-peak current.
- L is the inductance of inductor.
- f_{SW} is the switching frequency.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 4 to calculate the inductance value.

$$L_{MIN} = \frac{V_{OUT}}{f_{SW} * LIR * I_{OUT(max)}} * (1 - \frac{V_{OUT}}{V_{IN(max)}}) \quad (4)$$

Where:

- L_{MIN} is the minimum inductance required.
- f_{sw} is the switching frequency.
- V_{OUT} is the output voltage.
- $V_{IN(max)}$ is the maximum input voltage.
- $I_{OUT(max)}$ is the maximum DC load current.
- LIR is coefficient of I_{LPP} to I_{OUT}.

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in Equation 5 and Equation 6.

$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2} \quad (5)$$

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$$I_{LRMS} = \sqrt{(I_{OUT})^2 + \frac{1}{12} * (I_{LPP})^2} \quad (6)$$

Where:

- I_{LPEAK} is the inductor peak current.
- I_{OUT} is the DC load current.
- I_{LPP} is the inductor peak-to-peak current.
- I_{LRMS} is the inductor RMS current.

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 24A. The most conservative approach is to choose an inductor with a saturation current rating greater than 24A. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the SCT21F0Q can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a lower maximum output current.

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g. 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 7.

$$I_{CINRMS} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})} \quad (7)$$

The worst case condition occurs at $V_{IN}=2*V_{OUT}$, where:

$$I_{CINRMS} = 0.5 * I_{OUT} \quad (8)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 9 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} * C_{IN}} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

For this example, two 22μF and two 10uF, X7R ceramic capacitors rated for 10 V in parallel are used. And a 0.1μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

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The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 10 desired.

$$\Delta V_{OUT} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{8 * {f_{SW}}^2 * L * C_{OUT} * V_{IN}} \quad (10)$$

Where:

- ΔV_{OUT} is the output voltage ripple.
- f_{SW} is the switching frequency.
- L is the inductance of inductor.
- C_{OUT} is the output capacitance.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, two 47μF and two 22uF ceramic output capacitors work for most applications.

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Application Waveforms

V_{IN}=5V, L=0.16uH, fsw=2.2MHz, V_{OUT}=0.875V, unless otherwise noted.

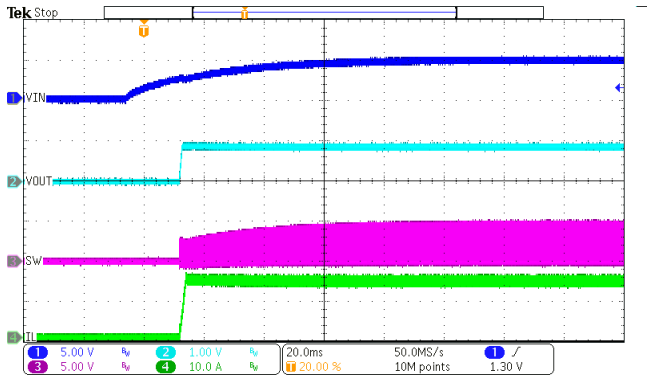


Figure 20. Power up (I_{LOAD}=15A)

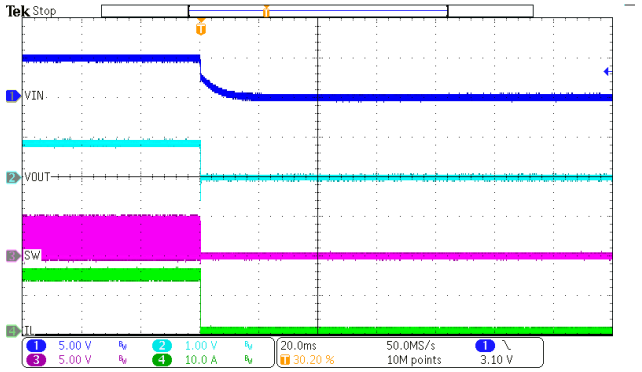


Figure 21. Power down (I_{LOAD}=15A)

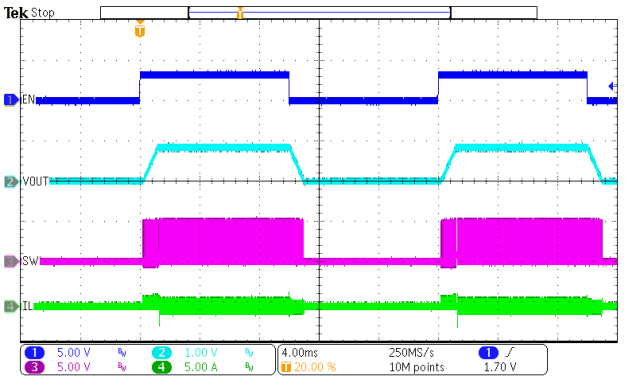


Figure 22. EN pin toggle (I_{LOAD}=0.1A, soft-stop enable)

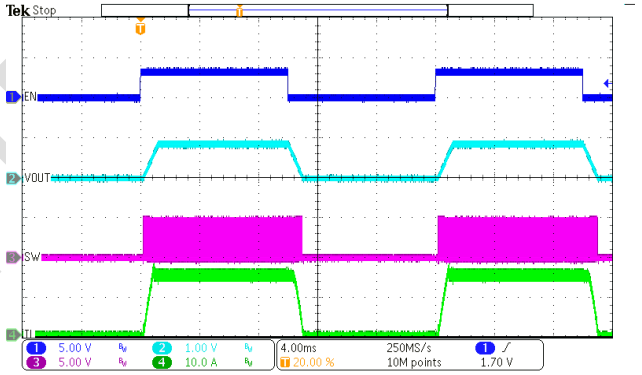


Figure 23. EN pin toggle (I_{LOAD}=15A, soft-stop enable)

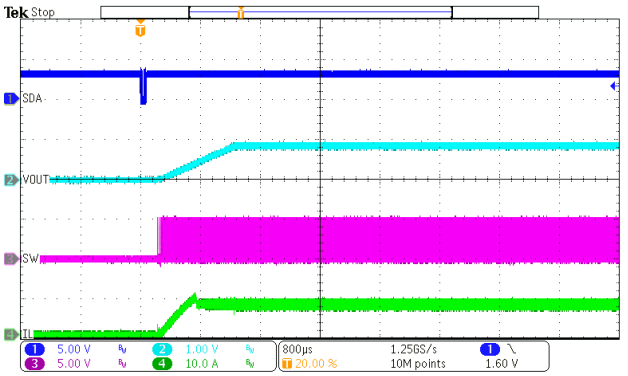


Figure 24. I²C digital enable(I_{LOAD}=7.5A)

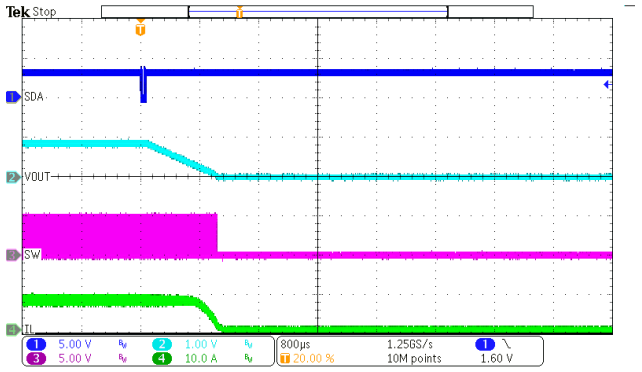


Figure 25. I²C digital disable(I_{LOAD}=7.5A, soft-stop enable)

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Application Waveforms *(continued)*

V_{IN}=5V, L=0.16uH, fsw=2.2MHz, V_{OUT}=0.875V, unless otherwise noted.

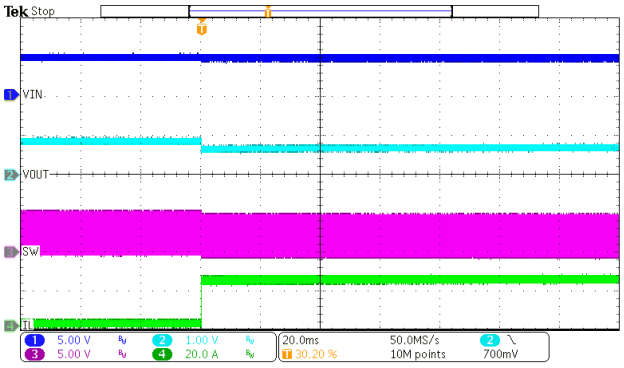


Figure 26. Over Current Protection: LIMIT Mode

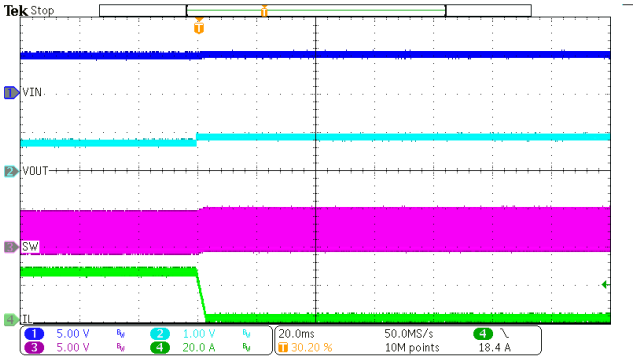


Figure 27. Over Current Release: LIMIT Mode

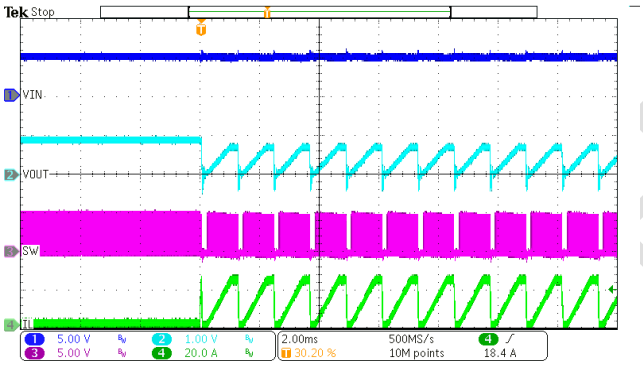


Figure 28. Over Current Protection: HICCUP Mode

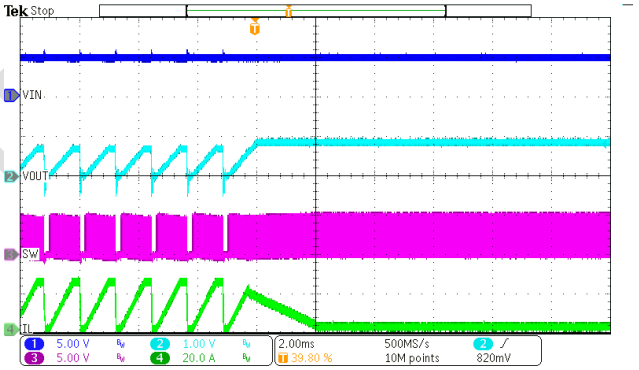


Figure 29. Over Current Release: HICCUP Mode

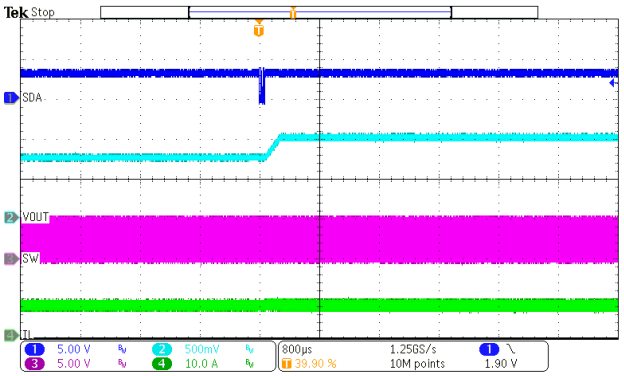


Figure 30. DVS from 0.75V to 1V (I_{LOAD}=7.5A)

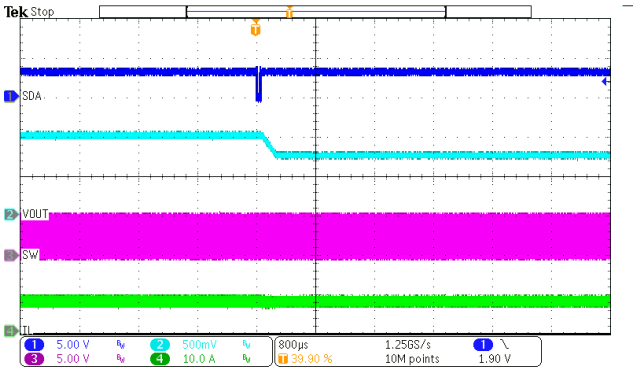


Figure 31. DVS from 1V to 0. 75V (I_{LOAD}=7.5A)

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Application Waveforms*(continued)*

V_{IN}=5V, L=0.16uH, fsw=2.2MHz, V_{OUT}=0.875V, unless otherwise noted

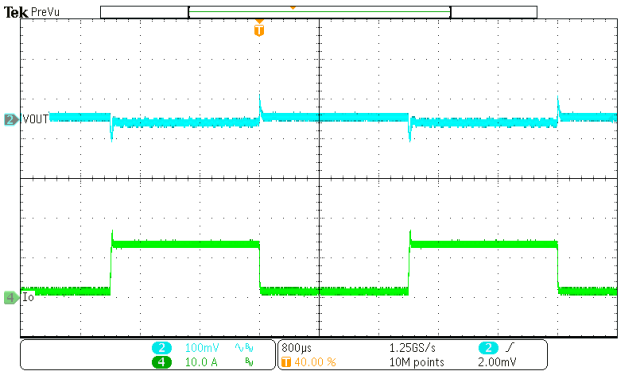


Figure 32. Load Transient (1.5A-13.5A, 1.6A/us)

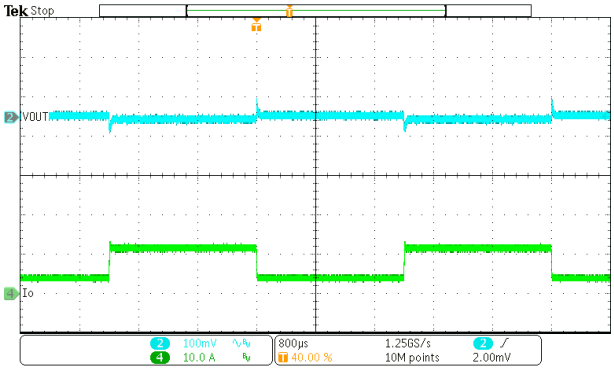


Figure 33. Load Transient (3.75A-11.5A, 1.6A/us)

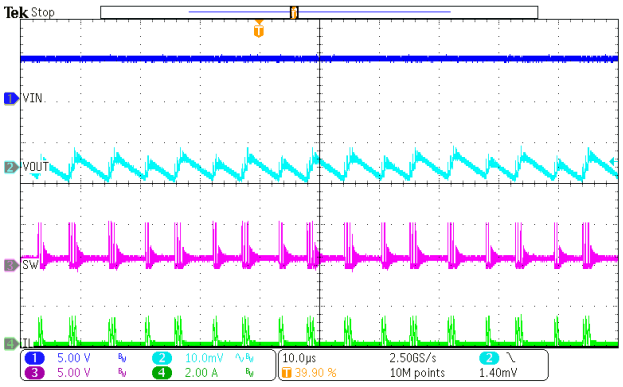


Figure 34. Output Ripple (I_{LOAD}=100mA, PFM mode)

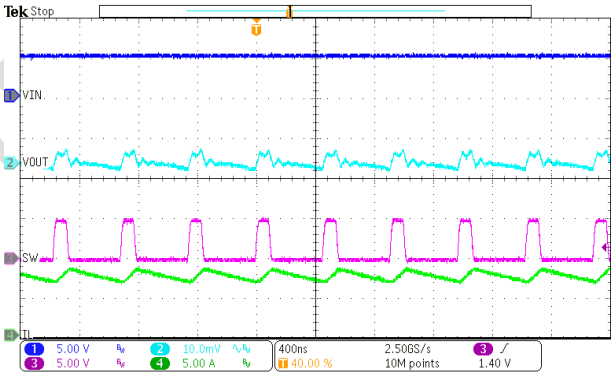


Figure 35. Output Ripple (I_{LOAD}=7.5A)

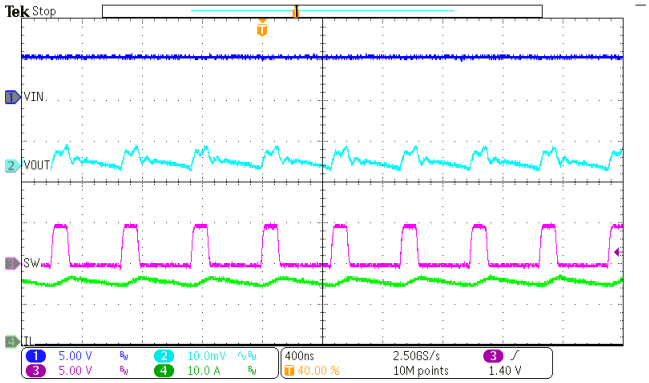


Figure 36. Output Ripple (I_{LOAD}=15A)

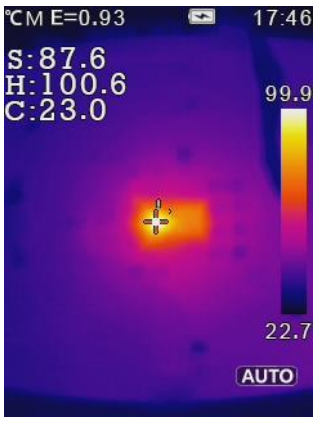


Figure 37. Thermal, V_{IN}=5V, V_{OUT}=0.875V, I_{LOAD}=15A

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Layout Guideline

Proper PCB layout is a critical for SCT21F0Q's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.
4. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias directly under the IC. The center thermal pad should always be soldered to the board for mechanical strength and reliability, using multiple thermal vias underneath the thermal pad. Improper soldering thermal pad to ground plate on PCB will cause SW higher ringing and overshoot besides downgrading thermal performance. It is recommended 8mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss thru the vias is of concern, plugging or tenting can be used to achieve a repeatable process.
5. Output inductor should be placed close to the SW pin. The area of the PCB conductor minimized to prevent excessive capacitive coupling.

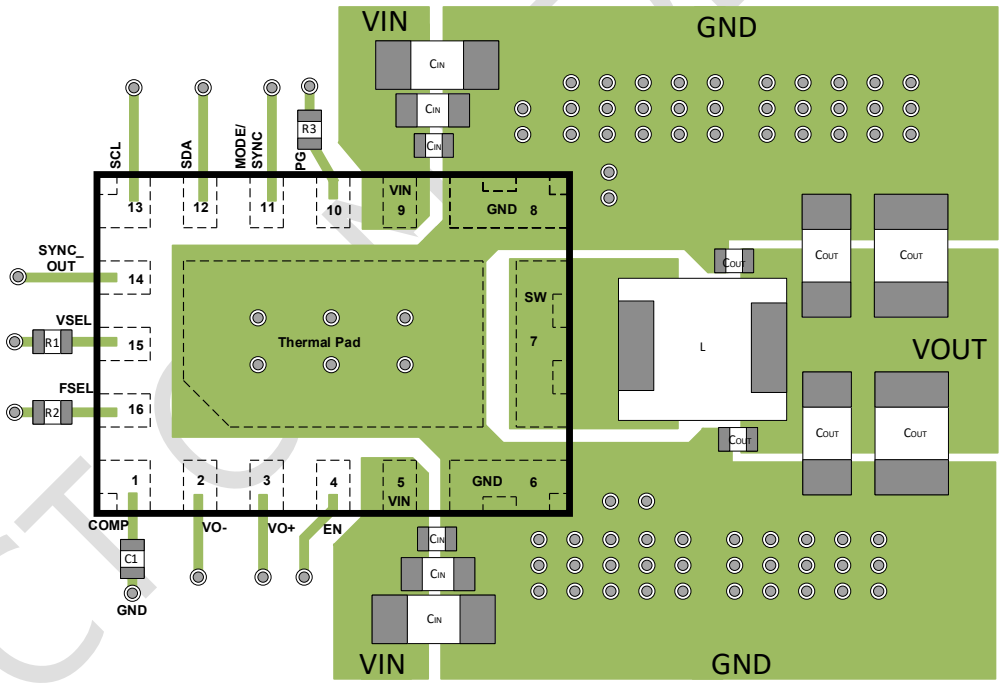
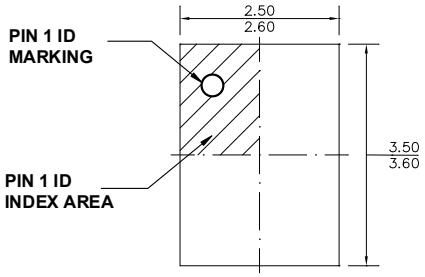


Figure 38. PCB Layout Example

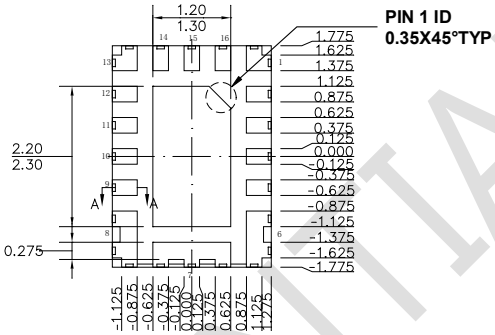
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PACKAGE INFORMATION



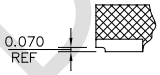
TOP VIEW



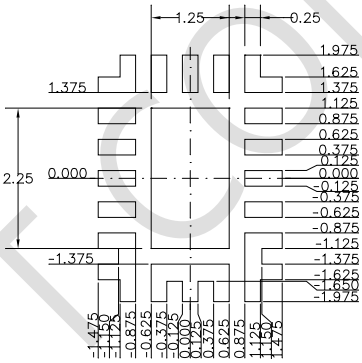
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

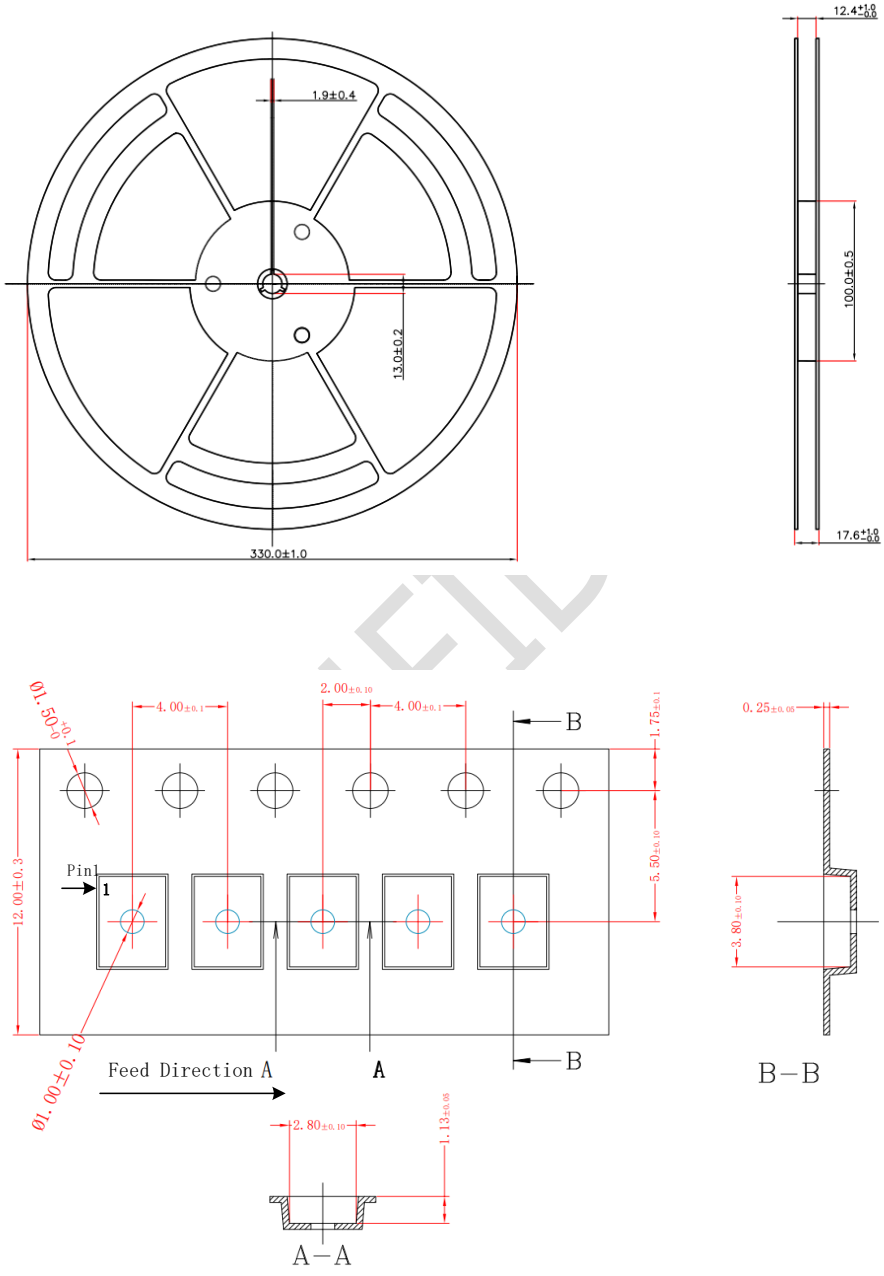
NOTE:

1)THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.1 MILLIMETERS MAX.
4) DRAWING CONFIRMS TO JEDEC MO-303.
5) DRAWING IS NOT TO SCALE.

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TAPE AND REEL INFORMATION



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