Wide Vin 60V Non-synchronous Boost/Flyback/SEPIC Converter

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 0: -40°C to 150°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- Wide Input Voltage Range: 3.1V-55V
- Low Shutdown Current: 2μA
- Low Quiescent Operating Current: 490μA
- +/- 1.5% Feedback Reference Voltage
- High Efficiency LS MOSFET with 77mΩ $R_{DS(ON)}$
- Adjustable Switching Frequency: 100KHz to 2.2MHz
- Selectable Frequency Dither for EMI Mitigation
- External Frequency Synchronic
- External Compensation
- Pulse Skipping Mode
- Adjustable Soft-start Time
- Power Good Indicator
- Integrated Protection Feature
  - Constant Peak-Current Protection Threshold Over Input Voltage
  - Output Overvoltage Protection
  - Adjustable Under-voltage Lockout
  - Selectable Hiccup Over Load Protection
  - Thermal Shutdown Protection:175°C
- TQFN-16L(3mm*3mm) Package

APPLICATIONS

- Multi-output Flyback
- LED Bias Supply
- Portable Speaker Supply
- Battery Powered Boost/Flyback/SEPIC application
- Automotive Start-stop Application
- High voltage LiDAR power supply

DESCRIPTION

The SCT81570Q device is a wide input, non-synchronous boost converter with an integrated 60V, 6A power switch. The device can be used in Boost, SEPIC and Flyback converters.

The switching frequency of the SCT81570Q device can be adjusted to any value between 100kHz and 2.2MHz by using a single external resistor or by synchronizing it to an external clock. Current mode control provides superior bandwidth and transient response in addition to cycle-by-cycle current limiting. Current limit is constant over input voltage.

The SCT81570Q is an Electromagnetic Interference (EMI) friendly controller with implementing optimized design for EMI reduction. The SCT81570Q features selectable Frequency Spread Spectrum (FSS) with ±6% jittering span of the switching frequency and modulation rate 1/512 of switching frequency to reduce the conducted EMI.

The SCT81570Q device has built-in protection features such as thermal shutdown, short-circuit protection and overvoltage protection. Power-saving shutdown mode reduces the total supply current to 2μA.

The device is available in a TQFN-16L(3mm*3mm) Package.

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TYPICAL APPLICATION

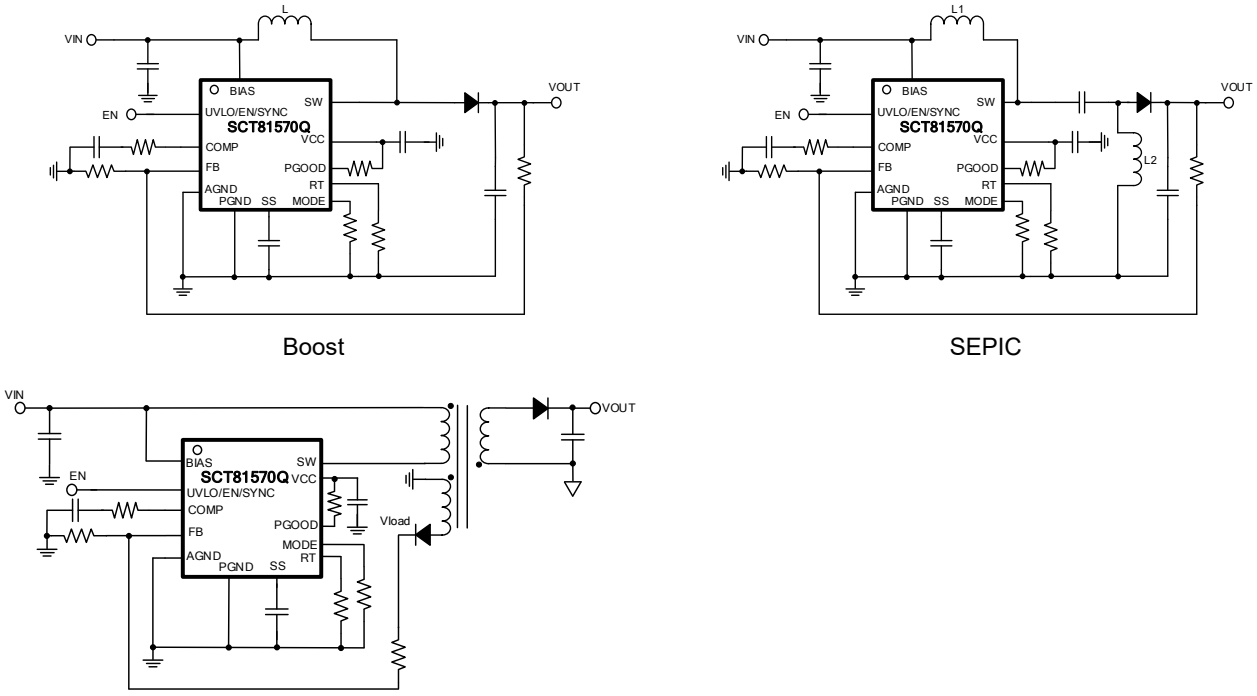

Figure 1. Typical Application Diagram

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version

Revision 1.0: Released to market

Revision 1.1: Updated Recommended Land Pattern

Revision 1.2: Added Pin1 and Feed Direction in Tape and Reel Information

Revision 1.3: Updated V_{EN_RISING} and $V_{EN_FALLING}$ in Electrical Characteristics

DEVICE ORDER INFORMATION

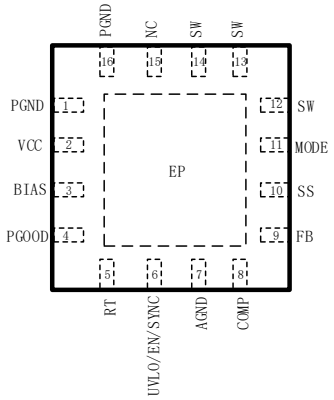
ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL
SCT81570QQLAR	Tape & Reel	5000	1570Q	16	TQFN3X3-16L	2

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted (1)

DESCRIPTION	MIN	MAX	UNIT
BIAS	-0.3	62	V
UVLO/EN/SYNC	-0.3	45	V
SW	-0.3	62	V
PGOOD	-0.3	18	V
VCC	-0.3	6.6	V
MODE, SS, COMP, FB, RT	-0.3	5.5	V
Junction temperature (2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

PIN CONFIGURATION



Top View: 16-Lead Plastic QFN 3mmx3mm

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) Guaranteed by design, not tested in productions.
(3) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 170°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	DESCRIPTION
PGND	1,16	Power ground pin. Connect directly to the power ground plane through wide and short path. Source connection of the internal N-channel power MOSFET.
VCC	2	Output of the internal VCC regulator and supply voltage input of the internal MOSFET driver. Connect a ceramic bypass capacitor from this pin to PGND.
BIAS	3	Power supply input pin. Connect a bypass capacitor from this pin to PGND.
PGOOD	4	Power Good indicator. This pin is an open-drain output. A high state indicates that the voltage at the FB pin is within a specified tolerance window centered. Connect a pull-up resistor to the system voltage rail.
RT	5	Switching frequency setting pin. The switching frequency is programmed by a single resistor between RT and AGND.

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PIN FUNCTIONS (continued)

NAME	NO.	DESCRIPTION
UVLO/EN/ SYNC	6	Undervoltage lockout programming pin. The converter start-up and shutdown levels can be programmed by connecting this pin to the supply voltage through a resistor divider. The internal clock can be synchronized to an external clock signal into the UVLO/EN/SYNC pin. This pin must not be left floating. If this pin is not directly used, connect it to BIAS pin through a resistor divider network with R_{UP} = 51kΩ and R_{DOWN} = 100kΩ.
AGND	7	Analog ground pin. Connect to the analog ground plane through a wide and short path. Connect to the PGND pin with path as short as possible.
COMP	8	Output of the internal transconductance error amplifier. Connect the loop compensation components between this pin and ground.
FB	9	Inverting input of the error amplifier. Connect a voltage divider from the output to this pin to set output voltage. The device regulates FB voltage to the internal reference value of 1V typical.
SS	10	Slow-start and tracking. An external capacitor connected to this pin sets the output rise time. Since the voltage on this pin overrides the internal reference, it can be used for tracking and sequencing.
MODE	11	MODE < 250mV or connect to AGND during initial power up. Hiccup mode protection is disabled and spread spectrum is disabled.
		250mV < MODE < 500 mV or connect a 37.4kΩ resistor between this pin and AGND during initial power up. Hiccup mode protection is enabled and spread spectrum is enabled.
		500mV < MODE < 750mV or connect a 62.0kΩ resistor between this pin and AGND during initial power up. Hiccup mode protection is enabled and spread spectrum is disabled.
		MODE > 750mV or connect a 100kΩ resistor between this pin and AGND during initial power up. Hiccup mode protection is disabled and spread spectrum is enabled.
SW	12, 13, 14	Switch pin. Drain connection of the internal N-channel power MOSFET.
NC	15	No internal electrical contact. Optionally connect to PGND for improved thermal conductivity.
EP	-	Exposed pad of the package. The exposed pad must be connected to AGND and the large ground copper plane to decrease thermal resistance.

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RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{BIAS}	Input voltage range	3.1	55	V
I_{SW}	Switch Current	0	See note (1)	A
f_{SW}	Typical Switching Frequency	100	2200	kHz
T_J	Operating junction temperature	-40	150 (2)	°C

(1) Maximum switch current is limited by pre-programmed peak current limit (I_{LIM}), and is guaranteed when $T_J < T_{SD}$.
(2) Junction temperatures exceeding 125°C may reduce operating lifetime of the device. The maximum operating junction temperature is specified at 150°C.

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per AEC-Q100-002	-2	+2	kV
	Charged Device Model (CDM), per AEC-Q100-011	-1	+1	kV

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	DFN-12L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	56.92	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	6.28	
Ψ_{JB}	Junction-to-board characterization parameter(1)	27.91	
$R_{\theta JC\ (top)}$	Junction to case (top) thermal resistance(1)	28.83	
$R_{\theta JC\ (bot)}$	Junction to case (bottom) thermal resistance(1)	80.64	
$R_{\theta JB}$	Junction to boarsd thermal resistance(1)	4.96	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT81570Q is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT81570Q. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

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ELECTRICAL CHARACTERISTICS

V_{BIAS}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{BIAS}	Operating input voltage		3.1		55	V
V_{BIAS_UVLO}	BIAS input UVLO hysteresis	V_{BIAS} rising		2.82 160	3	V mV
I_{SD}	Shutdown current	V_{UVLO}=0		2	6	μA
I_Q	Quiescent current from VBIAS	no load, no switching, V_{FB}=1V		490	600	μA
I_{SUPPLY} (1)	Supply current	Boost, V_{BIAS} =9V, V_{OUT}=12V, R_{RT}=9.53kΩ, switching, no load		2		mA
VCC Power						
V_{CC}	Internal linear regulator	V_{BIAS}>7V, I_{VCC}=18mA	4.4	4.9	5.4	V
$V_{CC_UVLO_RISING}$			2.65	2.8	2.95	V
$V_{CC_UVLO_HYS}$				105		mV
IV_{CC}	VCC Sourcing current limit		90	140		mA
UVLO/EN/SYNC						
V_{UVLO_RISING}	UVLO/SYNC threshold	V_{UVLO} ramping up	1.425	1.5	1.575	V
$V_{UVLO_FALLING}$	UVLO/SYNC threshold	V_{UVLO} ramping down	1.37	1.45	1.52	V
V_{UVLO_HYS}	UVLO/SYNC Hysteresis			50		mV
I_{UVLO}	UVLO source current		3.05	4.85	6.4	μA
V_{EN_RISING}	EN rising threshold	V_{EN} ramping down	0.74	0.88	0.98	V
$V_{EN_FALLING}$	EN falling threshold	V_{EN} ramping down	0.6	0.78	0.93	V
Reference and Control Loop						
V_{REF}	Reference voltage of FB		0.985	1	1.015	V
I_{FB}	FB pin leakage current	V_{FB}=1V			100	nA
G_{EA}	Error amplifier trans-conductance	V_{COMP}=1.5V	1.2	2	2.8	mA/V
I_{COMP_SRC}	Error amplifier maximum source current	V_{FB}=V_{REF}-200mV, V_{COMP}=1.5V	135	180	220	μA
I_{COMP_SNK}	Error amplifier maximum sink current	V_{FB}=V_{REF}+200mV, V_{COMP}=1.5V	135	180	220	μA
V_{COMP_H}	COMP high clamp	V_{FB}=0.8V	1.5	2.25	2.9	V
V_{COMP_L}	COMP low clamp	V_{FB}=1.7V	0.72	0.96	1.2	V
A_{CS}	$\Delta V_{COMP}/\Delta I_{SW}$			0.16		
Power Switch						
$R_{DS(ON)}$	Internal MOSFET switch on resistance	V_{BIAS} =12V		77	145	mΩ
I_{SW_LKG}	Leakage current	V_{SW} =12V			1200	nA

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ELECTRICAL CHARACTERISTICS (continued)

V_{BIAS}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Current Limit						
I_{LIM}	Internal MOSFET current limit		5.2	6	7	A
$C_{HICC-DEL}$	Hiccup mode activation delay	Clock cycles with current limiting before hiccup off-time activated (SS_done)		64		cycles
C_{HICCUP}	Hiccup mode off-time after activation	Clock cycles with no switching followed by SS release		32768		cycles
Soft start						
I_{SS}	Soft-start Current		7	10	14	μA
R_{SS}	SS pull-down switch $R_{DS(ON)}$			65		Ω
PGOOD						
R_{PG}	PG pulldown switch resistance	1mA sinking		95		Ω
V_{UVTH}	PG under-voltage threshold	FB rising (Reference to VREF)	92	95	98	%
		FB falling (Reference to VREF)	87	90	93	%
Switching Frequency						
f_{SW1}	Switching frequency	R_{RT}=49.3kΩ	400.5	445	489.5	kHz
f_{SW2}	Switching frequency	R_{RT}=9.09kΩ	1925	2140	2355	kHz
f_{SS}	Frequency Spread Range			±6		%
D_{MAX}	Maximum Duty Cycle	R_{RT}=49.3kΩ	85	91		%
t_{ON_MIN}	Minimum on-time	fsw=445kHz		160		ns
Protection						
V_{OVTH}	FB overvoltage threshold	FB rising	107	110	113	%
		FB falling	102	105	108	%
T_{SD} (1)	Thermal shutdown threshold	T_J rising		175		°C
	Hysteresis			25		°C

(1) Guaranteed by design and bench, not tested in production.

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TYPICAL CHARACTERISTICS

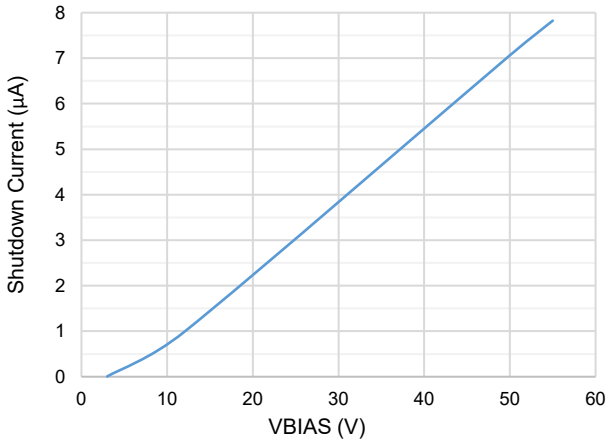

Figure 2. I_{SD} vs Input Voltage

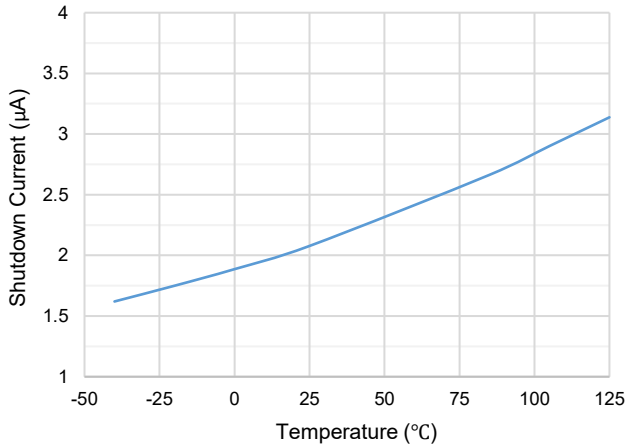

Figure 3. I_{SD} vs Temperature

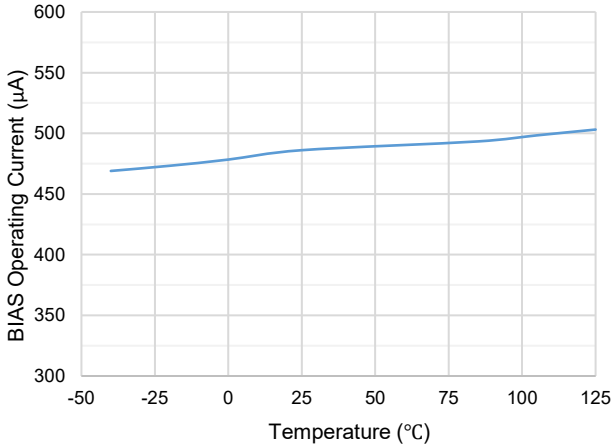

Figure 4. BIAS Operating Current vs Temperature

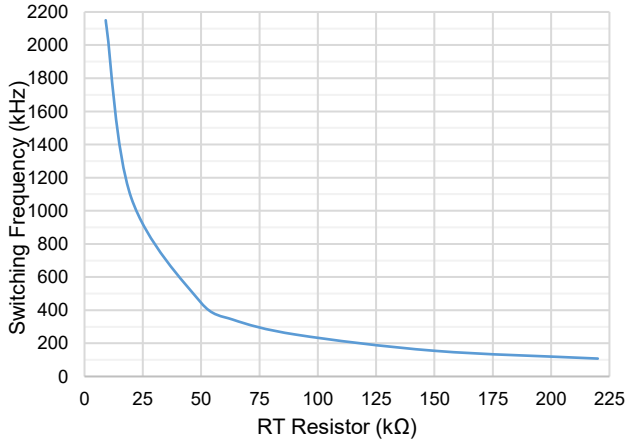

Figure 5. Switching Frequency vs RT

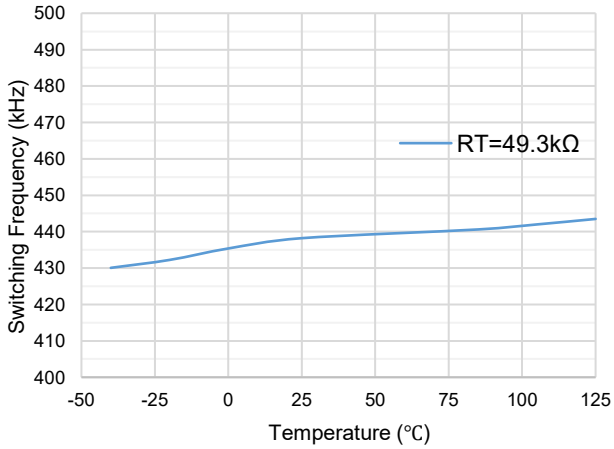

Figure 6. Switching Frequency vs Temperature

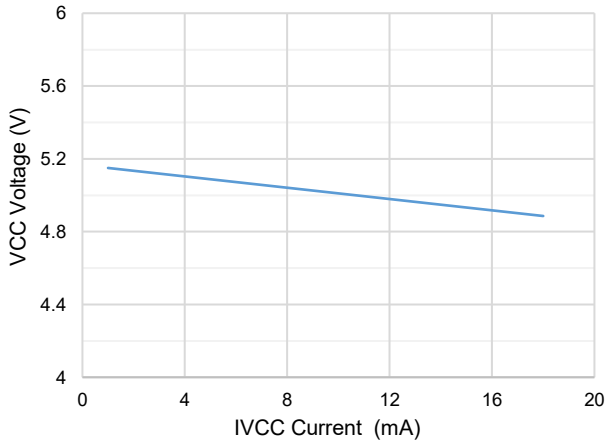

Figure 7. VCC vs I_{VCC}

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TYPICAL CHARACTERISTICS

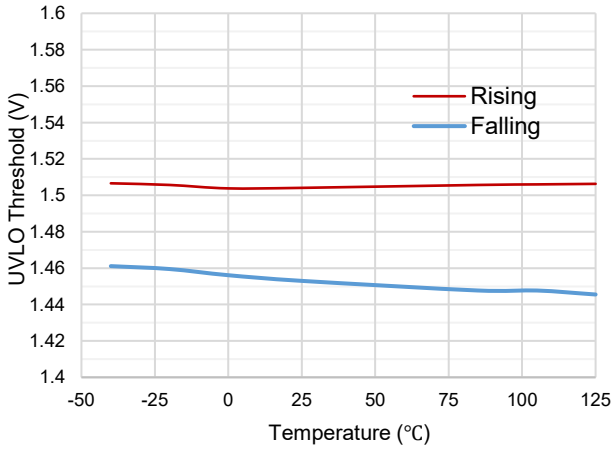

Figure 8. UVLO Threshold vs Temperature

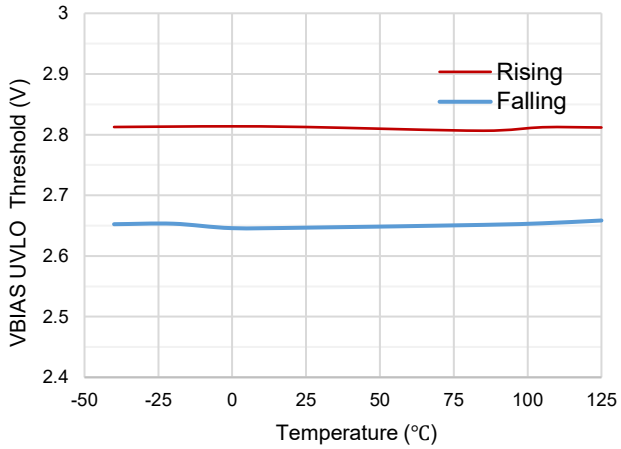

Figure 9. VBIAS UVLO Threshold vs Temperature

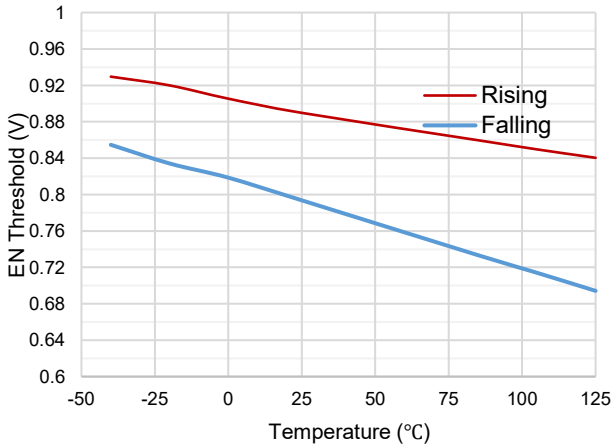

Figure 10. EN Threshold vs Temperature

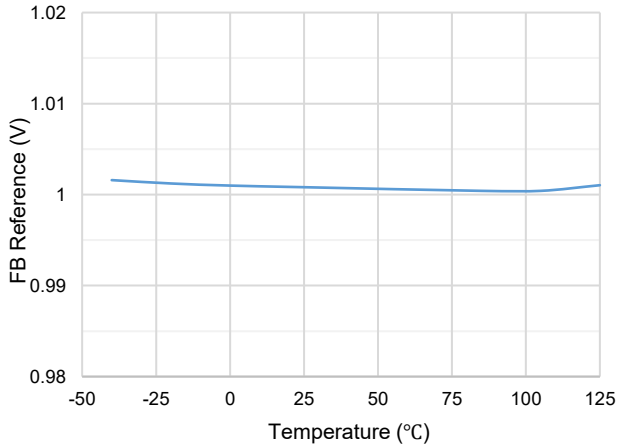

Figure 11. FB Reference vs Temperature

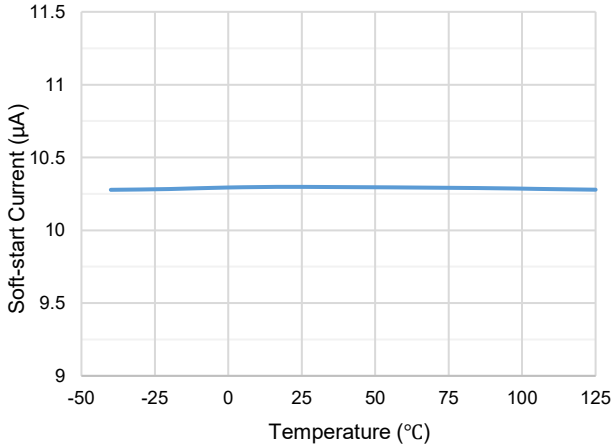

Figure 12. Soft-start Current vs Temperature

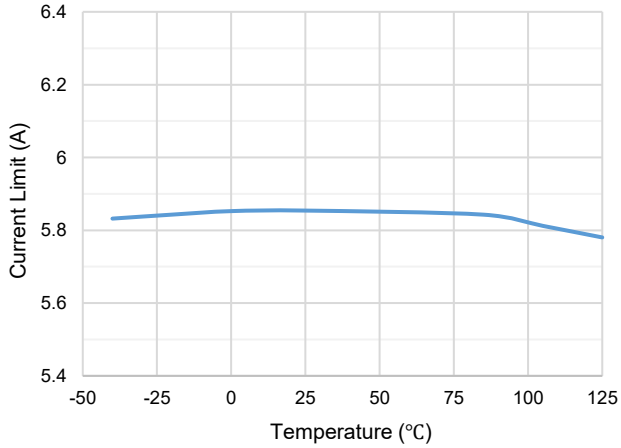

Figure 13. Internal MOSFET Current Limit vs Temperature

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TYPICAL CHARACTERISTICS

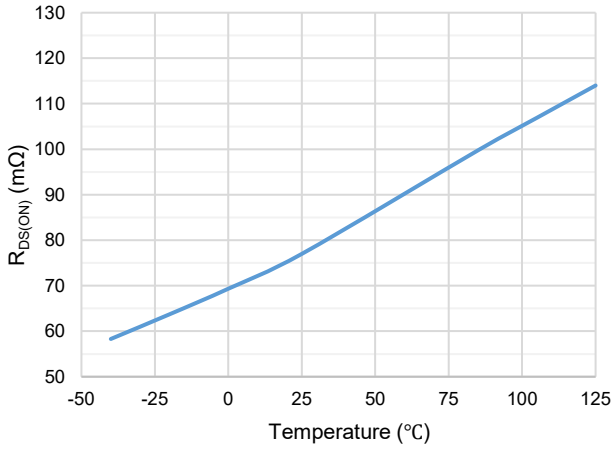

Figure 14. Internal MOSFET $R_{DS(ON)}$ vs Temperature

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FUNCTIONAL BLOCK DIAGRAM

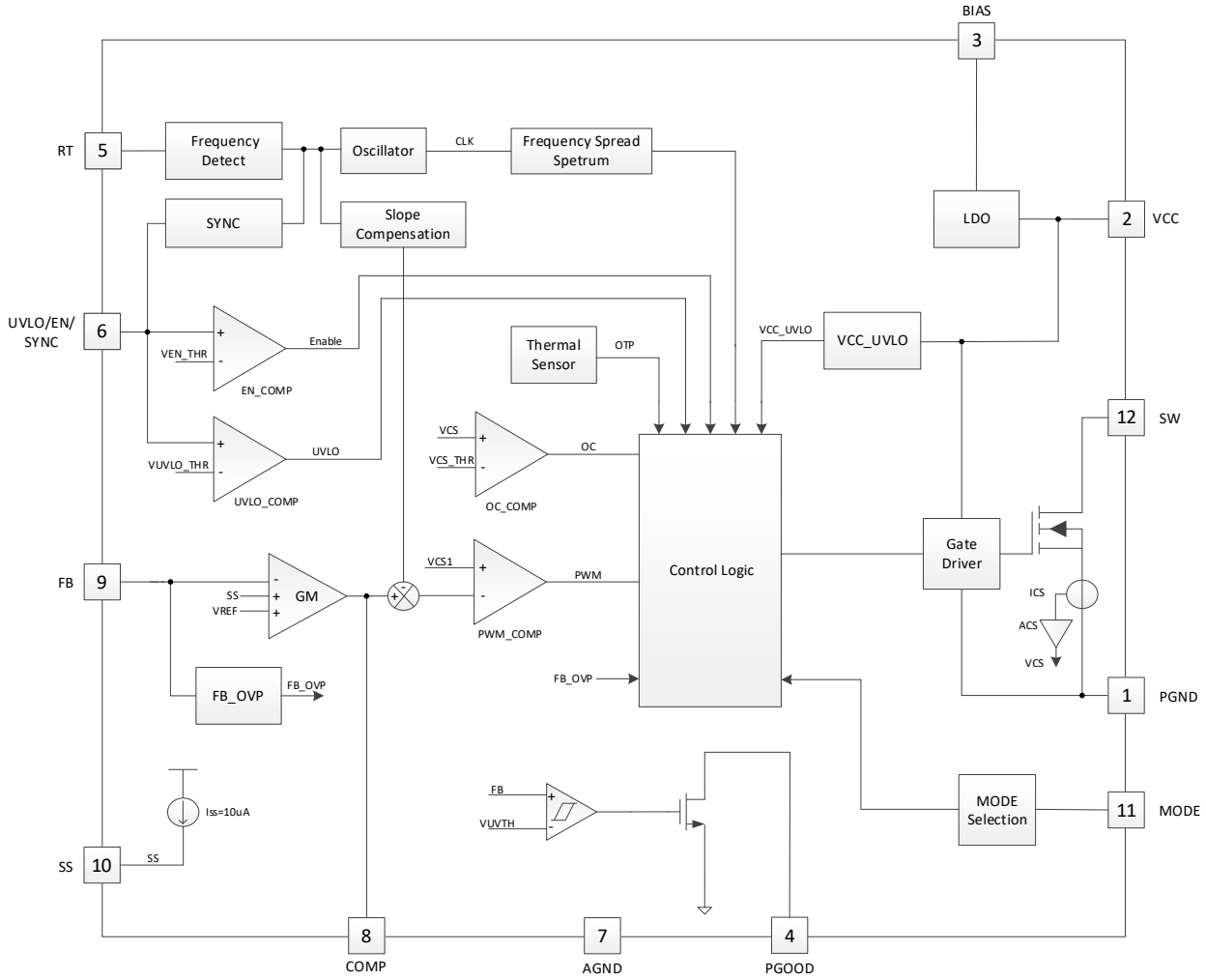

Figure 15. Functional Block Diagram

OPERATION

Overview

The SCT81570Q device is a wide input range, non-synchronous boost converter that uses peak-current-mode control. The device can be used in boost, SEPIC, and flyback topologies.

The switching frequency of the SCT81570Q device can be adjusted to any value between 100kHz and 2.2MHz by using a single external resistor or by synchronizing it to an external clock. Current mode control provides superior bandwidth and transient response in addition to cycle-by-cycle current limiting. Current limit is constant over input voltage.

The SCT81570Q is an Electromagnetic Interference (EMI) friendly controller with implementing optimized design for EMI reduction. The SCT81570Q features selectable Frequency Spread Spectrum (FSS) with ±6% jittering span of the switching frequency and modulation rate 1/512 of switching frequency to reduce the conducted EMI.

The SCT81570Q device has built-in protection features such as thermal shutdown, short-circuit protection and overvoltage protection.

The SCT81570Q works at pulse skip mode (PSM) to further increase the efficiency in light load condition.

The quiescent current of SCT81570Q is 490uA typical under no-load condition and no switching. Disabling the device, the typical supply shutdown current on BIAS pin is 2μA.

Overvoltage Protection

The SCT81570Q has over voltage protection (OVP) for the output voltage. OVP is sensed at the feedback pin (FB). If at any time the voltage at the feedback pin rises to 1.1V (typ.), OVP is triggered. OVP will cause the GATE pin to go low, forcing the power MOSFET off. With the MOSFET off, the output voltage will drop. The SCT81570Q begins switching again when the feedback voltage reaches 1.05V (typ.).

Current Sense and Slope Compensation Ramp

The device senses switch current which flows into the SW pin, and provides a fixed internal slope compensation ramp, helping prevent subharmonic oscillation at high duty cycle. The internal slope compensation ramp is added to the sensed switch current for the PWM operation, but no slope compensation ramp is added to the sensed inductor current for the current limit operation to provide an accurate peak current limit over the input supply voltage.

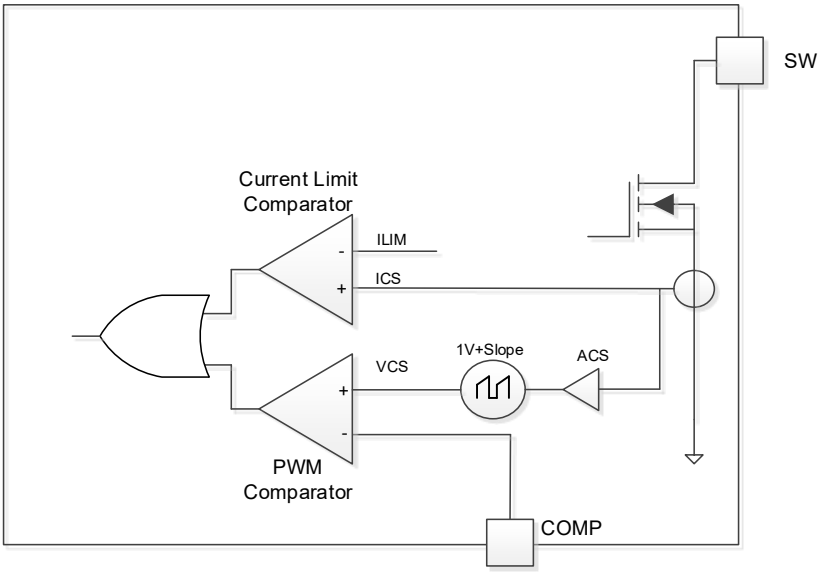

Figure 16. Current Sensing and Slope Compensation

Use Equation 1 to calculate the value of the peak slope voltage (V_{SLOPE}).

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$$V_{SLOPE} = 160mV \times \frac{f_{RT}}{f_{SYNC}} \quad (1)$$

where

• f_{SYNC} is f_{RT} if clock synchronization is not used

According to peak current mode control theory, the slope of the compensation ramp must be greater than half of the sensed inductor current falling slope to prevent subharmonic oscillation at high duty cycle. Therefore, the minimum amount of slope compensation in boost topology must satisfy the following inequality:

$$0.5 \times \frac{(V_{LOAD} + V_F) - V_{SUPPLY}}{L_M} \times A_{CS} \times \text{Margin} < 160mV \times f_{SW} \quad (2)$$

Where

• V_F is a forward voltage drop of diode, the external diode

Typically, 82% of the sensed inductor current falling slope is known as an optimal amount of the slope compensation. By increasing the margin to 1.6, the amount of slope compensation becomes close to the optimal amount.

If clock synchronization is not used, the f_{SW} frequency equals the f_{RT} frequency. If clock synchronization is used, the f_{SW} frequency equals the f_{SYNC} frequency.

Hiccup Mode Overload Protection

When overload happens, the converter cannot provide output current to satisfy loading requirement. The inductor current is clamped at over current limitation. Thus, the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously. The internal COMP voltage ramps up to high.

Hiccup Mode is enabled by a single resistor (37.4kΩ or 62kΩ typically) between the MODE pin and ground during initial power up. When COMP voltage is clamped for 64 cycles, the controller stops working. After remaining OFF for 32768 cycles, the device restarts from soft starting phase. If overload or hard short condition still exists during soft-start and make COMP voltage clamped at high , after soft start time and COMP still keep high for 64 cycles , the device enters into turning-off mode again. When overload or hard short condition is removed, the device automatically recovers to enters normal regulating operation.

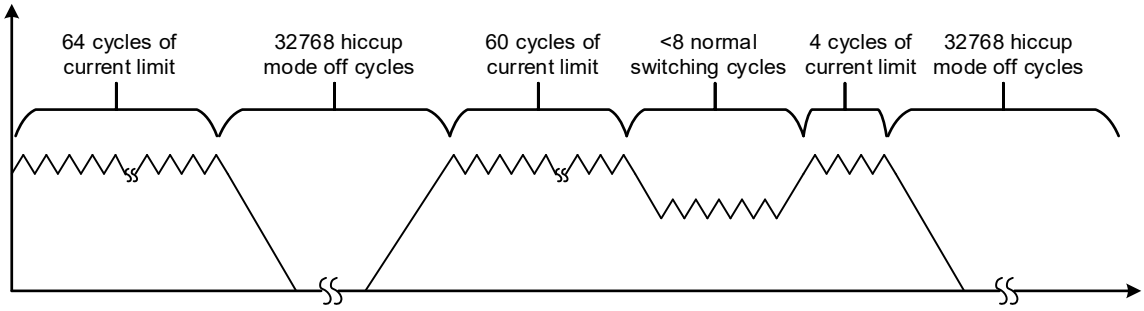

Figure 17. Hiccup Mode Protection

Output Voltage and Error Amplifier

The output voltage is set by an external resistor divider R_{FBT} and R_{FBB} in typical application schematic. The value of RFBT can be calculated by equation 3.

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \quad (3)$$

where:

- V_{REF} is the feedback reference voltage, typical 1V

The feedback resistor divider is connected to an internal transconductance error amplifier. The output of the error amplifier is connected to the COMP pin, allowing the use of a Type II loop compensation network. R_{COMP}, C_{COMP}, and optional C_{HF} loop compensation components configure the error amplifier gain and phase characteristics to

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achieve a stable loop response. If necessary, especially during automotive load dump transient, the feedback resistor divider input can be clamped by using an external zener diode.

The COMP pin features internal clamps. The maximum COMP clamp limits the maximum COMP pin voltage below its absolute maximum rating even in shutdown. The minimum COMP clamp limits the minimum COMP pin voltage to start switching as soon as possible during no load to heavy load transition. The minimum COMP clamp is disabled when FB is connected to ground in flyback topology.

Switching Frequency

The switching frequency of the SCT81570Q can be adjusted between 100 kHz and 2.2 MHz using a single external resistor. This resistor must be connected between the RT pin and ground. Equation 4 can be used to estimate the frequency adjust resistor.

$$R_{RT}(\Omega) = \frac{2.21 \times 10^{10}}{fsw(Hz)} - 955 \quad (4)$$

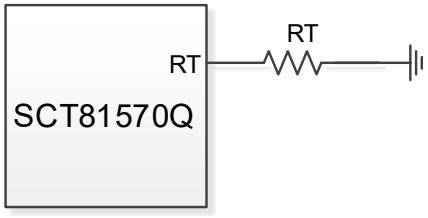

Figure 18. Frequency Adjust

Enable and Under Voltage Lockout

The external UVLO resistor divider must be designed so that the voltage at the UVLO pin is greater than 1.5V typical) when the input voltage is in the desired operating range. The values of R1 and R2 can be calculated as shown in Equation 5 and Equation 6.

$$R1 = \frac{V_{IN_ON} \times \frac{V_{UVLO(FALLING)}}{V_{UVLO(RISING)}} - V_{IN_OFF}}{I_{UVLO}} \quad (5)$$

where

- V_{IN_ON} is the desired start-up voltage of the converter
- V_{IN_OFF} is the desired turnoff voltage of the converter.

$$R2 = R1 * \frac{V_{UVLO(RISING)}}{V_{IN_ON} - V_{UVLO(RISING)}} \quad (6)$$

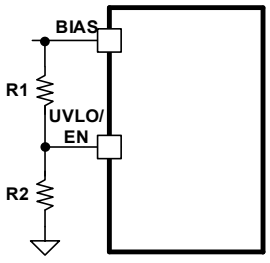

Figure 19. System UVLO Resistor Divider

When the UVLO pin voltage is above the UVLO threshold, the device enters run mode. In run mode, a soft-start sequence starts after 8 clocks once the VCC voltage exceeds the 2.8V VCC UV threshold. UVLO hysteresis is accomplished with an internal 50mV voltage hysteresis and an additional 5μA current source that is switched on or off. When the UVLO pin voltage exceeds the UVLO threshold, the current source is enabled to quickly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the UVLO threshold, the current source is disabled,

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causing the voltage at the UVLO pin to fall quickly. When the UVLO pin voltage is less than the enable threshold, the device enters shutdown mode after a 30μs (typical) delay with all functions disabled.

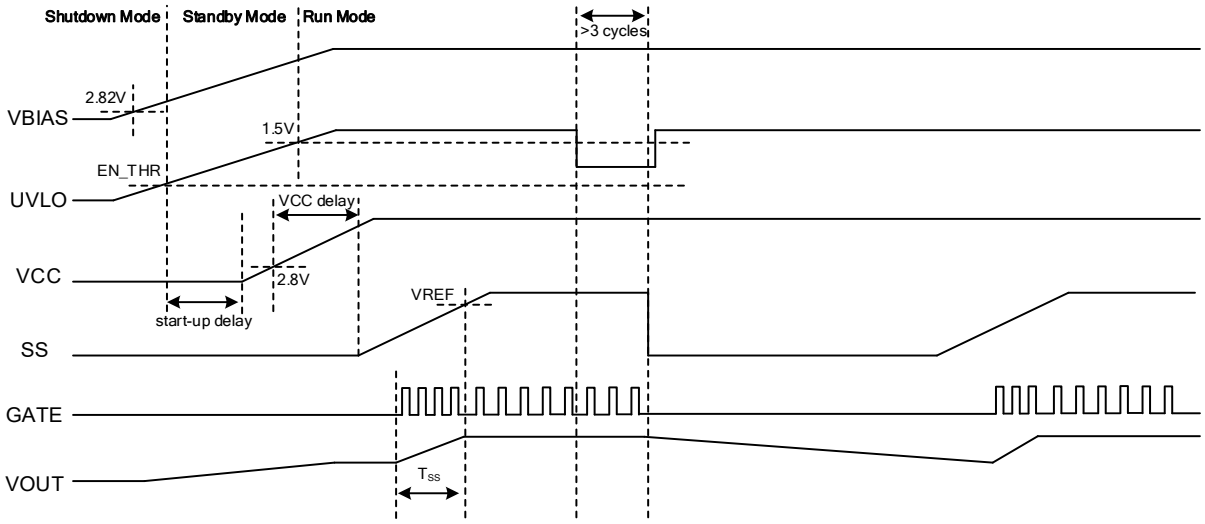

Figure 20. Boost Start-Up Waveforms Case 1: Start-Up diagram, UVLO Toggle After Start-Up

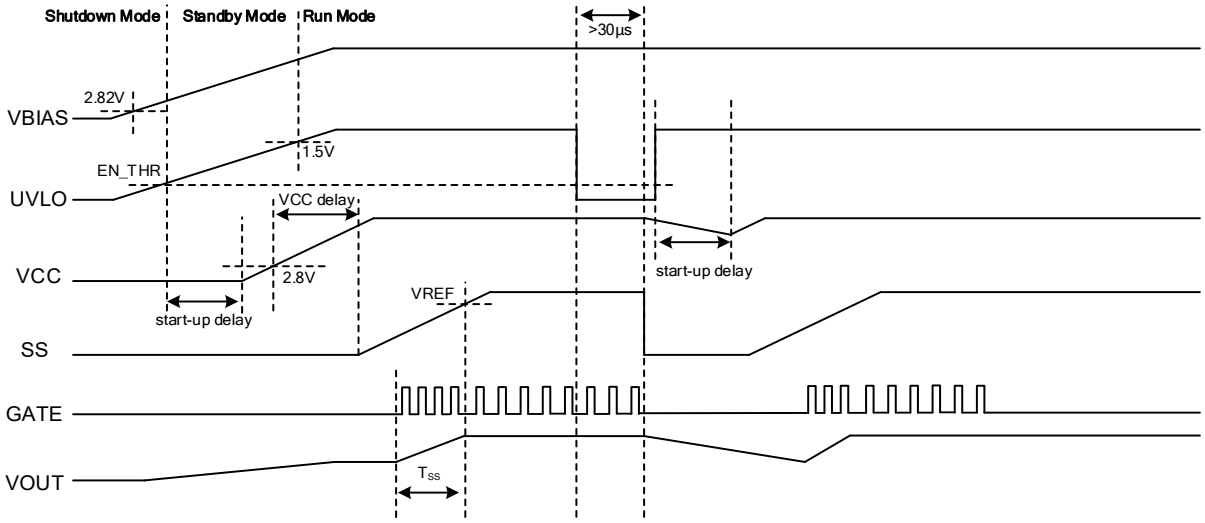

Figure 21. Boost Start-Up Waveforms Case 2: Start-Up diagram, EN Toggle After Start-Up

Clock Synchronization

The switching frequency of the device can be synchronized to an external clock by pulling down the UVLO/ SYNC pin. The external synchronization clock must pull down the UVLO/SYNC pin voltage below 1.45V (typical). The duty cycle of the pulldown pulse is not limited, but the minimum pulldown pulse width must be greater than 150 ns, and the minimum pullup pulse width must be greater than 250ns.

The external clock frequency f_{SYNC} must be within +25% and –30% of f_{RT}(TYPICAL). Because the maximum duty cycle limit and the peak current limit with slope resistor (R_{SL}) are affected by the clock synchronization, take extra care when using the clock synchronization function.

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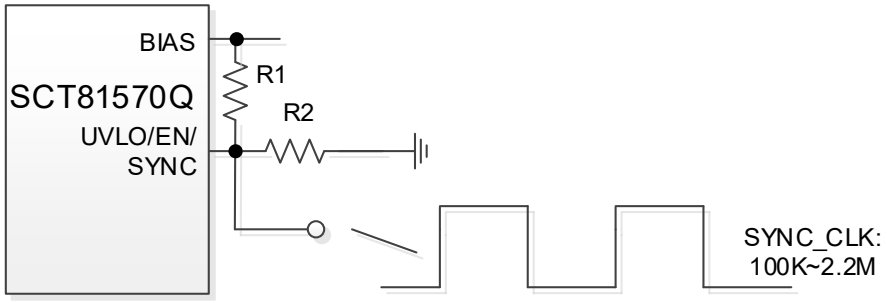

Figure 22. Frequency Sync

Programmable Soft-Start

The SS pin voltage controls start-up of output voltage. After the voltage is rising threshold of under voltage lockout reference voltage, the SCT81570Q begins regulating the output to the level dictated by the feedback resistor network and SS voltage. A 10μA current source charges the soft-start capacitor connecting SS pin. Soft start avoids inrush current as a result of high output capacitance to avoid an overcurrent condition. The inrush stress on the input supply rail is also reduced. The soft-start time, t_{SS}, for the output voltage to ramp to its nominal level is set by:

$$t_{SS} = \frac{C_{SS}}{I_{SS}} \quad (7)$$

where

- C_{SS} is the soft-start capacitance
- I_{SS} is the current sourced from the SS pin

The device adopts the lower voltage between the internal voltage reference 1V and the SS pin voltage as the reference input voltage of the error amplifier and regulates the output. The soft-start completes when the voltage at the SS pin exceeds the internal reference voltage of 1V. The SS pin is pulled down to ground by an internal switch when the VCC is less than VCC UVLO threshold, the UVLO is less than the UVLO threshold, during hiccup mode off-time or thermal shutdown.

Frequency Spread Spectrum

To reduce EMI, the device implements Frequency Spread Spectrum (FSS). The FSS is enabled by a single resistor (37.4kΩ or 100kΩ typically) between the MODE pin and ground during initial power up.

The FSS circuitry shifts the switching frequency of the regulator periodically within a certain frequency range around the adjusted switching frequency. The jittering span is ±6% of the switching frequency with 1/512 swing frequency. This frequency dithering function is effective for both frequency adjusted by resistor placed at RT pin and an external clock synchronization application.

Internal MOSFET

The device provides an internal switch with an $R_{DS(ON)}$ that is typically 77mΩ when the BIAS pin is greater than 5V. The $R_{DS(ON)}$ of the internal switch is increased when the BIAS pin is less than 5V. The device temperature must be checked at the minimum supply voltage especially when the BIAS pin is less than 5V.

The dV/dT of the SW pin must be limited during the internal start-up delay to avoid a false turn-on, which is caused by the coupling through CDG parasitic capacitance of the internal MOSFET switch.

Power Good

The PGOOD pin is an open-drain output. A pull up resistor between the values of 10KΩ and 100KΩ to a voltage source recommended.

The PGOOD pin is pulled low when the FB is lower than 90% or greater than 110% of the nominal internal reference voltage. Also, the PGOOD is pulled low if VBIAS UVLO or thermal shutdown are asserted or the UVLO/EN pin pulled low.

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Thermal Shutdown

An internal thermal shutdown turns off the VCC regulator, disables switching, and pulls down the SS when the junction temperature exceeds the thermal shutdown threshold (T_{SD}). After the temperature is decreased by 25°C, the VCC regulator is enabled again and the device performs a soft start.

Shutdown Mode

If the UVLO pin voltage is below the enable threshold for longer than 30μs (typical), the device goes to the shutdown mode with all functions disabled. In shutdown mode, the device decreases the BIAS pin current consumption to below 2μA (typical).

Standby Mode

If the UVLO pin voltage is greater than the enable threshold and below the UVLO threshold for longer than 2μs, the device is in standby mode with the VCC regulator operational, RT regulator operational, SS pin grounded, and no switching at the GATE output. The PGOOD is activated when the VCC voltage is greater than the VCC UV threshold.

Run Mode

If the UVLO pin voltage is above the UVLO threshold and the VCC voltage is sufficient, the device enters RUN mode. In this mode, soft start starts 8 internal clocks after the VCC voltage exceeds the 2.8V VCC UV threshold.

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APPLICATION INFORMATION

Typical Application (Boost)

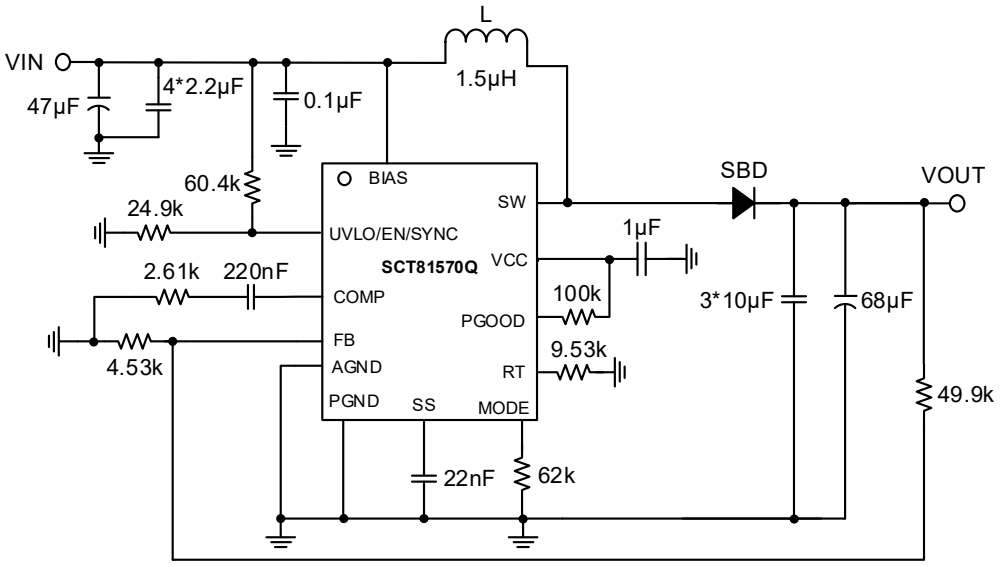

Figure 23. Application Schematic, 6V to 9V, 1.6A Boost Regulator at 2100kHz

Design Parameters

Design Parameters	Example Value
Input Voltage	6V to 9V
Output Voltage	12V
Maximum Output Current	1.6A
Switching Frequency	2100 KHz
Output voltage ripple (peak to peak)	60mV (Load=1.6A)

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Inductor Selection (Boost)

The performance of inductor affects the power supply's steady state operation, transient behavior, loop stability, and boost converter efficiency. The inductor value, DC resistance, and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DC resistance, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±50% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, maxim load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a boot converter, calculate the inductor DC current as:

$$I_{LDC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{8}$$

Where

- V_{OUT} is the output voltage of the boost converter
- I_{OUT} is the output current of the boost converter
- V_{IN} is the input voltage of the boost converter
- η is the power conversion efficiency

Calculate the inductor current peak-to-peak ripple, I_{LPP}, as:

$$I_{LPP} = \frac{1}{L \times \left(\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}} \right) \times f_{SW}} \tag{9}$$

Where

- I_{LPP} is the inductor peak-to-peak current
- L is the inductance of inductor
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Therefore, the peak switching current of inductor, I_{LPEAK}, is calculated as:

$$I_{LPEAK} = I_{LDC} + \frac{I_{LPP}}{2} \tag{10}$$

Set the current limit of the SCT81570Q higher than the peak current I_{LPEAK} and select the inductor with the saturation current higher than the current limit.

Input Capacitor Selection

Due to the presence of an inductor at the input of a boost converter, the input current waveform is continuous. The inductor ensures that the input capacitor sees fairly low ripple currents. However, as the input capacitor gets smaller, the input ripple goes up. The RMS current in the input capacitor is given using following equation.

$$I_{CIN(RMS)} = \frac{(V_{OUT} - V_{IN}) \times V_{IN}}{\sqrt{12} \times V_{OUT} \times L \times fsw} \tag{11}$$

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The input capacitor should be capable of handling the RMS current. Although the input capacitor is not as critical in a boost application, low values can cause impedance interactions. Therefore, a good quality capacitor should be chosen in the range of 10 μF to 40 μF. If a value lower than 10 μF is used, then problems with impedance interactions or switching noise can affect the SCT81570Q. To improve performance, especially with VBIAS below 8 volts, it is recommended to use a 2.2 Ohm resistor at the input to provide an RC filter. The resistor is placed in series with the BIAS pin with only a bypass capacitor attached to the BIAS pin directly. A 0.1-μF or 1-μF ceramic capacitor is necessary in this configuration. The bulk input capacitor and inductor will connect on the other side of the resistor at the input power supply.

Output Capacitor Selection

For small output voltage ripple, choose a low-ESR output capacitor like a ceramic capacitor. Typically, 3～4x 22μF ceramic output capacitors work for most applications. A 0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the switch node. Higher capacitor values can be used to improve the load transient response. Due to a capacitor's derating under DC bias, the bias can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. From the required output voltage ripple, use the equation 12 and 13 to calculate the minimum required effective capacitance, C_{OUT}.

$$V_{ripple_C} = \frac{(V_{OUT} - V_{IN_MIN}) \times I_{OUT}}{V_{OUT} \times C_{OUT} \times fsw} \quad (12)$$

$$V_{ripple_ESR} = I_{LPEAK} \times ESR \quad (13)$$

where

- V_{ripple_C} is output voltage ripple caused by charging and discharging of the output capacitor.
- V_{ripple_ESR} is output voltage ripple caused by ESR of the output capacitor.
- V_{IN_MIN} is the minimum input voltage of boost converter.
- V_{OUT} is the output voltage.
- I_{OUT} is the output current.
- I_{Lpeak} is the peak current of the inductor.
- f_{SW} is the converter switching frequency.
- ESR is the ESR resistance of the output capacitors.

Power MOSFET Selection

The following parameters should be taken into consideration for MOSFET: the on-resistance R_{DS_ON}, the minimum gate threshold voltage V_{TH_MIN}, the total gate charge Q_g, the reverse transfer capacitance C_{RSS}, and the maximum drain to source voltage V_{Q_MAX}. The peak switching voltage between drain to source in a Boost is given by

$$V_{SW_PEAK} = V_{IN} + V_D \quad (14)$$

Then the V_{Q_MAX} of power MOSFET should be greater than the peak switching voltage.

The peak switching current flowing through the MOSFET is given by:

$$I_{Q_PEAK} = I_{LPEAK} \quad (15)$$

The RMS current through the MOSFET is calculated by:

$$I_{Q_RMS} = \sqrt{(I_{LDC}^2 + \frac{I_{LPP}}{12}) * D} \quad (16)$$

Then power dissipation in MOSFET can be estimated by:

$$P_{DIS} = I_{Q_RMS}^2 \times R_{DS_ON} \times D_{MAX} + \left(V_O + V_{IN_MIN}\right) \times I_{Q_PEAK} \times \frac{Q_g \times f_{SW}}{I_G} \quad (17)$$

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Where

- I_G is the gate drive current.

The total power dissipation of MOSFET includes conduction loss as shown in the first term and switching loss as shown in the second term. The total power dissipation should be within package thermal ratings.

Output Diode Selection

Observation of the boost converter circuit shows that the average current through the diode is the average load current, and the peak current through the diode is the peak current through the inductor. The diode should be rated to handle more than its peak current. The peak diode current can be calculated using following equation.

$$I_{D(PEAK)} = \frac{I_{OUT}}{(1-D)} + \Delta I_L \quad (18)$$

Thermally the diode must be able to handle the maximum average current delivered to the output. The peak reverse voltage for boost converters is equal to the regulated output voltage. The diode must be capable of handling this voltage. To improve efficiency, a low forward drop schottky diode is recommended.

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Application Waveforms

VBIAS=8V, Vout=12V, unless otherwise noted



Figure 24. Power up (I_{LOAD}=1.6 A)
CH1: VIN; CH2: VO; CH3: SW; CH4: IL

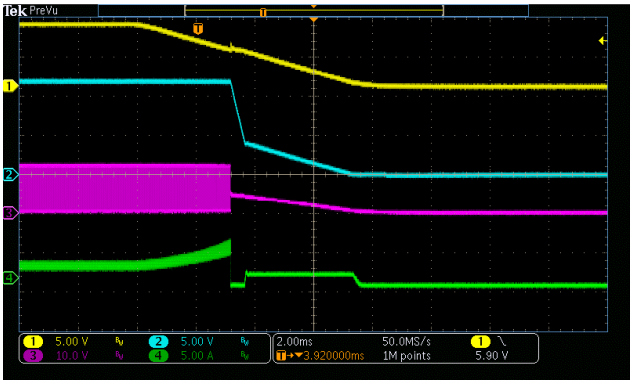

Figure 25. Power down (I_{LOAD}=1.6A)
CH1: VIN; CH2: VO; CH3: SW; CH4: IL

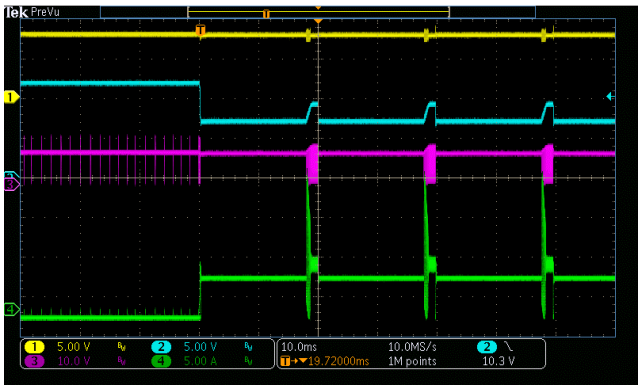

Figure 26. Over current protection (I_{LOAD}=5A)
CH1: VIN; CH2: VO; CH3: SW; CH4: IL

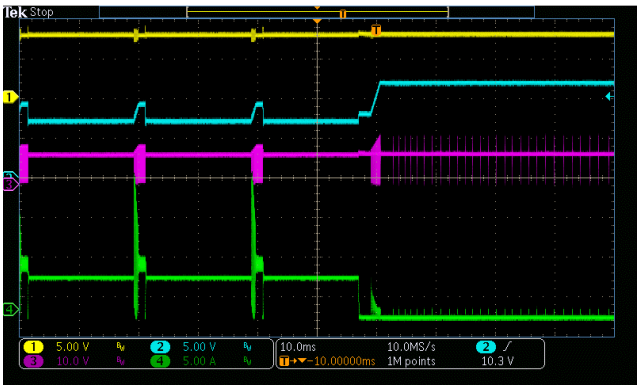

Figure 27. Over current recovery (I_{LOAD}=5A)
CH1: VIN; CH2: VO; CH3: SW; CH4: IL

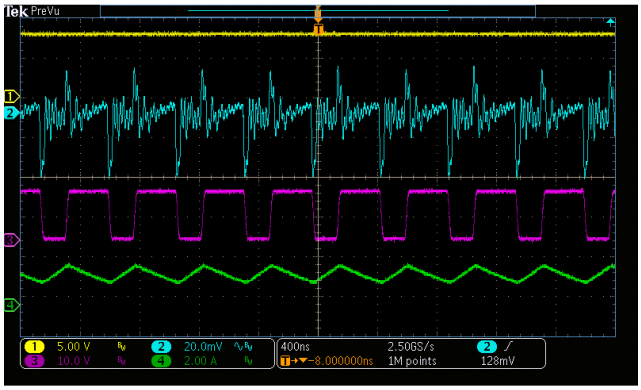

Figure 28. Steady-state (I_{LOAD}=1.6A)
CH1: VIN; CH2: VO/AC; CH3: SW; CH4: IL

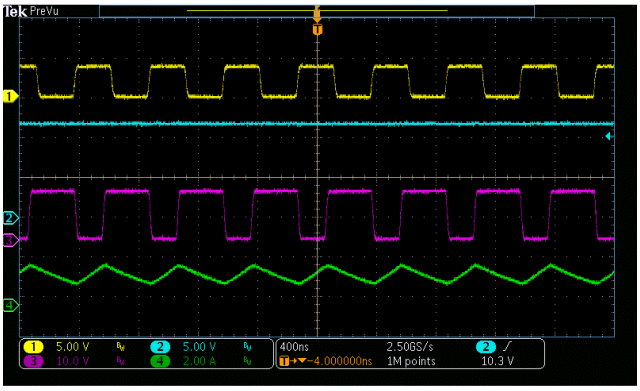

Figure 29. Sync Frequency
CH1: SYNC; CH2: VO; CH3: SW; CH4: IL

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APPLICATION INFORMATION

Typical Application (Sepic)

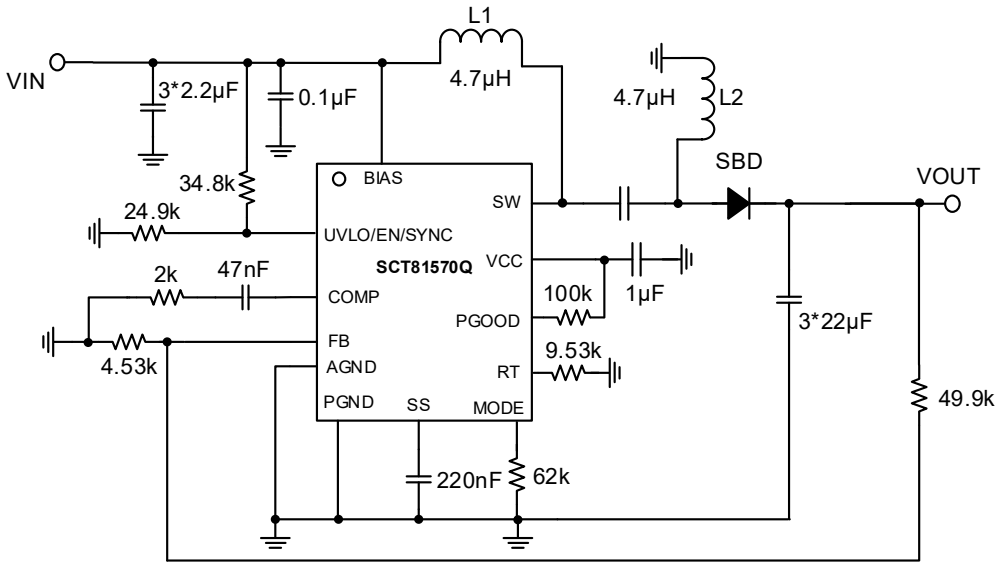

Figure 30. Application Schematic, 4V to 36V, 1A Sepic Regulator at 2100kHz

Design Parameters

Design Parameters	Example Value
Input Voltage	4V to 36V
Output Voltage	12V
Maximum Output Current	1A
Switching Frequency	2100 KHz
Output voltage ripple (peak to peak)	75mV (Load=1A)

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Inductor Selection (Sepic)

A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20% to 40% of the maximum input current at the minimum input voltage. The current ripple flowing in inductors L1 and L2 is given by:

$$\Delta I_{L1} = I_{IN} \times 40\% = I_O \times \frac{V_O}{V_{IN_MIN}} \times 40\% \quad (19)$$

$$\Delta I_{L2} = I_O \times 40\% = I_O \times 40\% \quad (20)$$

Normally we can select equal value for the inductors L1 and L2, derived as:

$$L_1 = L_2 = L = \frac{V_{IN_MIN}}{\Delta I_L \times f_{SW}} \times D_{MAX} \quad (21)$$

Where

- f_{SW} is the switching frequency.

Note that the saturation current of inductors should be greater than peak current flowing in inductors, given by:

$$I_{L1_PEAK} = I_{IN} + \frac{\Delta I_L}{2} = I_O \times \frac{V_O}{V_{IN_MIN}} \times (1 + \frac{40\%}{2}) \quad (22)$$

$$I_{L2_PEAK} = I_O + \frac{\Delta I_L}{2} = I_O \times (1 + \frac{40\%}{2}) \quad (23)$$

If L1 and L2 are wound in same core as a coupled inductor, the inductance required will be half due to the mutual induction, calculated by:

$$L_1 = L_2 = \frac{L}{2} = \frac{V_{IN_MIN}}{2 \times \Delta I_L \times f_{SW}} \times D_{MAX} \quad (24)$$

Power MOSFET Selection

The following parameters should be taken into consideration for MOSFET: the on-resistance R_{DS_ON}, the minimum gate threshold voltage V_{TH_MIN}, the total gate charge Q_g, the reverse transfer capacitance C_{RSS}, and the maximum drain to source voltage V_{Q_MAX}. The peak switching voltage between drain to source in a SEPIC is given by:

$$V_{SW_PEAK} = V_{IN} + V_O + V_D \quad (25)$$

Then the V_{Q_MAX} of power MOSFET should be greater than the peak switching voltage.

The peak switching current flowing through the MOSFET is given by:

$$I_{Q_PEAK} = I_{L1_PEAK} + I_{L2_PEAK} \quad (26)$$

The RMS current through the MOSFET I s calculated by:

$$I_{Q_RMS} = I_O \times \sqrt{\frac{\left(V_O + V_{IN_MIN} + V_D\right) \times \left(V_O + V_D\right)}{V_{IN_MIN}^2}} \quad (27)$$

Then power dissipation in MOSFET can be estimated by:

$$P_{DIS} = I_{Q_RMS}^2 \times R_{DS_ON} \times D_{MAX} + \left(V_O + V_{IN_MIN}\right) \times I_{Q_PEAK} \times \frac{Q_g \times f_{SW}}{I_G} \quad (28)$$

Where

I_G is the gate drive current.

The total power dissipation of MOSFET includes conduction loss as shown in the first term and switching loss as shown in the second term. The total power dissipation should be within package thermal ratings.

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Output Diode Selection

The diode at the output side must withstand the reverse voltage when the MOSFET is turned-on. The peak reverse voltage is given by:

$$V_{D_PEAK} = V_{IN_MAX} + V_{O_MAX} \quad (29)$$

The diode should also be capable to flow switch peak current I_{Q_PEAK}.

The power dissipation of the diode is equal to the forward voltage drop multiplies output current. Schottky diodes are recommended here to minimize the power loss.

Coupling Capacitor Selection

For ceramic capacitors with low-ESR, the peak to peak voltage ripple on coupling capacitor is estimated by:

$$\Delta V_{CS} = \frac{I_O \times D_{MAX}}{C_S \times f_{SW}} \quad (30)$$

The maximum voltage across the coupling capacitor is maximum input voltage. The voltage rating of the coupling capacitor must be greater than it.

The RMS current of coupling capacitor is given by:

$$I_{CS_RMS} = I_O \times \sqrt{\frac{V_O + V_D}{V_{IN_MIN}}} \quad (31)$$

There is a large RMS current through coupling capacitor relative to output power. Ensure the coupling capacitor can withstand it with good heat generation to have proper thermal performance.

Input Capacitor Selection

The SEPIC has an inductor at input side thus the input current is continuous and triangular. The RMS current flowing through the input capacitor is given by:

$$I_{IN_RMS} = \frac{\Delta I_{L1}}{\sqrt{12}} \quad (32)$$

Since input current ripple is relative low, the capacitance would be not too critical. While 100μF in total or higher value is strongly recommended in order to provide stable input supply.

Output Capacitor Selection

Similar to boost converter, the SEPIC output capacitor suffers large current ripple. The capacitance must be enough to provide the load current. The maximum voltage ripple in the output capacitor is:

$$\Delta V_{OUT} = \frac{I_O \times D_{MAX}}{C_{OUT} \times f_{SW}} + ESR \times \left(I_{L1_PEAK} + I_{L2_PEAK} \right) \quad (33)$$

Assuming ceramic capacitors are used here and ESR can be ignored, the output capacitor is given by:

$$C_{OUT} \geq \frac{I_O \times D_{MAX}}{\Delta V_{OUT} \times f_{SW}} \quad (34)$$

The output capacitor must have an enough RMS current rating to handle the maximum RMS current in the output capacitor, calculated by:

$$I_{COUT_RMS} = I_O \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} \quad (35)$$

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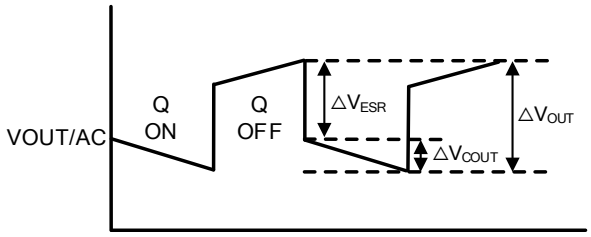

Figure 31. Output Voltage Ripple

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APPLICATION INFORMATION

Typical Application (Flyback)

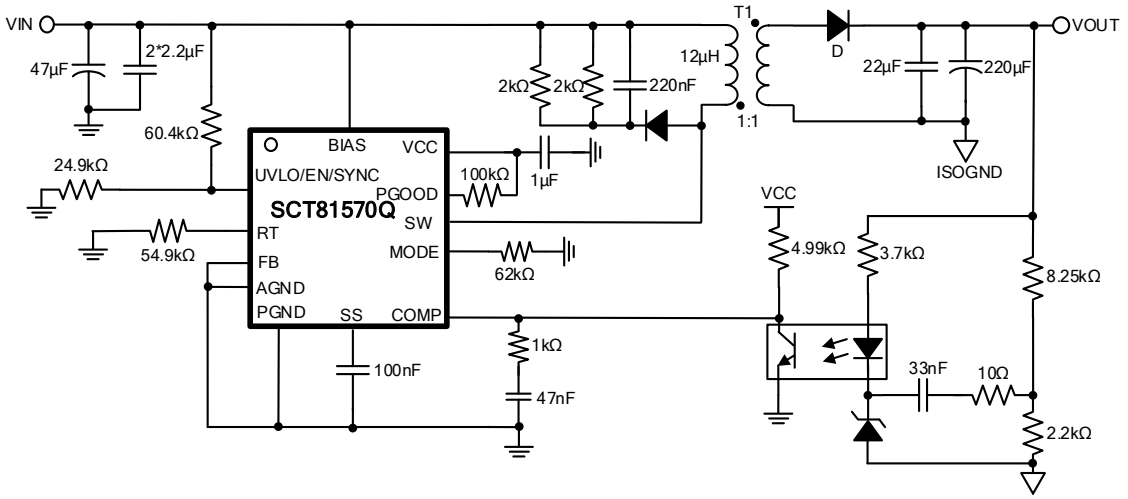

Figure 32. Application Schematic, 6V to 36V, 1A Flyback Regulator at 400kHz

Design Parameters

Design Parameters	Example Value
Input Voltage	6V to 36V
Output Voltage	12V
Maximum Output Current	1A
Switching Frequency	400 KHz
Output voltage ripple (peak to peak)	75mV (Load=1A)

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Transformer Selection (Flyback)

Transformer design is critical for flyback application. The first step is to select a proper operation mode. The discontinuous conduction mode (DCM) will minimize the transformer size at the cost of higher rating switch, while the continuous conduction mode (CCM) can achieve higher efficiency at full load and minimize output voltage ripple.

For DC-DC applications, where the input voltage is low, CCM operation is an attractive option to minimize the primary RMS current particularly in higher power systems even though the system's dynamic behavior is considerably difficult to maintain., it's easy to get the maximum duty cycle as below equation:

$$D_{MAX} = \frac{\frac{N_P}{N_S} \times V_O}{V_{IN_MIN} + \frac{N_P}{N_S} \times V_O} \quad (36)$$

where

- N_P is s the number of turns on the primary side winding
- N_S is s the number of turns on the secondary side winding

SCT recommends to determine the maximum duty cycle below 50%, which brings two benefit for flyback design: first, to get a stable loop, slope compensation is needed when duty cycle is larger than 50%. SCT81570Q also supports external additional slope compensation if duty cycle must be large to ease other designs. Second, the right-half plane zero of the modulator is pushed to high frequencies, helping to improve the load transient response and simplifying the control loop compensation calculations. Then the turns ration between primary side and secondary side N_{PS} can be determined accordingly.

The number of turns on the auxiliary winding is calculated using below equation:

$$N_{AUX} = N_S \times \frac{V_{AUX}}{V_O} \quad (37)$$

Assuming the efficiency of the flyback converter is η, the input power and output power relationship could be derived as shown in below equation:

$$V_{IN} \times I_{LM} \times D \times \eta = V_O \times I_O = P_O \quad (38)$$

where

- I_{LM} is the average current flowing in the transformer primary winding

The current increase of primary inductor during ON period is:

$$\Delta I_{LM} = V_{IN} \times \frac{D \times T_S}{L_P} \quad (39)$$

where

- L_P is the inductance of primary winding
- T_S is the switching period of flyback

Then the L_P can be derived as below equation:

$$L_P = \frac{V_{INMAX}^2 \times \eta}{K_L \times P_O \times f_S} \times \frac{V_O^2 \times N_{PS}^2}{\left(V_{INMAX} + V_O \times N_{PS}\right)^2} \quad (40)$$

where

- K_L is the ripple ratio

A maximum ripple ratio between 30% and 70% results in a good balance of the total power loss of the transformer, matching the down slope of the transformer current to the internal slope compensation and the increasing the right half plane zero frequency. The maximum ripple ratio of the inductor current is set to 60%. In CCM operation, the maximum primary winding ripple current occurs when the supply voltage is at the maximum value.

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The peak primary winding current occurs at the minimum supply voltage as below equation:

$$I_{L_PEAK} = I_{LM} + \frac{\Delta I_{LM}}{2} = \frac{P_O}{V_{INMIN} \times D_{MAX} \times \eta} + \frac{V_{INMIN} \times D_{MAX}}{2 \times L_P \times f_S} \quad (41)$$

The calculated turns ratio, primary winding inductance and peak current can be used to determine the magnetic core of the transformer, number of turns on primary and secondary windings, as well as wire thickness.

MOSFET and Diode Selection

The voltage rating of the MOSFET and the diode needs to be chosen with appropriate margin as both of them suffers from high voltage spike. In case of MOSFET, the primary leakage inductance resonates with output capacitance of MOSFET and similarly in case of diode, secondary leakage inductance resonates with diode capacitance and results into high voltage spikes. Considering the spike voltage, usually choose 1.5~2 times of the voltage stage as the voltage rating to ensure sufficient margin.

The voltage rating of MOSFET and Diode could be derived as shown in below equation:

$$V_{ds_MOS} = (1.5 \sim 2) \times \left(V_{IN_MAX} + \frac{N_P}{N_S} \times V_O \right) \quad (42)$$

$$V_{R_diode} = (1.2 \sim 1.5) \times \left(V_{IN_MAX} \times \frac{N_S}{N_P} + V_O \right)$$

The current RMS rating of MOSFET could be derived as shown in below equation:

$$I_{MOS_RMS} = \sqrt{D \times \left(\left(\frac{P_O}{V_{IN_MIN} \times D} \right)^2 + \frac{\Delta I_{LM}{}^2}{12} \right)} \quad (43)$$

The current rating of MOSFET and Diode should at least be I_{L_PEAK} and I_O respectively.

Output Capacitor Selection

The output capacitor is required to smooth the load voltage ripple, provides an energy source during load transients and provides energy to the load during the on-time of the MOSFET. A practical way to size the output capacitor is based on the required load transient specification. The load transient specification is related to the control loop crossover frequency. For this estimate it is expected that the control loop cross over frequency is set to 1/5th the right half plane zero frequency. This right half plane zero frequency is calculated using below equation:

$$f_{CROSS} = \frac{f_{RHZP}}{5} = \frac{N_P{}^2}{N_S{}^2} \times \frac{\frac{V_O{}^2}{P_O} \times (1-D)^2}{5 \times 2\pi \times L_M} \quad (44)$$

Then below equation is used to calculate the estimated load capacitance to achieve the specified load transient requirements.

$$C_O \geq \frac{\Delta I_O}{2\pi \times f_{CROSS} \times \Delta V_{RIPPLE}} \quad (45)$$

where

- ΔI_O is the difference in the load current conditions
- ΔV_{RIPPLE} is the specified overshoot voltage specification and undershoot voltage specification

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Input Capacitor Selection

The input capacitors smooth the supply ripple voltage during operation. Below equation is used to estimate the required input capacitor based on the supply ripple voltage specification.

$$C_{IN} \geq \frac{\frac{P_O}{V_{IN_MIN}} \times (1-D)}{f_{SW} \times \Delta V_{SUPPLY}} \quad (46)$$

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Application Waveforms

VBIAS=12V, Vout=12V, unless otherwise noted

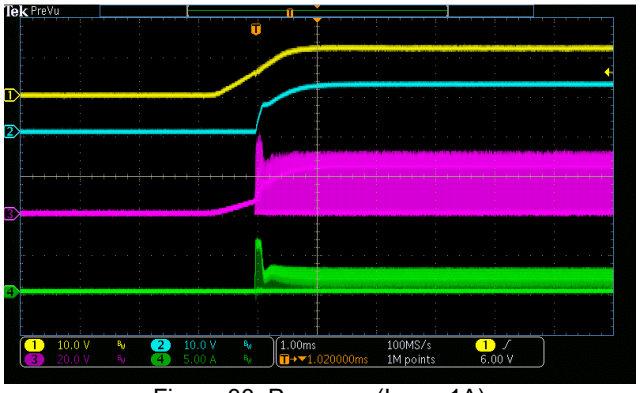

Figure 33. Power up (I_{LOAD}=1A)
CH1: VIN; CH2: VO; CH3: SW; CH4: IL

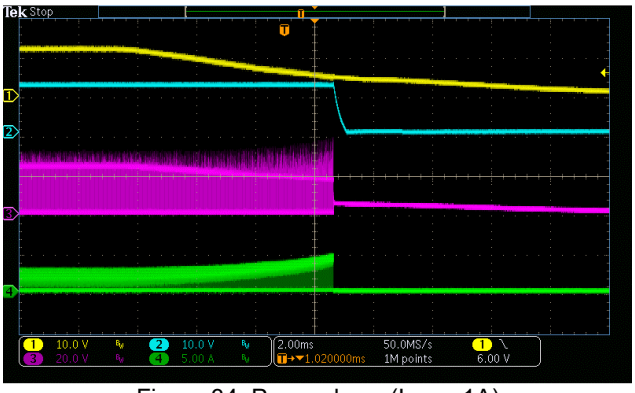

Figure 34. Power down (I_{LOAD}=1A)
CH1: VIN; CH2: VO; CH3: SW; CH4: IL.

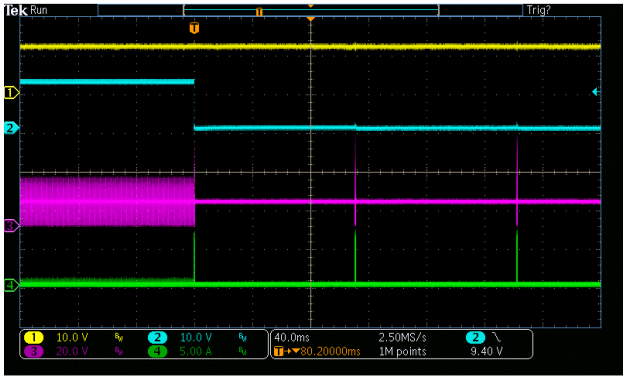

Figure 35. Over current protection (output short to GND)
CH1: VIN; CH2: VO; CH3: SW; CH4: IL

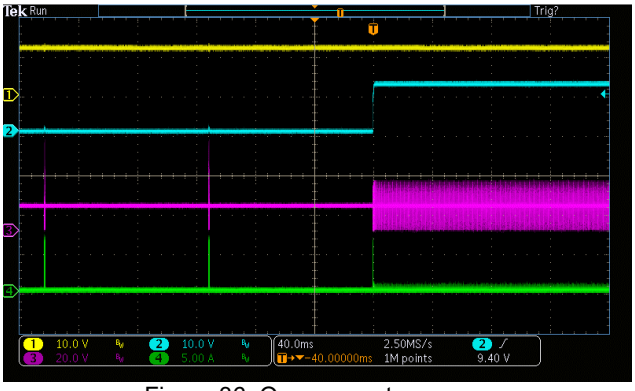

Figure 36. Over current recovery
CH1: VIN; CH2: VO; CH3: SW; CH4: IL

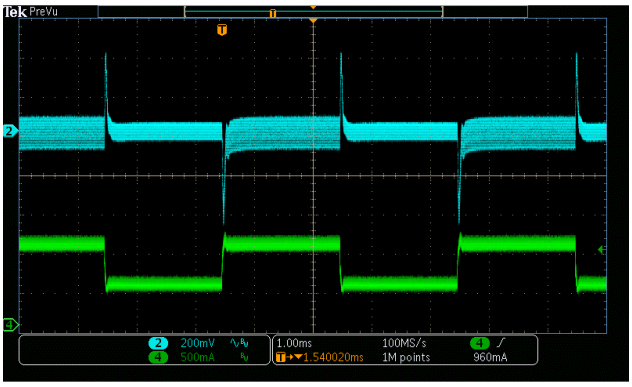

Figure 37. Load Transient (I_{LOAD}=0.5A-1A)
CH2: VO/AC; CH4: IO

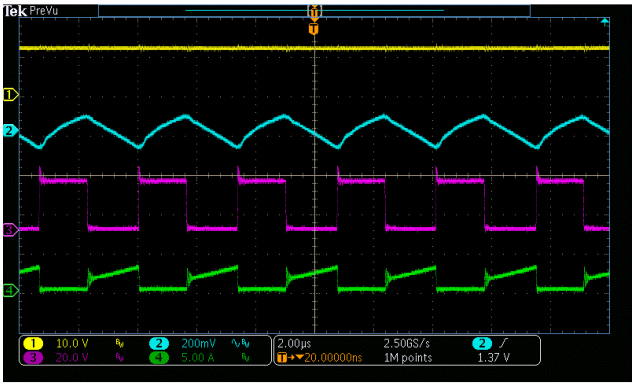

Figure 38. Steady-state (I_{LOAD}=1A)
CH1: VIN; CH2: VO/AC; CH3: SW; CH4: IL

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Layout Guideline

The performance of switching converters heavily depends on the quality of the PCB layout. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimize generation of unwanted EMI.

- Use a small size ceramic capacitor for C_{OUT}.
- Make the switching loop (C_{OUT} to D to SW to PGND to C_{OUT}) as small as possible.
- Leave a copper area near the D diode for thermal dissipation.
- Put the C_{VCC} capacitor as near the device as possible between the VCC and PGND pins.
- Connect the COMP pin to the compensation components.
- Connect the AGND pin directly to the analog ground plane. Connect the AGND pin to the UVLO, RT, SS and FB components.
- Connect the exposed pad to the AGND and PGND pins under the device.
- Add several vias under the exposed pad to help conduct heat away from the device. Connect the vias to a large ground plane on the bottom layer.

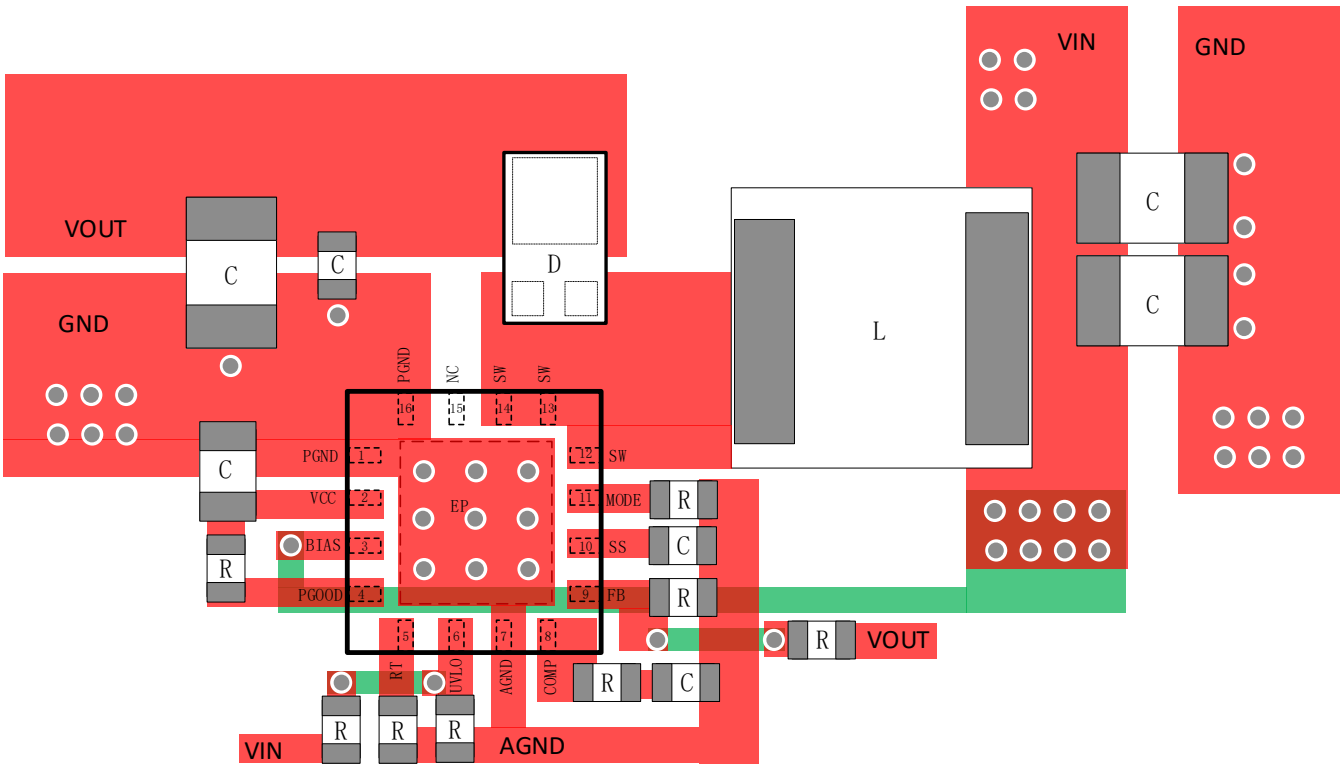

Figure 39. BOOST PCB Layout

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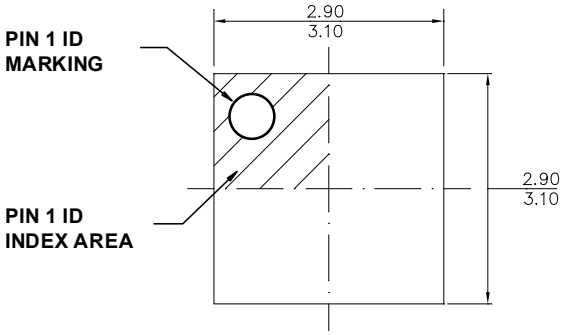
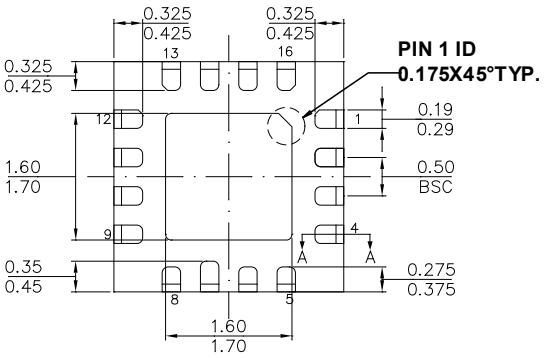
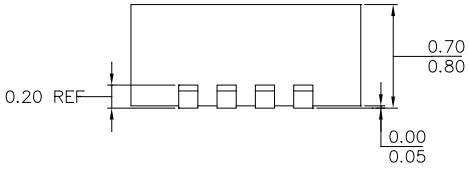
PACKAGE INFORMATION



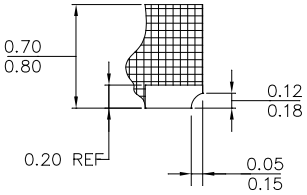
TOP VIEW



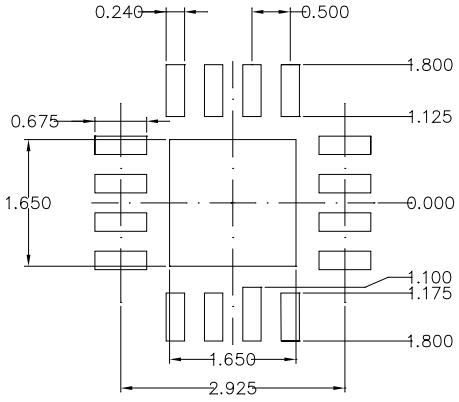
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

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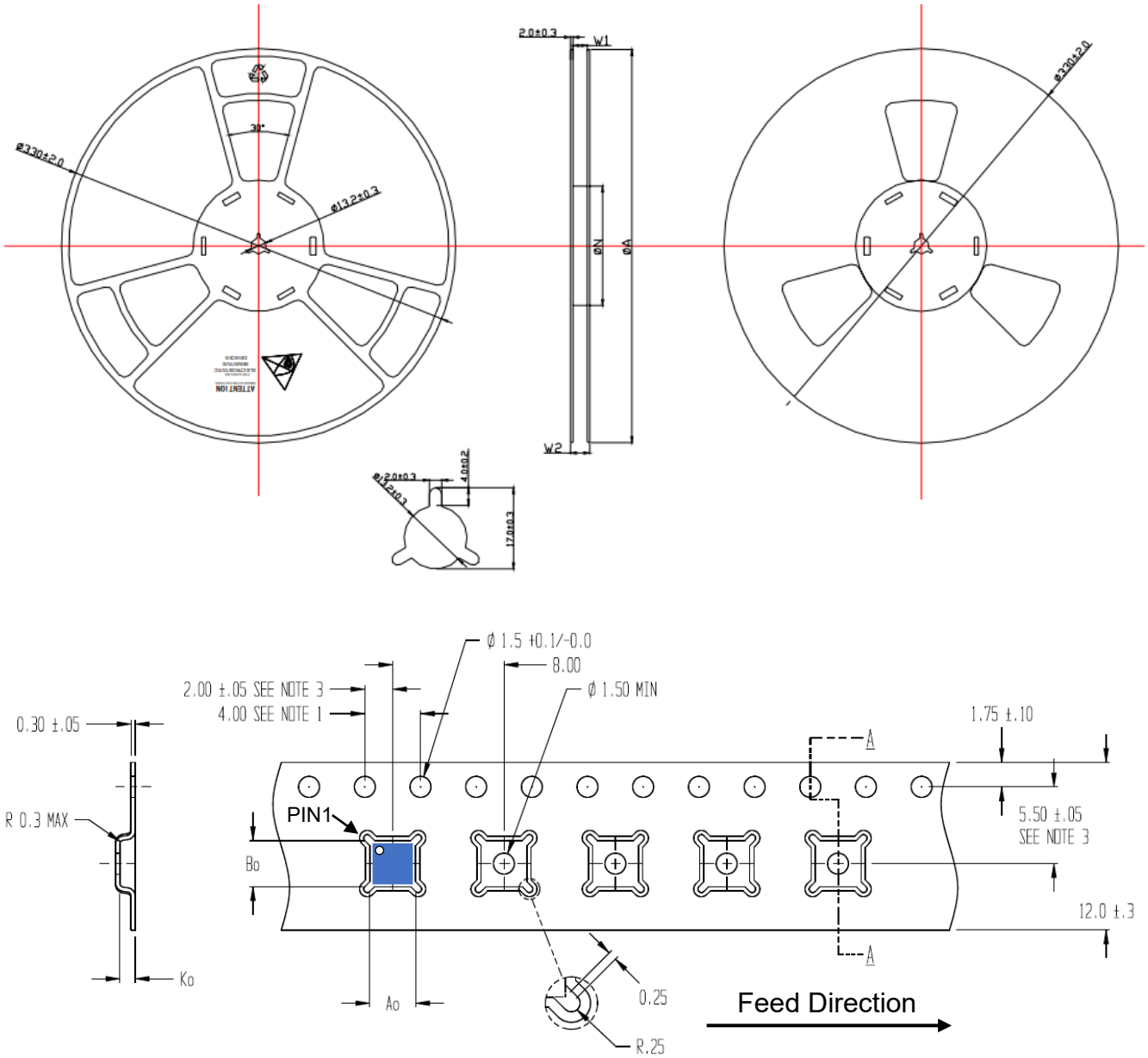
TAPE AND REEL INFORMATION



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