1.6V-5V Vin, 2A Output Current Buck-Boost Converter

FEATURES

- Integrated four power MOSFETs
- Input voltage range: 1.6V-5V
  (Input voltage > 1.65V if start-up with load)
- 1.2V to 5V output voltage range
- 1.0V output voltage is supported in PFM mode
- Up to 3A switch peak current limit
- Support 2A output current for V_{IN}≥3V, V_{OUT}=3.3V
- Support 1.5A output current for V_{IN}≥2.7V, V_{OUT}=3.3V
- 0.5V±1% feedback reference voltage
- Low shutdown current: 0.5μA
- Low quiescent operating current: 8μA
- Pulse frequency modulation (PFM) and forced CCM mode selectable
- 2MHz switching frequency
- 7.5ms internal soft-start time
- Active output discharge
- Supports V_{OUT} pre-bias start-up
- Integrated protection feature
  - Cycle-by-cycle current limit
  - Under-voltage Lockout
  - Input and output overvoltage protection
  - Thermal shutdown protection: 160°C
- WLCSP-8L (0.8725mm × 1.7725mm)

APPLICATIONS

- E-cigarette
- TWS earphones
- Battery-powered devices
- Wearable and portable devices

DESCRIPTION

The SCT3120 is a monolithic buck-boost converter with built-in internal power MOSFETs. The device achieves a peak output current of 2A from a 3V to 5V input voltage range, with excellent load and line regulation. The output voltage can be regulated down to as low as 1.0V in PFM mode.

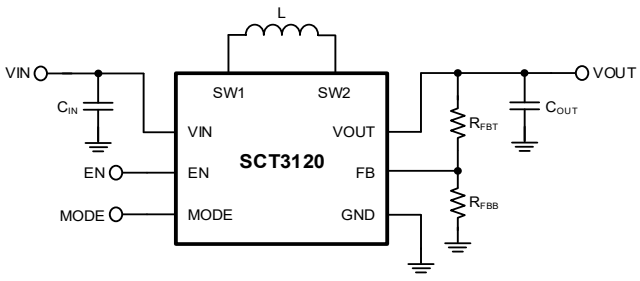
Depending on the input and output voltages, the SCT3120 automatically switches between boost, buck, or buck-boost operation when the input voltage approaches the output voltage. The transition between these modes occurs at predefined duty cycles, effectively preventing undesired toggling within modes, which minimizes output voltage ripple.

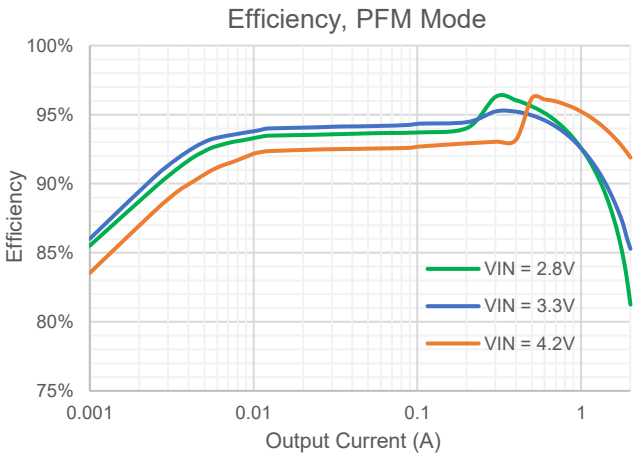
With a quiescent current of 8μA and a power-saving PFM mode, the SCT3120 ensures maximum efficiency even under light-load or no-load conditions.

The SCT3120 includes comprehensive protection features, such as overcurrent protection, short-circuit protection, input under-voltage lockout, output overvoltage protection, and thermal shutdown.

The SCT3120 requires only a minimal number of external components and is available in an ultra-compact Wafer Level Chip Scale Package (WLCSP) sized at 0.8725mm × 1.7725mm.

TYPICAL APPLICATION





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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 0.81: Preliminary Version

DEVICE ORDER INFORMATION

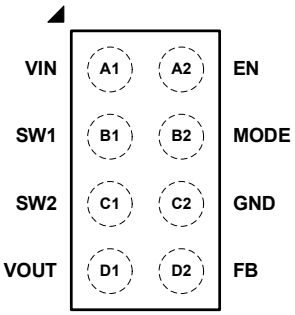
ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DISCRIPTION	MSL
SCT3120CTGR	Tape & Reel	3000	3120	8	WLCSP0.8725X1.7725-8L	3

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted (1)

DESCRIPTION	MIN	MAX	UNIT
VIN, VOUT, EN, MODE, FB	-0.3	6	V
SW1, SW2 (DC voltage)	-0.3	6	V
SW1, SW2 (Transient for <10ns)	-2	7	V
Junction temperature (2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

PIN CONFIGURATION



Top View: WLCSP0.8725X1.7725-8L

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 160°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	DESCRIPTION
VIN	A1	Power supply input. Must be locally bypassed with a capacitor as close as possible to the pin.
SW1	B1	Switching node of the buck stage.
SW2	C1	Switching node of the boost stage.
VOUT	D1	Buck-boost converter output. Connect the output capacitors as close to VOUT pin as possible.
FB	D2	Feedback input. Connect a resistor divider from VOUT to FB to set up output voltage.
GND	C2	Power ground. Must be connected directly to ground planes using multiple vias for improved thermal performance and electrical contact.
MODE	B2	PFM or FCCM mode selection. Ground the pin to operate the device in power save PFM mode. Connect the pin to VIN to force the device in Forced CCM operation mode. It must not be left floating.
EN	A2	Device enable. Set High to enable and Low to disable. It must not be left floating.

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RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted.

PARAMETER	DEFINITION	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	1.6	-	5	V
V_{OUT}	Output voltage range	1.2	-	5	V
C_{IN}	Effective input capacitance (1)	4	10	-	μF
C_{OUT}	Effective output capacitance (1)	8.7	17.5	330	μF
L	Effective inductance	0.7	1	1.3	μH
T_J	Operating junction temperature	-40	-	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM)	-2	+2	kV
	Charged Device Model (CDM)	-1	+1	kV

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	WLCSP-8L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance (2)	TBD	°C/W
$R_{\theta JC\ (top)}$	Junction to case (top) thermal resistance (2)	TBD	
$R_{\theta JB}$	Junction to board thermal resistance (2)	TBD	

(1) Effective capacitance accounts for DC bias derating in ceramic capacitors. The nominal capacitance (e.g., 47 μF) printed on the component label may be significantly higher than the actual capacitance under operating voltage. Refer to the manufacturer's "Capacitance vs. DC bias" to verify effective capacitance.

(2) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT3120 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT3120. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

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ELECTRICAL CHARACTERISTICS

V_{IN}=3.8V, V_{OUT}=3.3V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		1.6		5	V
V_{OUT}	Output voltage range		1.2		5	V
V_{IN_UVLO}	Input UVLO rising	V_{IN} rising	1.5	1.55	1.599	V
	Input UVLO falling	V_{IN} falling	1.4	1.45	1.499	V
	Hysteresis			100		mV
I_{SD}	Shutdown current from VIN	V_{EN}=0V		0.5	0.9	μA
I_Q	Quiescent current from VIN	V_{IN}=2.2V, V_{OUT}=3.3V, V_{EN}=2.2V, no load, no switching, V_{FB}=600mV		5	6.5	μA
	Quiescent current from VOUT			2.5	3.5	μA
Enable and MODE Selection						
V_{IH}	EN/MODE high threshold		0.81	0.93	1.1	V
V_{IL}	EN/MODE low threshold		0.6	0.7	0.8	V
V_{HYS}	EN/MODE hysteresis			200		mV
I_{LKG_H}	EN/MODE high-level input current	V_{EN}=V_{MODE}=1.5V		±0.01	±0.25	μA
I_{LKG_L}	EN/MODE low-level input current	V_{EN}=V_{MODE}=0V		±0.01	±0.1	μA
I_{EN_5V5}	EN high-level input current	V_{EN}=5.5V		±0.01	±0.3	μA
Reference						
V_{REF}	Reference voltage of FB		495	500	505	mV
Power MOSFETs						
R_{DSON_Q1}	MOSFET Q1 on-resistance	Test current=0.2A		45	55	mΩ
R_{DSON_Q2}	MOSFET Q2 on-resistance			50	65	mΩ
R_{DSON_Q3}	MOSFET Q3 on-resistance			50	65	mΩ
R_{DSON_Q4}	MOSFET Q4 on-resistance			50	65	mΩ
Output Discharge						
$R_{DISCHARGE}$	Output discharge resistance	V_{EN}=0V, V_{IN}=2.2V, V_{OUT}=3.3V		40		Ω
Current Limit						
I_{LIM_PK}	Internal peak current limit of MOSFET Q1	Output sourcing current, V_{IN}=3.8V, V_{OUT}=3.3V	2.6	3	3.35	A
		Output sinking current, V_{IN}=V_{OUT}=3.3V	-0.7	-0.55	-0.45	A
I_{PFM_ENTRY}	PFM mode entry threshold (peak) current	I_{OUT} falling		185		mA
Protection						
V_{IN_OV}	V_{IN} overvoltage threshold	V_{IN} rising	5.55	5.75	5.95	V
V_{OUT_OV}	V_{OUT} overvoltage threshold	V_{OUT} rising	5.55	5.75	5.95	V

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SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
T_{SD} (1)	Thermal shutdown threshold	T_J rising		160		°C
	Hysteresis			25		°C
Timing and Switching Frequency						
t_{EN_DELAY}	Delay between a rising edge on the EN pin and the start of the output voltage ramp			0.87	1.5	ms
t_{SS}	Soft-start ramp time		6.5	7.5	8.5	ms
f_{SW}	Switching frequency		1.8	2	2.2	MHz

(1) Guaranteed by sample characterization, not tested in production.

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TYPICAL CHARACTERISTICS

V_{IN}=2.8V to 4.2V, V_{OUT}=3.3V, T_A = 25°C, unless otherwise noted.

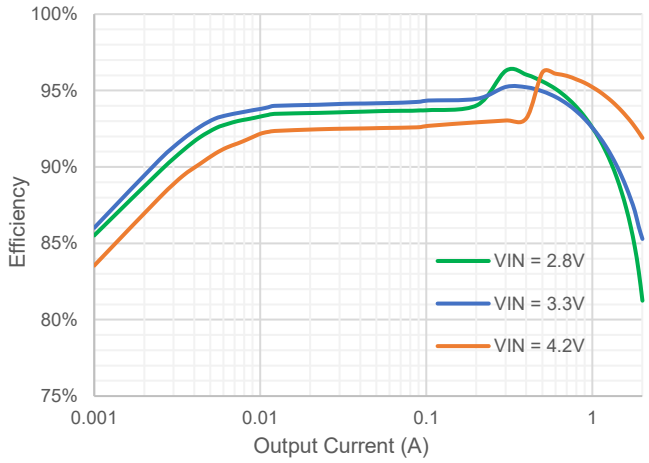

Figure 1. Efficiency vs Output Current (PFM)

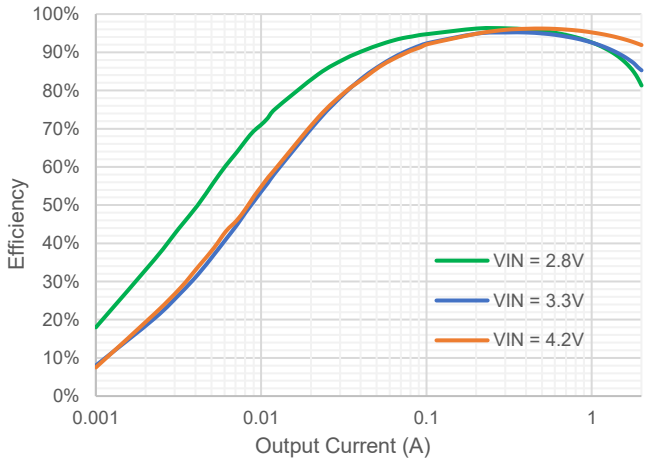

Figure 2. Efficiency vs Output Current (FCCM)

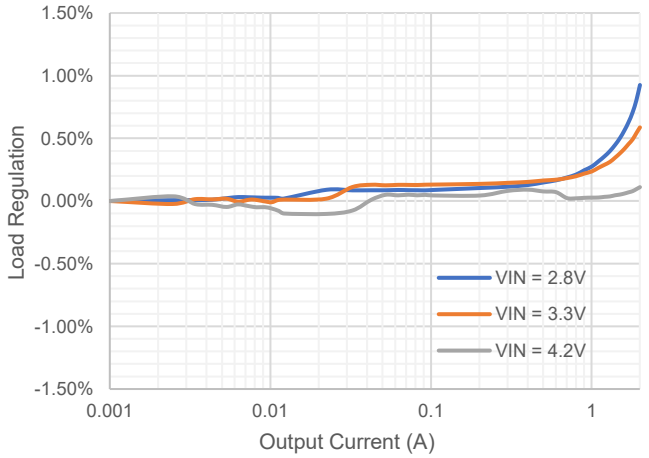

Figure 3. Load Regulation (PFM)

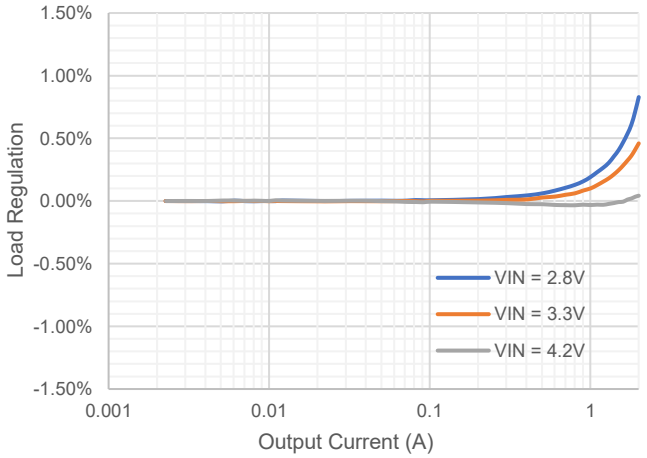

Figure 4. Load Regulation (FCCM)

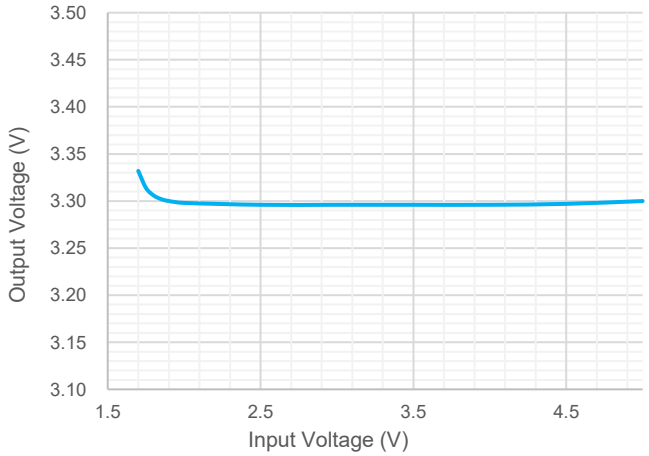

Figure 5. Line Regulation

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FUNCTIONAL BLOCK DIAGRAM

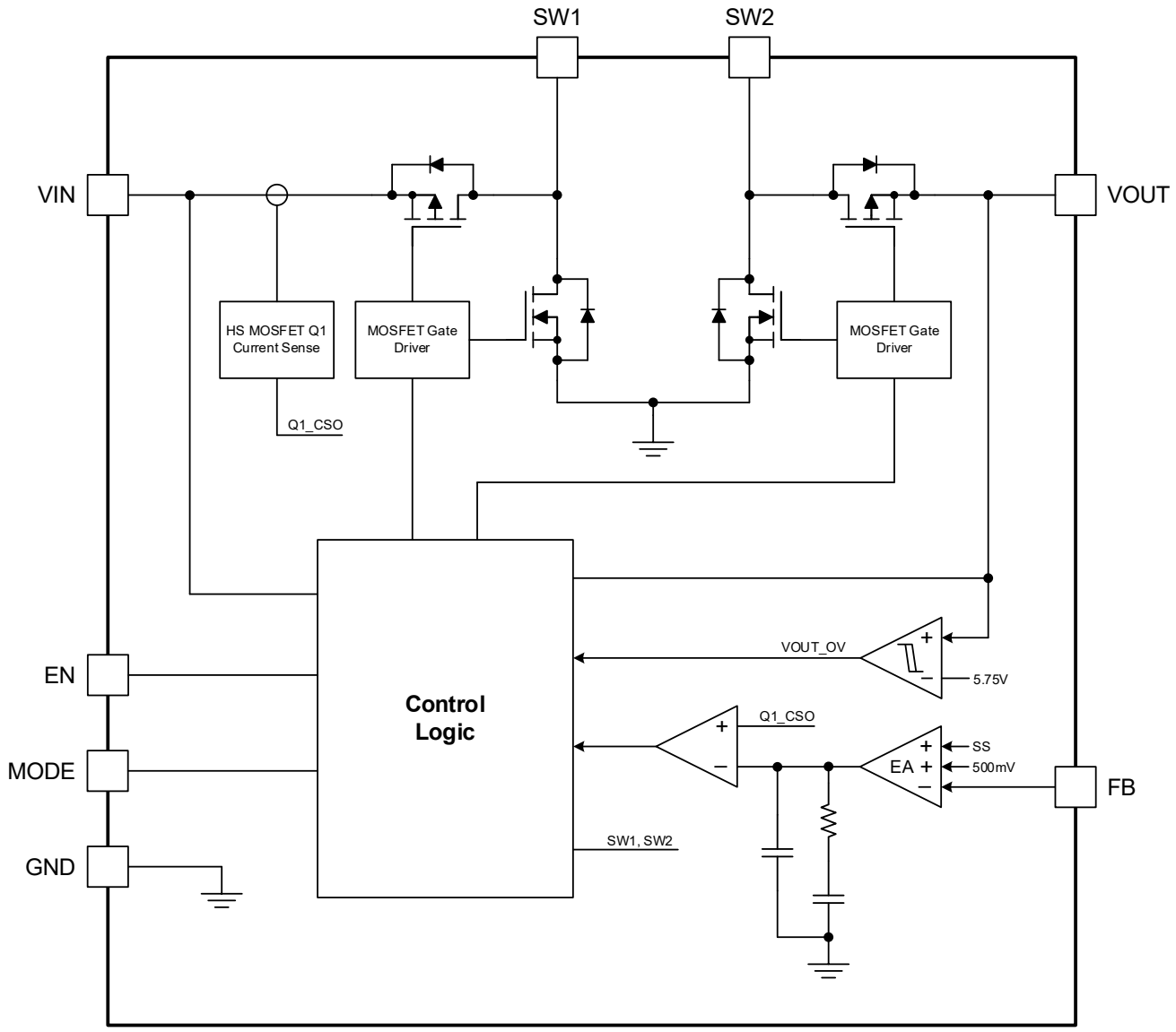

Figure 6. Functional Block Diagram

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OPERATION

Overview

The SCT3120 is a high-efficiency, monolithic buck-boost DC-DC converter designed for battery-powered and space-constrained applications. It integrates four low-$R_{DS(ON)}$ power MOSFETs and operates over a wide input voltage range of 1.6V to 5V, supporting output voltages from 1.0V (in PFM mode) up to 5V. The device seamlessly transitions between buck, boost, and buck-boost operating modes as the input voltage approaches or crosses the regulated output voltage, ensuring stable regulation with minimal output ripple.

Based on constant-frequency peak current-mode control architecture with a fixed 2MHz switching frequency, the SCT3120 delivers up to 2A continuous output current when V_{IN}≥3V and V_{OUT}=3.3V, and 1.5A when V_{IN}≥2.7V under the same output condition. A typical 3A switch peak current limit provides robust headroom for dynamic load transients.

Optimized for ultra-low power operation, the SCT3120 features a quiescent current of only 8μA in active mode and 0.5μA in shutdown, making it ideal for always-on or intermittent-use portable electronics. The device supports selectable operating modes: Pulse Frequency Modulation (PFM) for maximum light-load efficiency and forced Continuous Conduction Mode (CCM) for low-noise performance under medium-to-heavy loads.

Additional features include a 7.5ms internal soft-start to limit inrush current, active output discharge for rapid shutdown, and support for pre-biased output startup. Comprehensive protection mechanisms—such as cycle-by-cycle current limiting, input under-voltage lockout (UVLO), input/output overvoltage protection (OVP), and thermal shutdown at 160°C to ensure safe and reliable operation under abnormal conditions.

Housed in an ultra-compact WLCSP-8L package (0.8725mm × 1.7725mm), the SCT3120 minimizes external component count and PCB footprint, making it well-suited for applications such as TWS earphones, e-cigarettes, wearables, and other compact battery-operated devices.

Enable, UVLO and Soft Start

The SCT3120 starts operation when two conditions are met simultaneously:

- The input voltage on the VIN pin exceeds the UVLO rising threshold, and
- The EN pin voltage is above 1.1V.

The device continuously monitors VIN when not in shutdown. If VIN falls below the UVLO falling threshold, the converter immediately halts switching to prevent unstable operation during input brownout conditions. The UVLO detection includes de-glitching to avoid false triggering from transient input disturbances. When VIN recovers above the rising threshold, the device automatically restarts with a soft-start sequence. Notably, if the output retains a pre-biased voltage at this time, the startup process completes faster than a cold start.

Once enabled, the SCT3120 initiates startup after a short internal enable delay, T_{EN_DELAY}. An internal soft-start circuit limits inrush current during startup by clamping the inductor peak current to a reduced level I_{LIM_SS}. This current limit ensures controlled charging of the output capacitor while allowing the output voltage to rise smoothly. The total soft-start time is fixed at 7.5ms, ensuring reliable startup across a wide range of input voltages, output loads, and capacitance values.

The EN pin must not be left floating. To enable automatic startup when input power is applied, connect the EN pin directly to VIN.

Adjustable Output Voltage

The output voltage of the SCT3120 is set by an external resistor divider connected between VOUT, the FB pin, and GND. The converter regulates the FB pin to a typical reference voltage of 0.5V ±1% over the full operating temperature and input voltage range.

The output voltage is calculated using the following equation:

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$$R_1 = R_2 * \left(\frac{V_{OUT}}{V_{FB}} - 1\right) \quad (1)$$

Where:

- R_1 is the upper resistor (from VOUT to FB),
- R_2 is the lower resistor (from FB to GND),
- V_{FB}=0.5V (typical).

It is recommended that R2 be selected below or equal to 100kΩ to minimize sensitivity to FB pin bias current and improve output voltage accuracy. Using resistors with 1% tolerance or better is advised for tight output regulation.

Note that the minimum regulated output voltage is 1.2V in standard operation. However, 1.0V output is supported when the device operates in PFM mode, making it suitable for ultra-low-voltage applications such as MCU core supplies in deep-sleep states.

Mode Selection (PFM / Forced CCM)

The operating mode of the SCT3120 is controlled by the MODE pin:

When the MODE pin is pulled low (≤0.6V), the device operates in automatic PFM (Pulse Frequency Modulation) mode. In this mode, the converter dynamically switches between continuous conduction mode (CCM) at higher loads and PFM at light loads to maximize efficiency across the entire load range.

When the MODE pin is pulled high (≥1.1V), the device enters forced CCM (Continuous Conduction Mode), maintaining a fixed 2MHz switching frequency regardless of load current. This mode minimizes output voltage ripple and is preferred in noise-sensitive applications.

The MODE pin must not be left floating. For PFM operation, connect MODE directly to GND. For forced CCM operation, connect MODE to VIN or any logic-high signal above 1.1V.

Fixed-Frequency Operation

The SCT3120 operates at a fixed switching frequency of 2MHz, enabling compact external components and predictable EMI characteristics. The constant-frequency peak current-mode control architecture ensures stable loop dynamics and fast transient response across the full input and output voltage range.

Active Output Discharge

When the EN pin is pulled low, the SCT3120 activates an internal active discharge circuit that pulls the VOUT node to ground through a typical 40Ω discharge resistor. This feature rapidly discharges the output capacitor, preventing the output from floating during shutdown and ensuring clean power-down sequencing.

Caution should be exercised when using the SCT3120 in applications involving output power multiplexing or shared rails, as the discharge path creates a direct current sink to GND that may affect other connected supplies.

Reverse Current Capability

In forced CCM mode, the SCT3120 supports reverse current operation, allowing current to flow from the VOUT pin back to the VIN pin when the feedback voltage exceeds the internal reference (e.g., due to an external bias on VOUT). This behavior is inherent to the buck-boost topology and remains functional across all operating modes including buck, boost, and buck-boost, regardless of the VIN/VOUT ratio.

This capability enables seamless operation in systems where the output may be pre-biased or driven externally during startup or fault conditions.

Protection Features

The SCT3120 integrates comprehensive protection mechanisms to ensure robust and reliable operation under abnormal conditions.

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Input Overvoltage Protection (VIN_OVP)

If the input voltage exceeds the internal OVP threshold (typically triggered by reverse energy flow from VOUT to VIN), the device disables forced CCM operation and blocks reverse current to protect upstream circuitry. Normal operation resumes once VIN falls below the hysteresis threshold.

Output Overvoltage Protection (VOUT_OVP)

An internal comparator monitors the FB pin voltage. If VOUT rises above 5.75V, the power stage is immediately disabled, placing the SW nodes in high-impedance state to prevent damage from feedback failure or transient overshoot.

Cycle-by-Cycle Current Limit

The converter implements cycle-by-cycle peak current limiting on the high-side switch to prevent inductor current runaway during overload or output short-circuit events.

Thermal Shutdown

An on-chip thermal sensor monitors the die temperature. If the junction temperature reaches 160°C, the device shuts down all internal power switches. Operation automatically resumes once the temperature drops below the thermal hysteresis threshold (typically ~135°C), initiating a new start-up cycle.

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APPLICATION INFORMATION

Typical Application

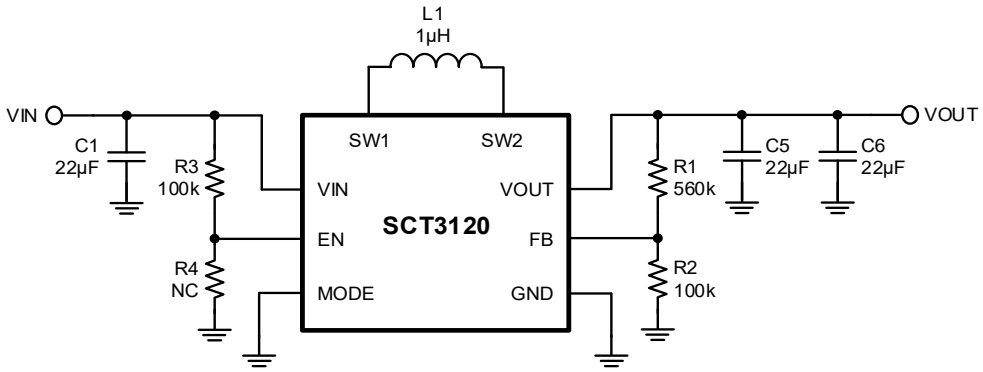

Figure 7. SCT3120 Design Example, 3.3V Output Voltage

Design Parameters

Design Parameters	Example Value
Input Voltage	3.8V Normal, 2.7V to 5V
Output Voltage	3.3V
Maximum Output Current	2A for V_{IN}≥3V 1.5A for V_{IN}≥2.7V
Operating mode	Automatic PFM mode
Output voltage ripple (peak to peak)	30mV

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Output Voltage

The output voltage is set by an external resistor divider R1 and R2 in Typical Application schematic. Recommended R2 resistance is below or equal to 100kΩ. Use Equation 2 to calculate R1.

$$R_1 = R_2 * \left(\frac{V_{OUT}}{V_{FB}} - 1\right) \quad (2)$$

where:

- V_{FB} is the feedback reference voltage, typical 0.5V.

Table 1. R_1, R_2 Value for Common Output Voltage (Room Temperature)

V_{OUT}	R_1	R_2
1.8V	237kΩ	91kΩ
2.5V	365kΩ	91kΩ
3.3V	560kΩ	100kΩ
3.5V	604kΩ	100kΩ
3.6V	620kΩ	100kΩ
5V	909kΩ	100kΩ

Mode Selection

In the Typical Application schematic, the MODE pin is connected to GND, selecting Automatic PFM mode. This mode delivers lower quiescent current and higher efficiency under light-load conditions by automatically transitioning between continuous conduction mode (CCM) at higher loads and pulse frequency modulation (PFM) at light loads.

To select Forced CCM mode—which maintains a fixed 2MHz switching frequency and provides lower output voltage ripple at light load, connect the MODE pin to VIN or any logic-high signal above 1.1V.

Under Voltage Lock-Out

In the Typical Application schematic, a 100kΩ resistor R3 is connected between VIN and EN to automatically enable the SCT3120 once the input voltage exceeds the V_{IN_UVLO} threshold. This configuration ensures the device powers up whenever sufficient input voltage is present.

The EN pin must not be left floating. A pull-down resistor (R4, from EN to GND) is included in the schematic as an optional component. If the system uses an external controller (e.g., an MCU) to manage power sequencing or on/off control, it is strongly recommended to:

- Leave R3 unpopulated (NC), and
- Install R4=100kΩ and
- Drive EN directly from the MCU. High level to enable and low level to disable the SCT3120.

This prevents undefined states due to EN pin floating and ensures reliable enable/disable behavior under all operating conditions.

Inductor Selection

The SCT3120 is optimized for operation with a 1μH power inductor. This value has been carefully selected to balance efficiency, output voltage ripple, load transient response, and loop stability across the full input and output voltage range. Use of other inductance values is not recommended, as it may degrade performance or compromise reliability.

When selecting the 1μH inductor, the following parameters must be considered:

- **Saturation Current (I_{SAT}):**

  The inductor must have a saturation current rating higher than the peak switch current limit of the SCT3120 (typically 3A). To ensure robust operation under all conditions—including startup, load transients, and overcurrent events, it is recommended to choose an inductor with I_{SAT}≥4A.

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- **RMS Current Rating:**

  The RMS current through the inductor depends on the output load and ripple. For worst-case estimation at maximum load (e.g., 2A output), the RMS current typically remains below 2.5A. Select an inductor rated for I_{RMS}≥2.5A.

- **DC Resistance (DCR):**

  Low DCR minimizes conduction losses and improves efficiency, especially at high load currents. A DCR below 50mΩ is preferred.

- **Core Material and Package:**

  Use shielded, low-loss ferrite-core inductors in compact packages such as 2.5mm×2.0mm×1.2mm or 2.0mm×1.6mm×1mm. Shielded types reduce EMI and are less susceptible to external magnetic fields.

Table 2. Recommended Inductors Options

Value	Saturation Current	DCR	Part Number (1)	Manufacturer (1)	Size (mm)
1μH	6A	22mΩ	FTC252012S1R0MBCD	Cjiang	2.5×2.0×1.2
1μH	4.7A	40mΩ	DFE252012F-1R0M=P2	MuRata	2.5×2.0×1.2
1μH	4.1A	48mΩ	DFE252010F-1R0M=P2	MuRata	2.5×2.0×1.0
1μH	4.2A	36mΩ	FTC201610S1R0MBCD	Cjiang	2.0×1.6×1.0
1μH	4.2A	43mΩ	HTEK20161T-1R0MSR	Cyntec	2.0×1.6×1.0
1μH	4A	48mΩ	DFE201612E-1R0M=P2	MuRata	2.0×1.6×1.2

(1) The listed components are provided for reference only. Silicon Content Technology (SCT) does not endorse or guarantee their suitability, performance, or reliability. Users are responsible for verifying the suitability and performance of any third-party component in their specific application.

Output Capacitor Selection

The SCT3120 is designed to operate with a nominal output capacitance of 44μF, which can be implemented using either a single 47μF or two parallel 22μF X5R/X7R ceramic capacitors. Both configurations ensure that the effective capacitance remains above the minimum required 8.7μF across the full output voltage range, accounting for DC bias derating. This capacitance level provides an optimal balance among load transient response, output voltage ripple, and stability in all operating modes (buck, boost, and buck-boost).

Due to significant capacitance reduction under DC bias, always select capacitors with a voltage rating at least 1.5× the maximum expected V_{OUT}. For example, for a 5V output, use 10V rated capacitors—avoid operating 6.3V parts at their absolute voltage limit.

Place the output capacitor(s) as close as possible to the VOUT and GND pins to ensure effective high-frequency decoupling. If additional bulk capacitance (e.g., polymer or electrolytic) is used for extreme load transients, it must be paralleled with at least one ceramic capacitor (≥22μF) located directly adjacent to the IC.

Recommendation:

- One 47μF, 0805 size, 6.3V or 10V X5R/X7R ceramic capacitor, or
- Two 22μF, 0603 size, 6.3V or 10V X5R/X7R ceramic capacitors.

Input Capacitor Selection

A nominal input capacitance of 22μF using an X5R or X7R ceramic capacitor is recommended to suppress input voltage ripple and improve EMI performance. As with the output side, account for DC bias derating by selecting a capacitor with a voltage rating at least 1.5× the maximum VIN (e.g., a 10V capacitor for a 5V maximum input).

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For best performance:

- Place the input capacitor directly between the VIN and GND pins with minimal trace length.
- If the power source is more than a few centimeters away, consider adding bulk capacitance (e.g., 47μF tantalum or polymer) near the board entry point—but never omit the local 22μF ceramic bypass capacitor.

Recommendation:

- One 22μF, 0603 or 0805 size, 6.3V or 10V X5R/X7R ceramic capacitor, or
- Two 10μF, 0603 size, 6.3V or 10V X5R/X7R ceramic capacitors.

Table 3. Recommended Capacitors Options

Function	Value (1)	Voltage	Dielectric	Size	Part Number (2)	Manufacturer (2)
C_{IN}	22μF	10V	X5R	0603	GRM188R61A226ME15	MuRata
C_{OUT}	47μF	6.3V	X5R	0805	GRM21BR60J476ME11	MuRata
C_{OUT}	22μF	6.3V	X5R	0603	GRM188R60J226ME15	MuRata
C_{OUT}	22μF	10V	X5R	0603	C1608X5R1A226M080AC	TDK

(1) The effective capacitance of ceramic capacitors can drop by 50% or more at rated voltage. Always verify the actual capacitance at operating bias using manufacturer DC bias curves.
(2) The listed components are provided for reference only. Silicon Content Technology (SCT) does not endorse or guarantee their suitability, performance, or reliability. Users are responsible for verifying the suitability and performance of any third-party component in their specific application.

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Application Waveforms

V_{IN}=2.5V to 5V, V_{OUT}=3.3V, unless otherwise noted

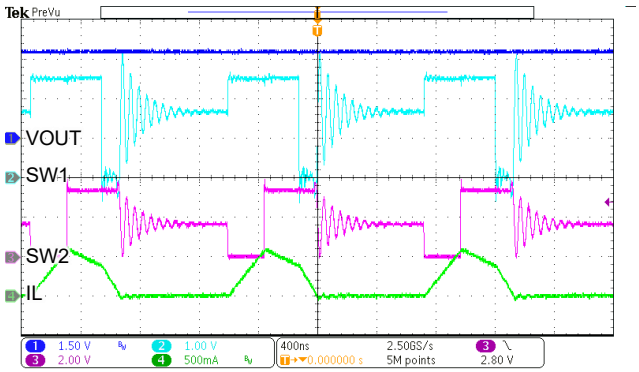

Figure 8. Steady state, Boost Operation
(V_{IN}=2.5V, I_{LOAD}=0.1A, PFM)

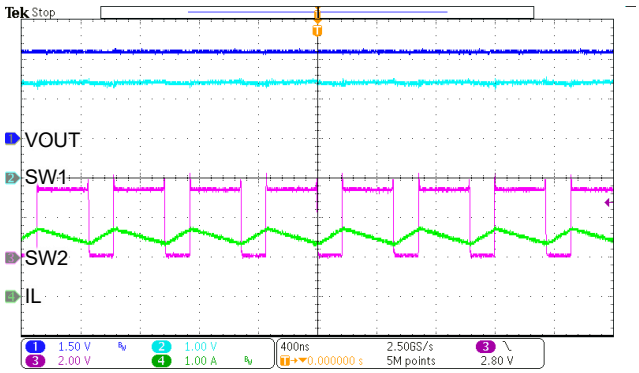

Figure 9. Steady state, Boost Operation
(V_{IN}=2.5V, I_{LOAD}=1A, PFM)

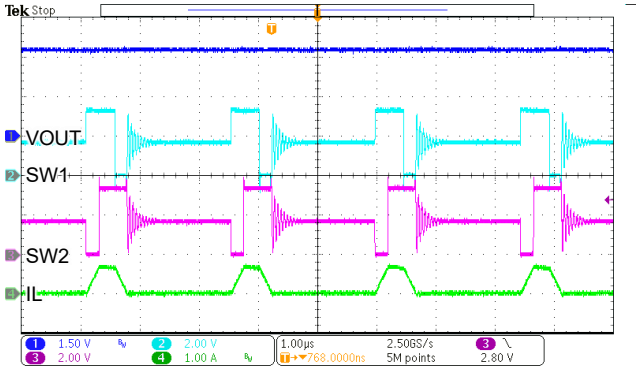

Figure 10. Steady state, Buck-Boost Operation
(V_{IN}=3.3V, I_{LOAD}=0.1A, PFM)

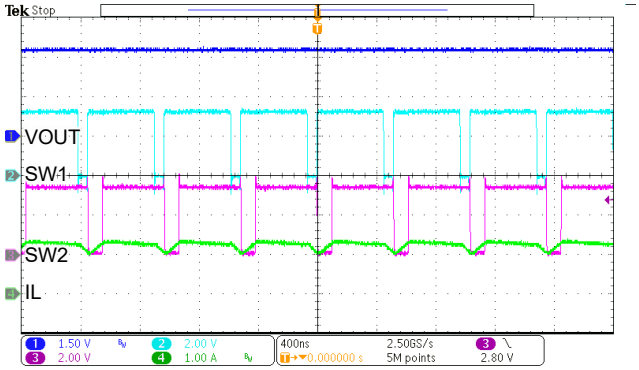

Figure 11. Steady state, Buck-Boost Operation
(V_{IN}=3.3V, I_{LOAD}=1A, PFM)

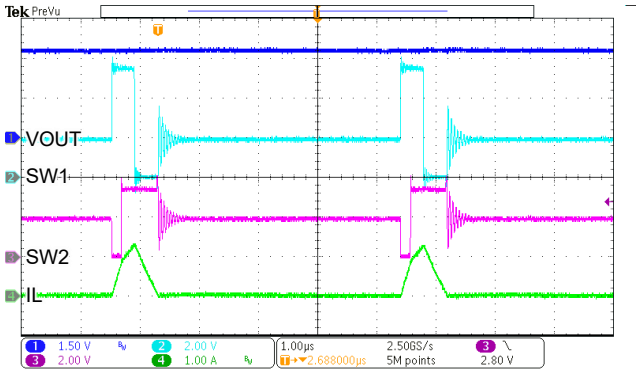

Figure 12. Steady state, Buck Operation
(V_{IN}=5V, I_{LOAD}=0.1A, PFM)

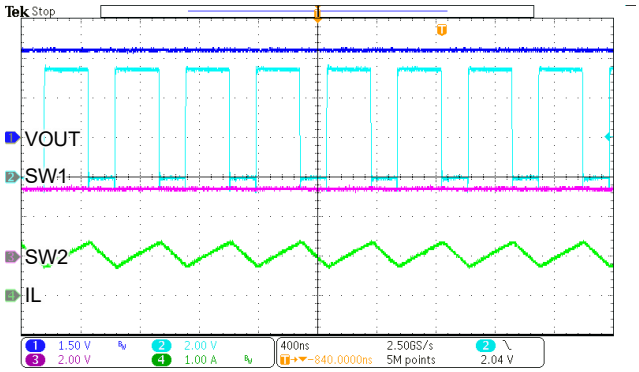

Figure 13. Steady state, Buck Operation
(V_{IN}=5V, I_{LOAD}=1A, PFM)

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Application Waveforms (continued)

V_{IN}=2.5V to 5V, V_{OUT}=3.3V, unless otherwise noted

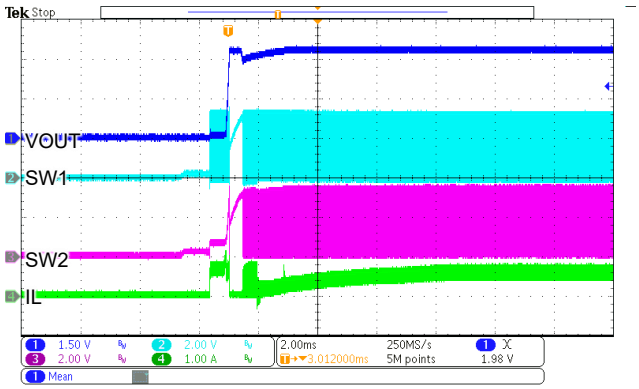

Figure 14. VIN Power up, Buck-Boost Operation
(V_{IN}=3.3V, I_{LOAD}=0.5A, PFM)

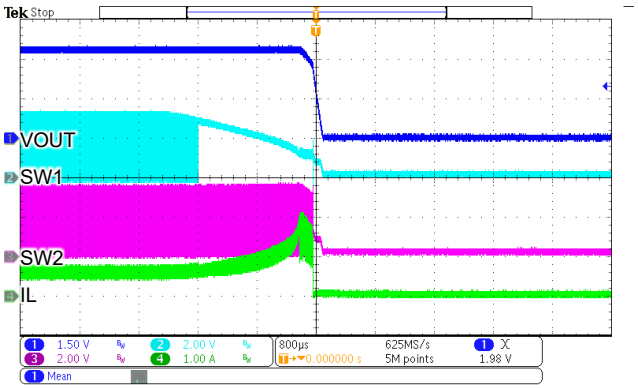

Figure 15. VIN Power down, Buck-Boost Operation
(V_{IN}=3.3V, I_{LOAD}=0.5A, PFM)

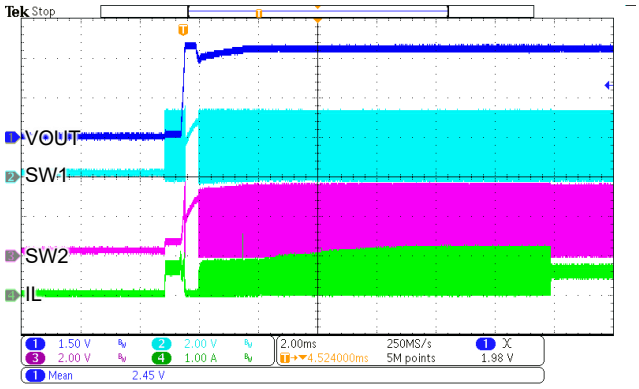

Figure 16. EN Power up, Buck-Boost Operation
(V_{IN}=3.3V, I_{LOAD}=0.5A, PFM)

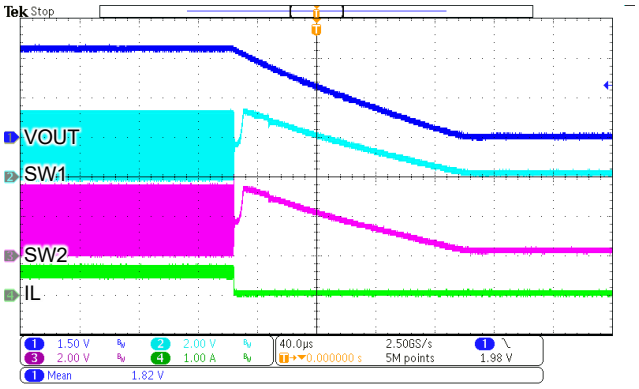

Figure 17. EN Power down, Buck-Boost Operation
(V_{IN}=3.3V, I_{LOAD}=0.5A, PFM)

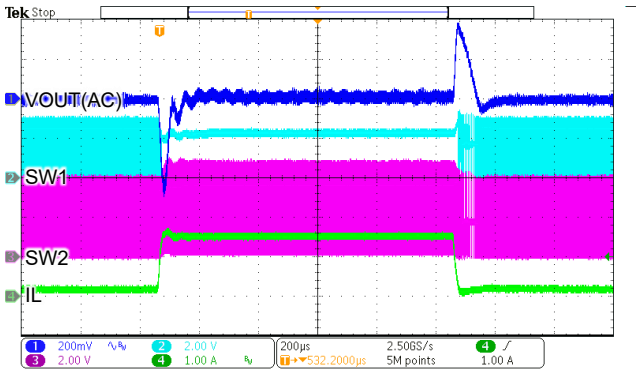

Figure 18. Load transient, Boost Operation
(V_{IN}=2.5V, I_{LOAD}=0.15A-1.5A, 1A/µs)

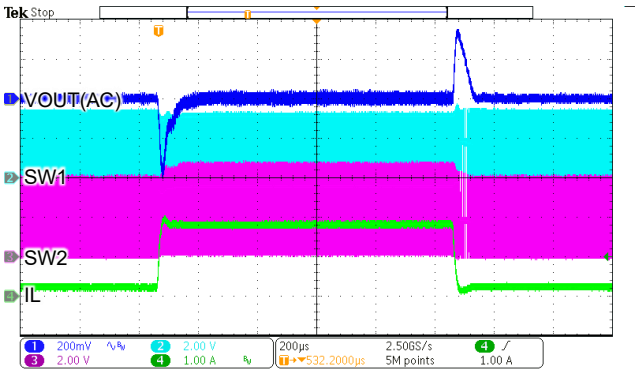

Figure 19. Load transient, Buck-Boost Operation
(V_{IN}=3.3V, I_{LOAD}=0.2A-1.8A, 1A/µs)

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Application Waveforms (continued)

V_{IN}=2.5V to 5V, V_{OUT}=3.3V, unless otherwise noted

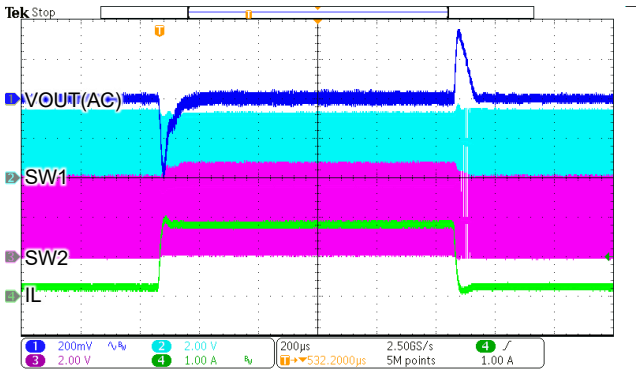

Figure 20. Load transient, Buck Operation
(V_{IN}=5V, I_{LOAD}=0.2A-1.8A, 1A/µs)

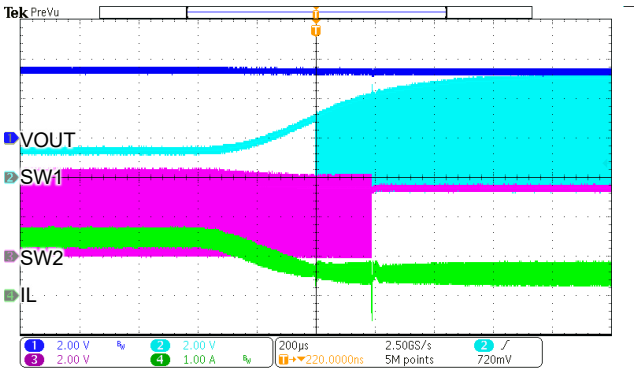

Figure 21. Mode transition, Boost → Buck-Boost → Buck
(V_{IN}=1.6V→5V, I_{LOAD}=0.5A, FCCM)

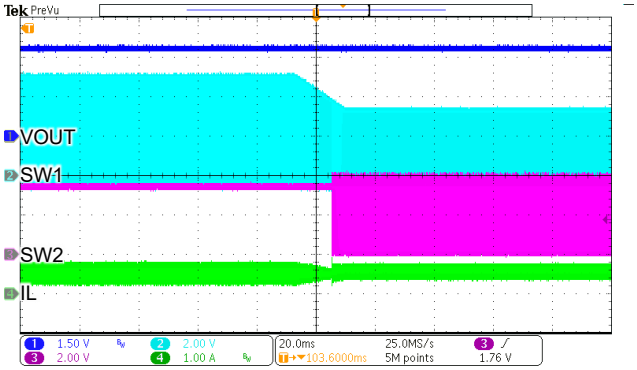

Figure 22. Mode transition, Buck → Buck-Boost
(V_{IN}=5V→3.3V, I_{LOAD}=0.5A, FCCM)

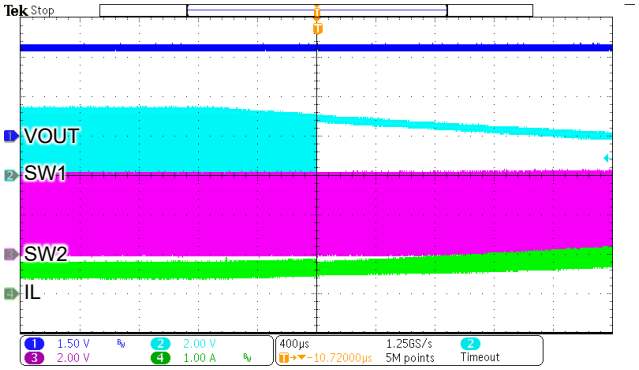

Figure 23. Mode transition, Buck-Boost →Boost
(V_{IN}=3.3V→1.6V, I_{LOAD}=0.5A, FCCM)

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Layout Guidelines

The performance of switching converters heavily depends on the quality of the PCB layout. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimize generation of unwanted EMI.

1. Minimize the high di/dt switching loop area.
2. Place both C_{IN} (22 µF) and C_{OUT} (47 µF or 2×22 µF) as close as possible to the VIN, VOUT, and GND pins.
3. Provide a continuous ground plane on the inner or bottom layer, connected to the GND pins using multiple vias. This improves thermal performance, reduces EMI, and minimizes ground bounce.
4. Use multiple vias on the VIN, VOUT, and GND pins to transfer heat to inner or bottom layers.
5. Keep sensitive traces away from switching nodes: Route the FB feedback trace away from the SW1/SW2 pin and inductor (L) to avoid noise coupling. Keep FB traces short and use a ground guard if necessary.

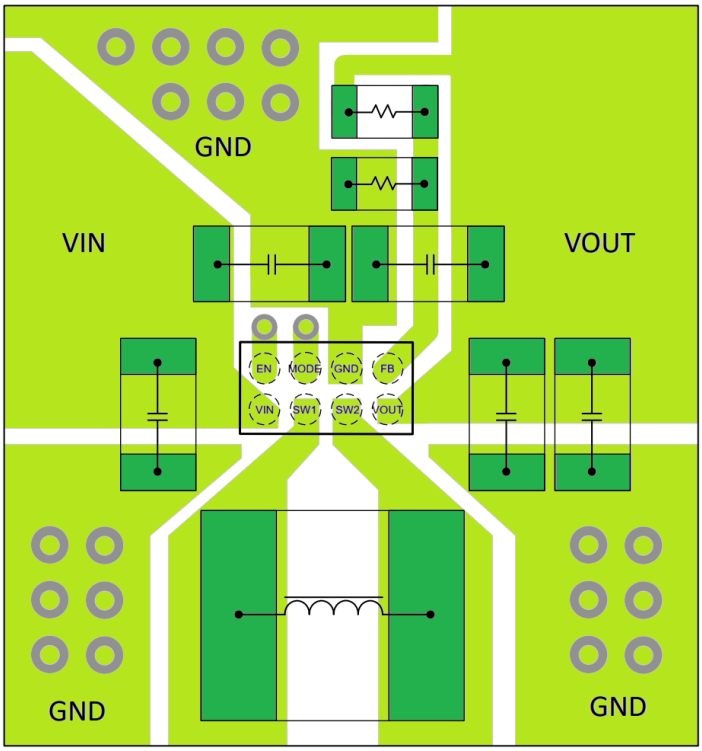

Figure 24. PCB Layout Example, Top Layer

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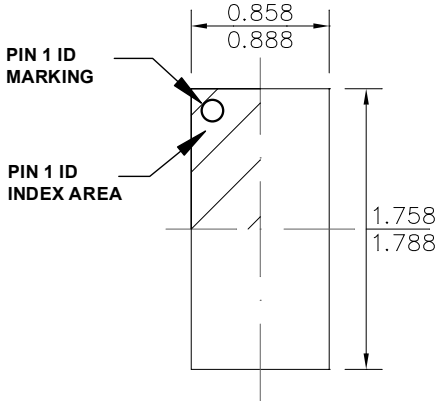
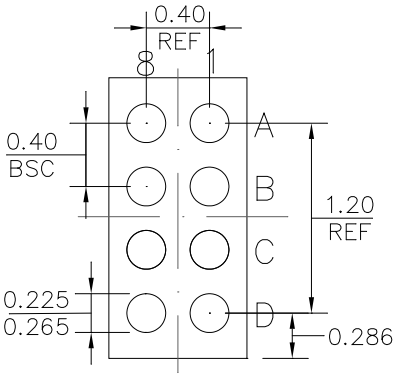
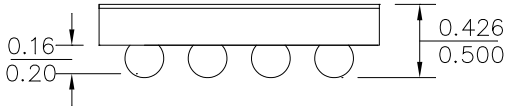
PACKAGE INFORMATION



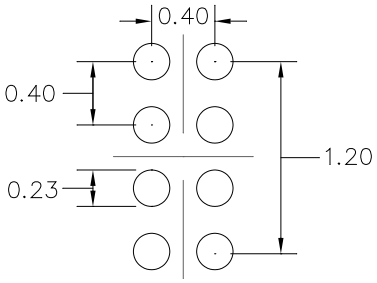
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211, VARIATION BC.
4) DRAWING IS NOT TO SCALE.

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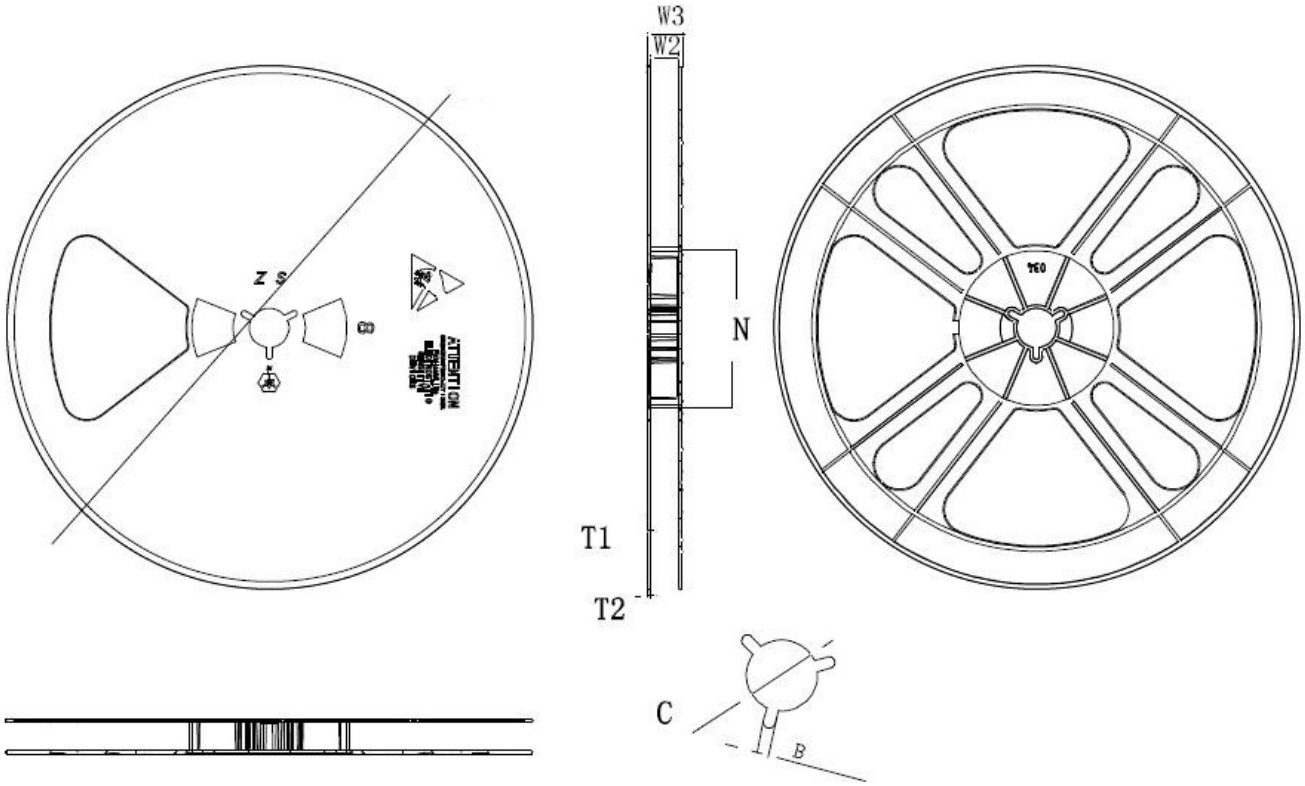
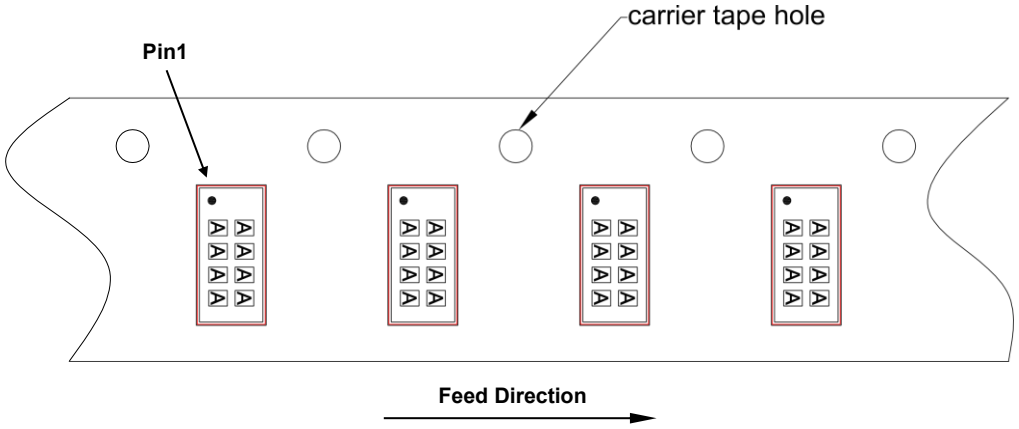
TAPE AND REEL INFORMATION



Dimension	A	B	C	N	T1	T2	W2	W3
Millimeters (mm)	179±1	2.0±0.2	13.5±0.2	54.8±0.2	1.2±0.2	1.5±0.2	9.0±0.2	9.2±0.2



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