芯 洲 科 技
Silicon Content Technology

PRODUCT RELIABILITY REPORT

Product: SCT2613TVBR

Package & Reliability Department
Silicon Content Technology

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1. Device Information

Product:	SCT2613TVBR
Package:	TSOT236
Process Technology:	BCD
Report Date:	2023.08.14

2. Summary of Test Results

Test	Test Condition	Lot# or Date Code	Test Results (S.S./Rej)*lots	Comment
Temperature, Bias, and Operating Life (HTOL)	JESD22-A108, @+125 ℃, Vcc=60V for 1000 hours	1037651	(79/0)*1	
ESD: Device Charged Model (CDM)	ESDA/JEDEC JS-002-2018	2038A00	(9/0)*1	±1000V
ESD: Human Body Model (HBM)	ESDA/JEDEC JS-001-2017	2038A00	(15/0)*1	±2000V
Latch-up (LU)	JESD78E	2038A00	(6/0)*1	Class I ±100mA
MSL Precondition, prior to THB, HAST, TC, PCT, UHAST, HTSL	J-STD-020, Reflow: Tp>=260 ℃, tp>=30sec, 3 ×reflows	1037651	(240/0)*1	MSL = 3
High Temperature Storage Life (HTSL)	JESD22-A103, @150 ℃ for 1000 hours	1037651	(80/0)*1	
Temperature Cycling (TC)	JESD22-A104, from -65 ℃ to 150 ℃ for 1000 cycles	1037651	(80/0)*1	
Accelerated Moisture Resistance- Unbiased Autoclave after (PCT)	JESD22-A102, @121 ℃/100%RH/205 kPa for 168 hours	1037651	(80/0)*1	
Solderability Test	J-STD-002E	1037651	(15/0)*1	

3. Failure Rate Calculation

Sample Size:	2985
Rejects:	0
Activation Energy (eV):	0.7
Failure Rate (FIT@60%CL):	1.15 FIT
MTBF (years):	99376 Years

Revision / Update History

Revision	Reason for Change	Date	EQD Engineer
0.0	Initial release	Aug.2023	Joker Bai

Appendix: Description of Reliability Test and Failure Rate Calculation

High Temperature Operating Life Test

Purpose: This test is a worst-case life test that checks the integrity of the product. The high temperature testing is use for acceleration of any potential failures over time. The calculation for failure rate (FIT) using the operating ambient temperature is done using the Arrhenius equation.
Condition: 125 ℃ @ V_{in} max
Pass Criteria: All units must pass the min/max limits of the datasheet.

ESD Test

Purpose: The purpose of the ESD test is to guarantee that the device can withstand electrostatic voltages during handling.
Condition: Human Body Model and Charged Device Model
Pass Criteria: ESD testing on every pin. The device must be fully functional after testing and pass the min/max limits in the datasheet.

IC Latch-Up Test

Purpose: The purpose of this specification is to establish a method for determining IC latch-up characteristics and to define latch-up failure criteria. Latch-up characteristics are extremely important in determining product reliability and minimizing No Trouble Found (NTF) and Electrical Overstress (EOS) failures due to latch-up.
Condition: Voltage and current injection
Pass criteria: All pins with the exception of "no connect" pins and timing related pins, shall be latch-up tested. The device must be fully functional after testing and pass the min/max limits in the datasheet.

Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

Purpose: The purpose of this standard is to identify the classification level of nonhermetic solid state surface mount devices (SMDs) that are sensitive to moisture-induced stress so that they can be properly packaged, stored, and handled to avoid damage during assembly solder reflow attachment and/or repair operations.
Condition: Bake + moisture soak + 3X reflow at 260 ℃ (MSL1: 85℃/85%RH/168hours; MSL2: 85℃ /60%RH/168hours; MSL2a: 30℃/60%RH/696hours; MSL3: 30℃/60%RH/192hours; MSL4: 30 ℃/60%RH/96hours; MSL5: 30℃/60%RH/72hours; MSL5a: 30℃/60%RH/48hours; MSL6: 30℃ /60%RH/TOL;
Pass criteria: All units must pass the min/max limits of the datasheet

High Temperature Storage Life

Purpose: The test is typically used to determine the effects of time and temperature, under storage conditions, for thermally activated failure mechanisms and time-to-failure distributions of solid state electronic devices, including nonvolatile memory devices (data retention failure mechanisms).
Condition: Bake at 150 ℃
Pass Criteria: All units must pass min/max limits of the datasheet

Accelerated Moisture Resistance- Unbiased Autoclave

Purpose: To check the performance of the device in humid environments. This test checks the integrity of the passivation, poor metal to plastic seal and contamination level during assembly and material compatibility.
Condition: 121 ℃/15psig/100% RH (no bias)
Pass Criteria: All units must pass min/max limits of the datasheet

Temperature Cycle Test

Purpose: This test is used to evaluate the die attach integrity and bond integrity. This is similar to the Thermal Shock test, but can generate different failure modes due to the longer dwell time and gradual temperature change.
Condition: -65 ℃ to 150 ℃
Pass Criteria: All units must pass min/max limits of the datasheet

Failure Rate Calculation

The failure rate is gauged by a Failures-In-Time (FIT) based upon accelerated stress data. The unit for FIT is failure per billion device hour.

$$FIT\ Rate = \frac{(\chi^2/2) \times 10^9}{EDH}$$

Where

$\chi 2$ (Chi-Squared) is the goodness-of-fit test statistic at a specified level of confidence;
EDH= Equivalent Device Hours = AF ×(Life test sample size) ×(test duration);
AF= Acceleration Factor.

High Temperature Operating Life (HTOL) test is usually done under acceleration of temperature and voltage. The total number of failures from the stress test determines the chi-squared factor.

$$AF=AF_T \times AF_V$$

The Temperature Acceleration Factor AF_T:

$$AF_T = \exp\left(\frac{E_a}{k}\left(\frac{1}{T_{J(use)}} - \frac{1}{T_{J(stress)}}\right)\right)$$

T_{Juse} = Junction temp under typical operating conditions;
$T_{Jstress}$ =Junction temp under accelerated test conditions;
Ea is Activation energy=0.7eV;
K=Boltzmann's constant=8.62×10^{-5} eV/K.

The voltage Acceleration Factor AF_V:

$$AF_V = e^{\beta \times [V_{stress} - V_{use}]}$$

V_{use} = Gate voltage under typical operating conditions;
V_{stress} = Gate voltage under accelerated test conditions;
β = Voltage acceleration factor (in 1/Volts) and specified by technology.

MTBF (Mean Time Between Failure) equals to 10^9 /FIT (in hours).